H-Bridge/Full Bridge Array of P and N channel MOSFETs

1. Functional Description of the AMG-PI004

The AMG-PI004 is built by utilizing one of the latest state-of-the-art trench technologies to achieve ultra low resistance RDS(on) for the power MOSFETs. The complementary H-bridge consists of 2 PMOS/NMOS transistor pairs. Based on this trench-technology the input gate capacity is very low, so that high switching frequencies are possible thus making it ideal for use in different applications. The DFN8 package is footprint compatible with the SOP8 package, making the H-bridge an ideal choice for wide spread off high efficiency applications for motor driving, lighting, and power management.

2. Features

- ❑ Supply voltage 5VDC...60VDC
- ❑ Complementary N/P-MOS H-Bridge
- ❑ 60V/5.1A/ RDS(on) =34mΩ(typ)
  -60V/-4.2A/ RDS(on) =54mΩ(typ)
- ❑ Low QG of 9.86/12.6nC for PMOS/NMOS
  Low CISS of 1447pF/1378pF for PMOS/NMOS
- ❑ Low voltage gate drive VGS = ±20V
- ❑ RoHS compliant and green product
- ❑ Temperature Range -55C…+150C
- ❑ DFN8L (5mm x 6mm x 0.75 mm)

3. Application

The AMG-PI004 is suitable for motor driving, lighting and power management.

3.1. Application Circuit Example

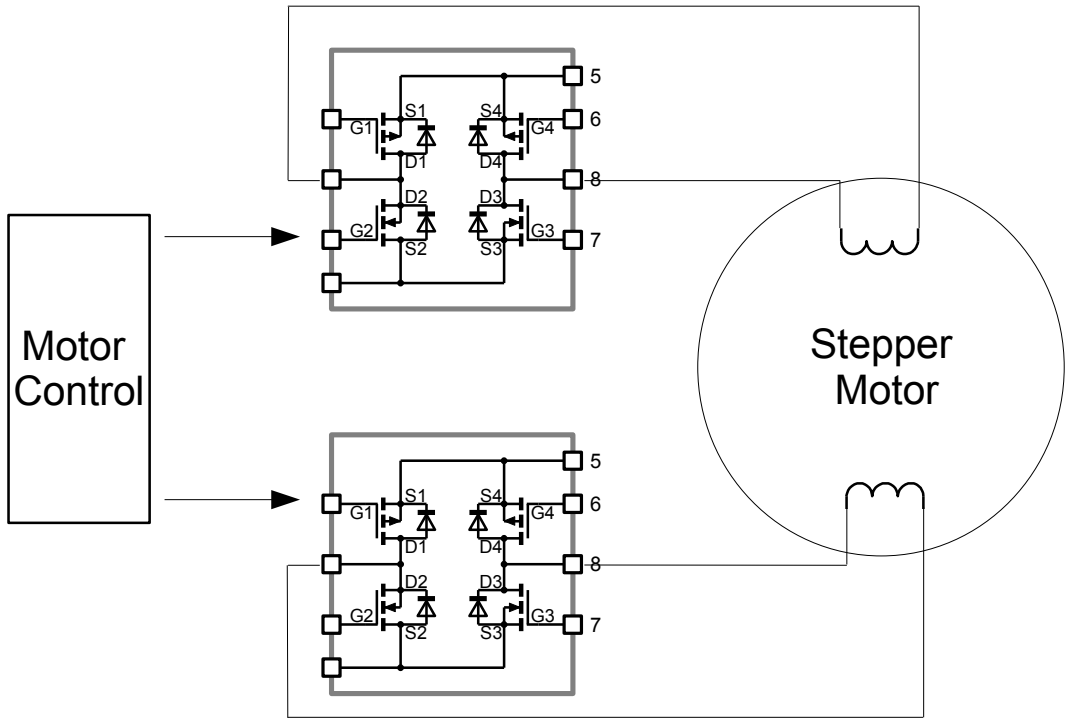


Figure 1: Application Circuit Example

3.2. Application Notes

The thermal resistance of the DFN8L package can be enhanced by using the bottom pad as heat sinks.

In order to lower the thermal resistance, vias should be placed below the Drain and Source pads. These vias should connect to big enough heat sinks within the PCB. This will also be beneficial for the ohmic resistance of the traces.

Table of Contents

4. Block Diagram

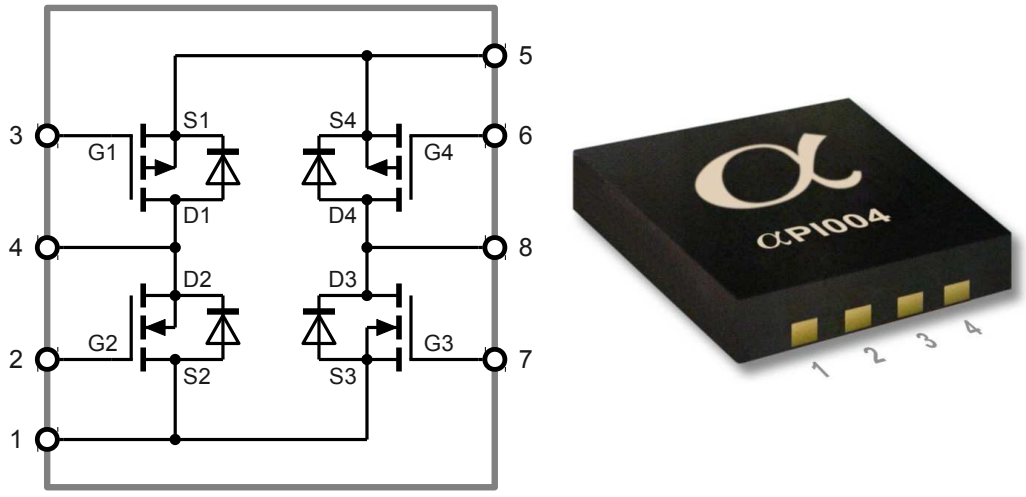


Figure 2: Block Diagram

5. Block Descriptions

2x PMOS and 2x NMOS

6. Pinning

PIN#	Symbol	Description
1	N-Source	Common NMOS Source, negative supply or GND
2	G2	Left NMOS Gate
3	G1	Left PMOS Gate
4	L-Drain	Left Drain, left load connection
5	P-Source	Common PMOS Source, positive supply
6	G4	Right PMOS Gate
7	G3	Right NMOS Gate
8	R-Drain	Right Drain, right load connection

7. Absolute Maximum Ratings

The Absolute Maximum Ratings may not be exceeded under any circumstances.

#	Symbol	Parameter	N-CH	P-Ch	Unit
1	V_{DS}	Drain-Source Voltage	60	-60	V
2	I_D	Drain Current - Continuous @V_{GS}=10V @T_C=25℃	5.1	-4.2	A
		Drain Current - Continuous @ V_{GS}=10V1、T_C=70℃	4.2	-3.5	A
3	I_{DM}	Pulsed Drain Current[2]	15	-12	A
4	V_{GS}	Gate-Source Voltage	± 20	± 20	V
5	P_D	Power Dissipation[4] (T_C= 25°C)	2.2	2.2	W
6	T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		℃

Note(s): none

8. Electrical Characteristics

8.1. Thermal Data

#	Symbol	Parameter	Typ	Max	Unit
1	$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	-	328.15	K/W
2	$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	-	277.15	K/W

8.2. N-Channel Electrical Characteristics

T_j = 25°C unless otherwise noted

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics							
1	BV_{DSS}	Drain-Source Breakdown	V_{GS}=0V , I_D=250uA	60	-	-	V
2	$\triangle BVDSS/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	-	0,063	-	V/K
3	I_{DSS}	Drain-Source Leakage Current	V_{DS}=48V , V_{GS}=0V , T_J=25℃	-	-	1	uA
			V_{DS}=48V , V_{GS}=0V , T_J=55℃	-	-	5	
4	I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	-	-	±100	nA
On Characteristics							
1	$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS}, I_D=250uA	1,2	-	2,5	V
2	$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		-	-5.24	-	mV/K

H-Bridge/Full Bridge Array of P and N channel MOSFETs

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2	$R_{DS(ON)}$	Static Drain-Source On-Resistance²	V_{GS}=10V , I_D=5A	-	34	40	mΩ
			V_{GS}=4.5V , I_D=4A	-	37	48	
3	gfs	Forward Transconductance	VDS=5V , ID=4A	-	28	-	S
Dynamic Characteristics							
1	C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	-	1378	-	pF
2	C_{oss}	Output Cap		-	86	-	
3	C_{rss}	Reverse Transfer Capacitance		-	64	-	
Switching Characteristics							
1	R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	-	3.2	6.4	Ω
2	Q_g	Total Gate Charge (4.5V)	V_{DS}=48V, V_{GS}=4.5V, I_D=4A	-	12.6	-	nC
3	Q_{gs}	Gate-Source Charge		-	3.2	-	
4	Q_{gd}	Gate-Drain Charge	V_{DS}=48V, V_{GS}=4.5V, I_D=4A	-	6.3	-	nC
5	$T_{d(on)}$	Turn-On Delay Time	V_{DD}=30V , V_{GS}=10V R_G=3.3Ω I_D=4A	-	8	-	ns
6	T_r	Rise Time		-	14.2	-	
7	$T_{d(off)}$	Turn-off Delay Time		-	24.4	-	
8	T_f	Fall Time		-	4.6	-	
Drain-Source Diode Characteristics and Maximum Ratings							
1	I_S	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	-	-	5.1	A
2	I_{SM}	Pulsed Source Current[2,4]		-	-	12	A
3	V_{SD}	Diode Forward Voltage²	V_{GS}=0V , I_S=1A , T_J=25°C	-	-	1.2	V

Note(s):

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≦ 300us , duty cycle ≦ 2%
3. The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V, L=0.1mH, I_{AS}=22.6A
4. The power dissipation is limited by 150°C junction temperature.
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

8.3. P-Channel Electrical Characteristics

T_j = 25°C unless otherwise noted

#	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics							
1	BV_{DSS}	Drain-Source Breakdown	V_{GS}=0V , I_D=250uA	-60	-	-	V
2	$\triangle BV_{DSS}$ /$\triangle T_J$	BVDSS Temp. Coefficient	Reference to 25°C , I_D=-1mA	-	-0.03	-	V/°C
3	I_{DSS}	Drain-Source Leakage Current	V_{DS}=-48V , V_{GS}=0V, T_J=25°C	-	-	1	uA
			V_{DS}=-48V , V_{GS}=0V, T_J=55°C	-	-	5	
4	I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
On Characteristics							
1	$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS}, I_D =-250uA	-1.5	-	-3.0	V
2	$\triangle V_{GS(th)}$	VGS(th) Temp. Coefficient		-	4.56	-	mV/°C
3	$R_{DS(ON)}$	Static Drain-Source On-Resistance²	V_{GS}=-10V , I_D=-4A	-	60	80	MΩ
			V_{GS}=-4.5V , I_D=-3A	-	73	90	
4	gfs	Forward Transconductance	V_{DS}=-5V , I_D=-3A	-	15	-	S
Dynamic Characteristics							
1	C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz	-	1447	-	pF
2	C_{oss}	Output Capacitance		-	97.3	-	
3	C_{rss}	Reverse Transfer Capacitance		-	70	-	
Switching Characteristics							
1	R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	-	21	42	Ω
2	Q_g	Total Gate Charge (-4.5)	V_{DS}=-48V, V_{GS}=-4.5V, I_D=-3A	-	9.86	-	nC
3	Q_{gs}	Gate-Source Charge		-	3.08	-	
4	Q_{gd}	Gate Charge		-	2.95	-	
5	$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, V_{GS}=-10V , R_G=3.3Ω I_D=-1A	-	28.8	-	ns
6	T_r	Rise Time		-	19.8	-	
7	$T_{d(off)}$	Turn-Off Delay Time		-	60.8	-	
8	T_f	Fall Time		-	7.2	-	
Drain- Diode Characteristics and Maximum Ratings							
1	I_s	Continuous Source Current[1,6]	V_G=VD=0V, Force Current	-	-	-4.2	A
2	I_{SM}	Pulsed Source Current[2,6]		-	-	-10.5	A
3	V_{SD}	Diode Forward Voltage²	V_{GS}=0V , I_S-1A , T_J=25°C	-	-	-1.2	V

Note(s):

1. The data tested by surface mounted on a 1 inch² FR-4 with 2OZ copper.

2. The data tested by pulse, pulse width
3. The EAS data shows MAX. rating. The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-26.6A
4. The power dissipation is limited by 150℃ junction temperature.
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

9. Characteristics

9.1. N-channel Typical Characteristics

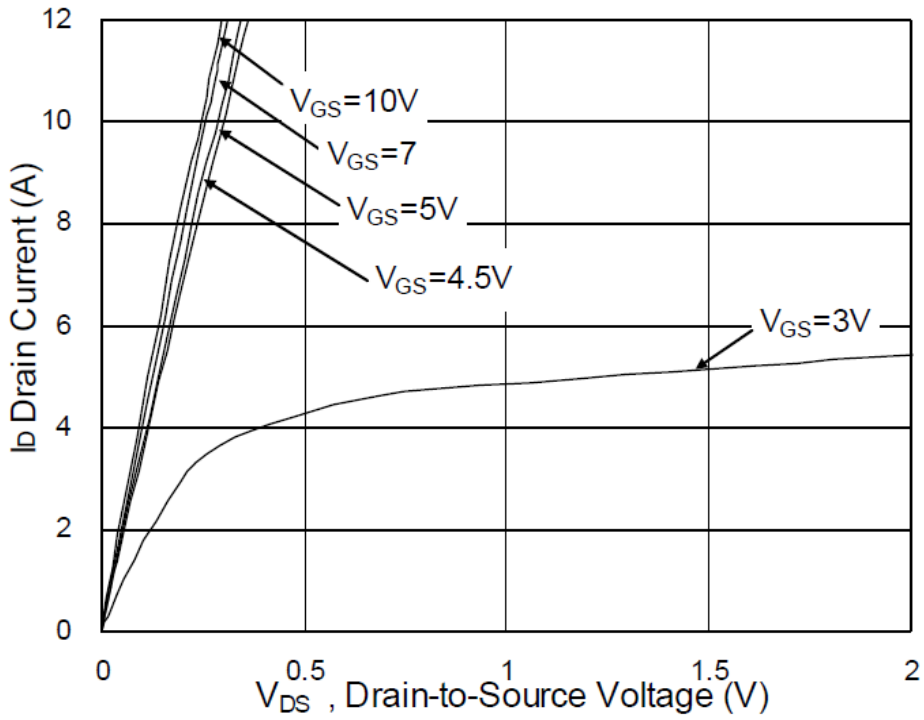


Figure 3: Typical Output Characteristics

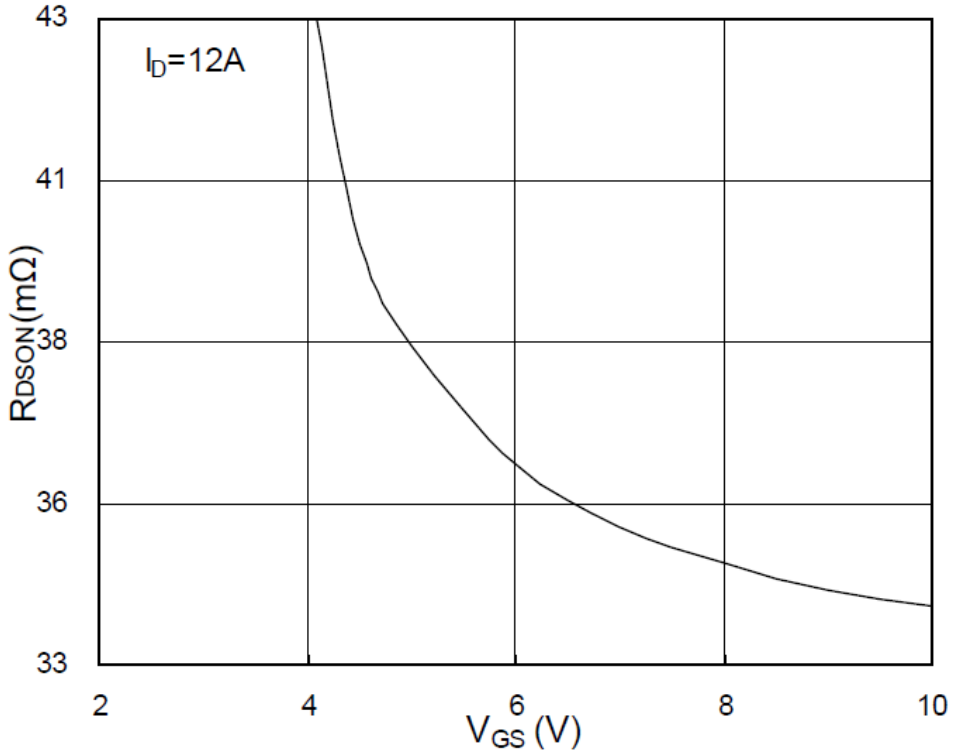


Figure 4: On-Resistance vs. Gate-Source Voltage

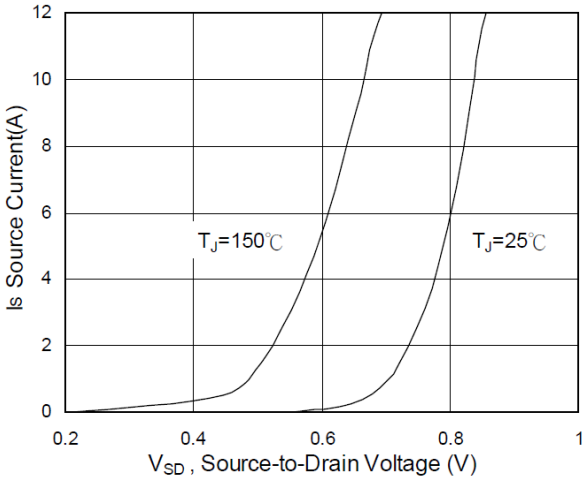


Figure 5: Forward Characteristics of revers

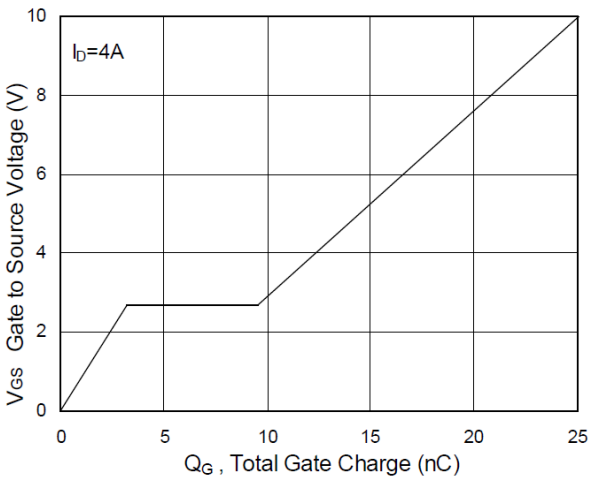


Figure 6: Gate-Charge Characteristics

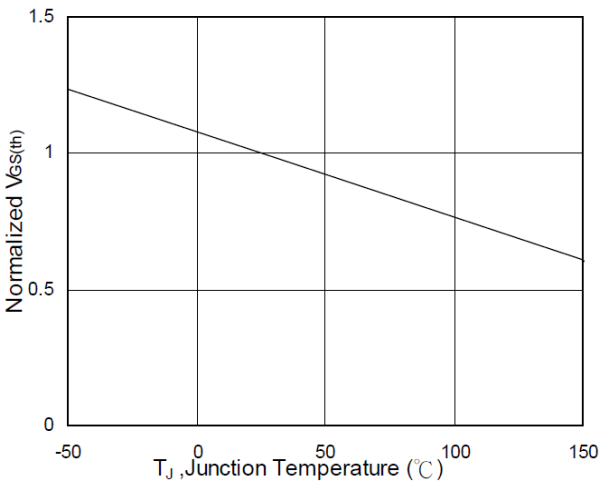


Figure 7: Normalized $V_{GS(th)}$ vs. T_j

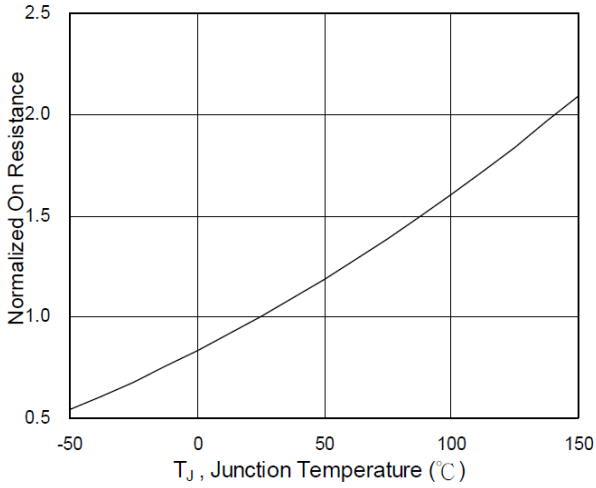


Figure 8: Normalized R_{DSON} vs. T_j

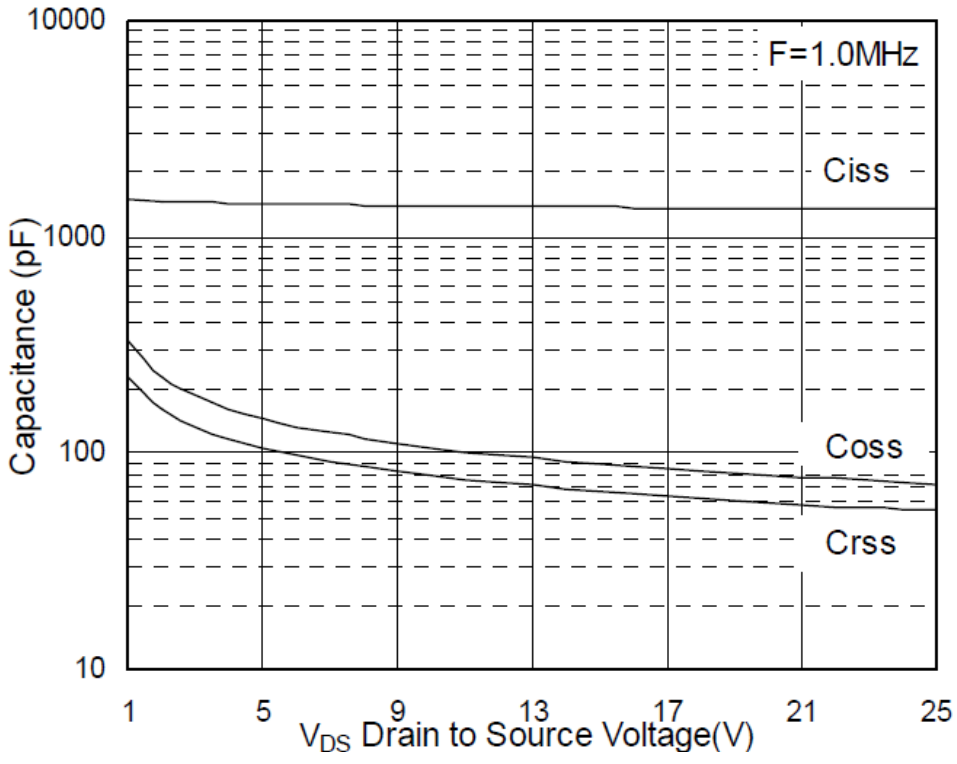


Figure 9: Capacitance

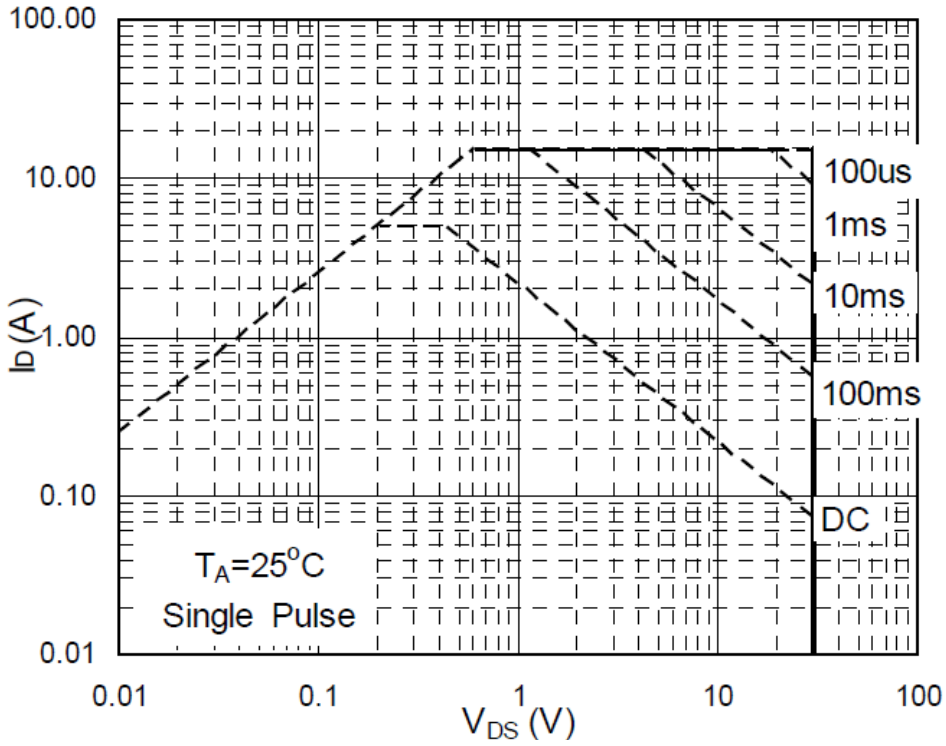


Figure 10: Safe Operating Area

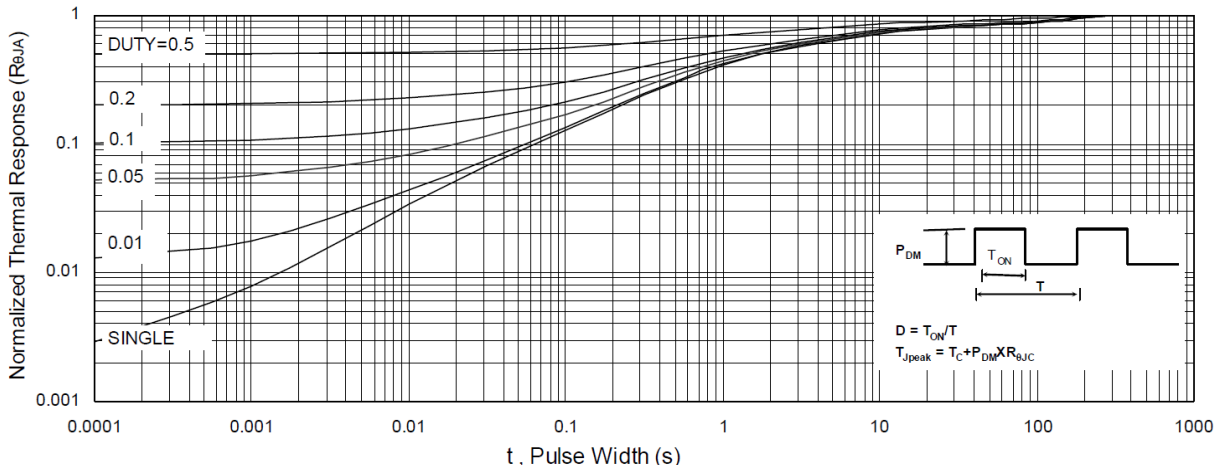


Figure 11: Normalized Maximum Transient Thermal Impedance

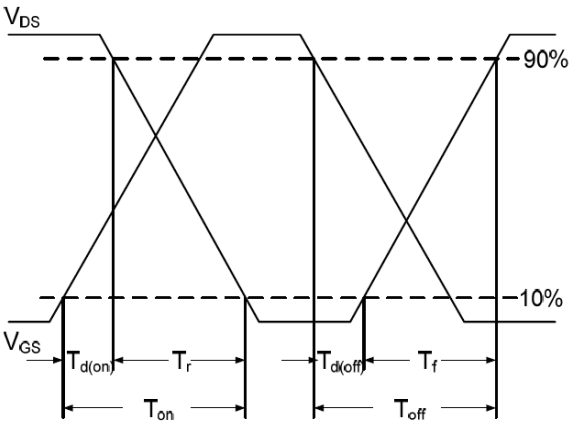


Figure 12: Switching Time Waveform

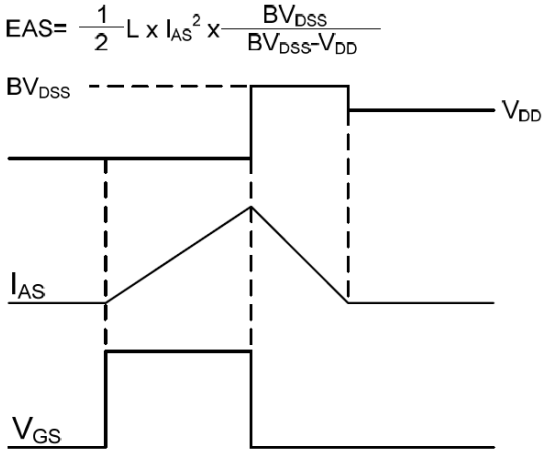


Figure 13: Unclamped Inductive Waveform

9.2. P-channel Typical Characteristics

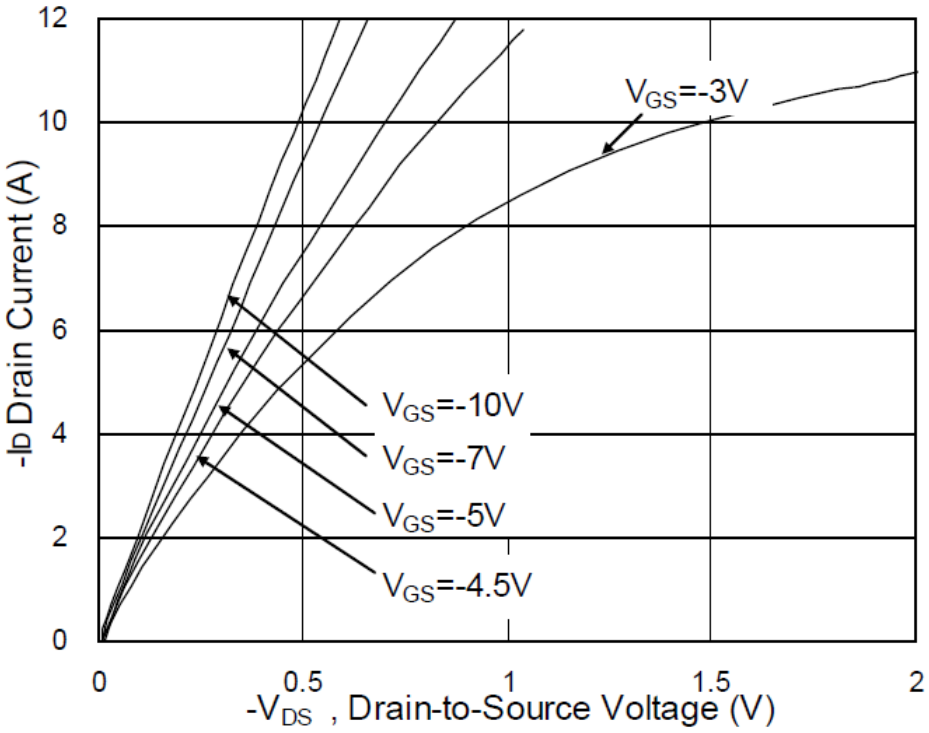


Figure 14: Typical Output Characteristics

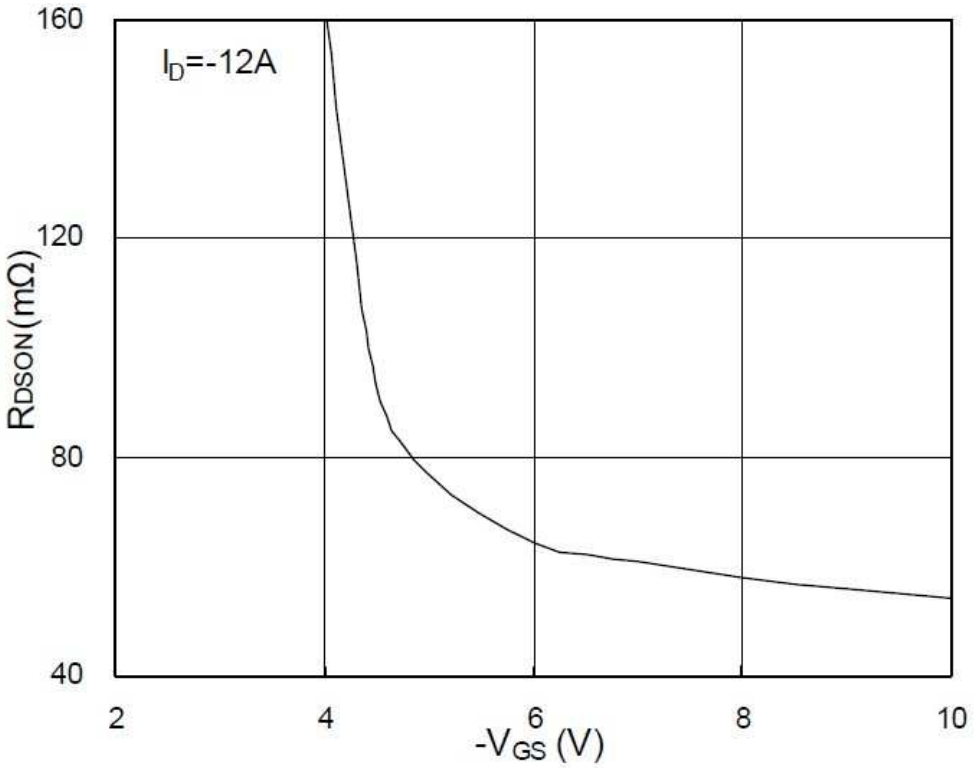


Figure 15: On-Resistance vs. Gate-Source Voltage

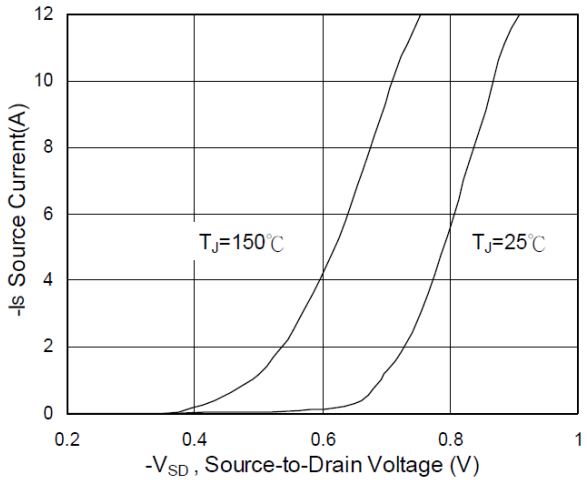


Figure 16: Forward Characteristics of reverse

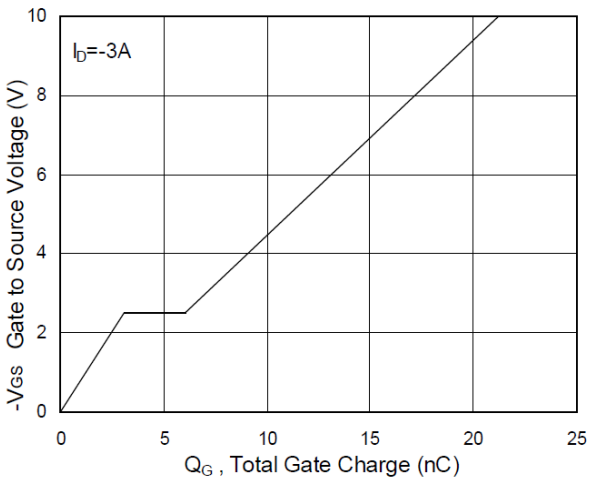


Figure 17: Gate Charge Characteristics

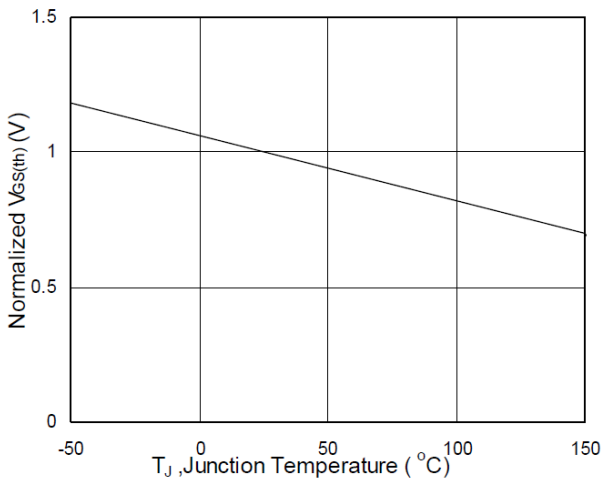


Figure 18: Normalized $V_{GS(th)}$ vs. T_j

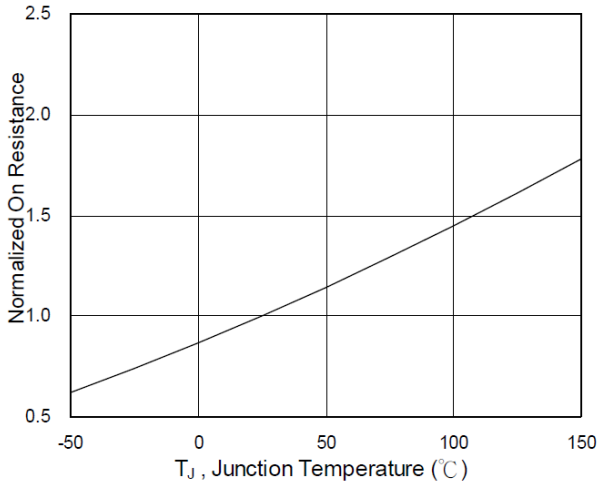


Figure 19: Normalized R_{DSON} vs. T_j

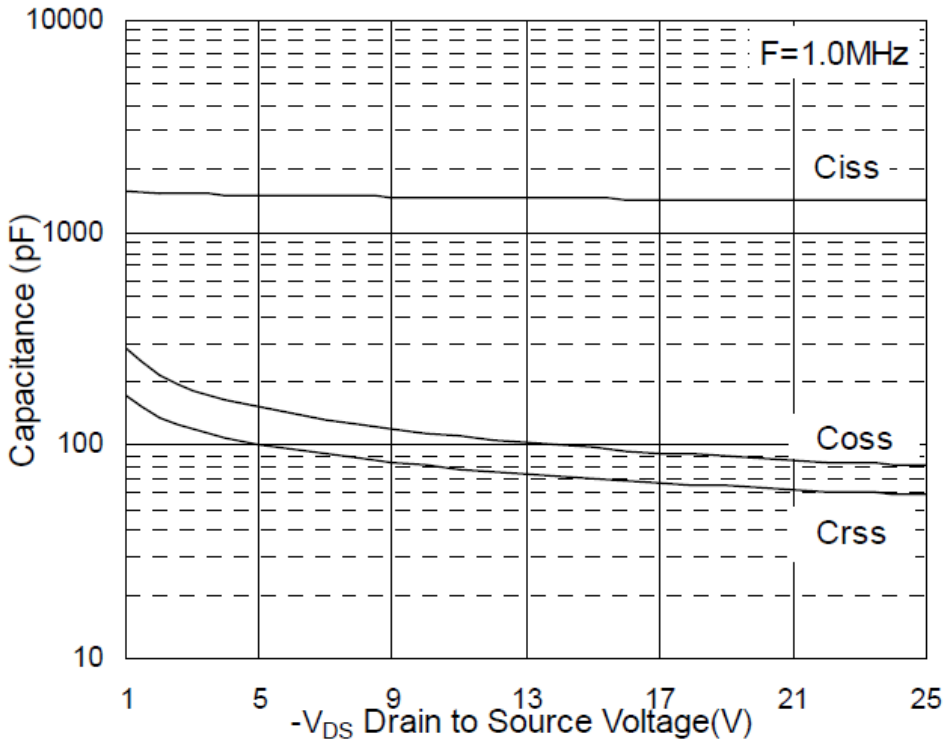


Figure 20: Capacitance

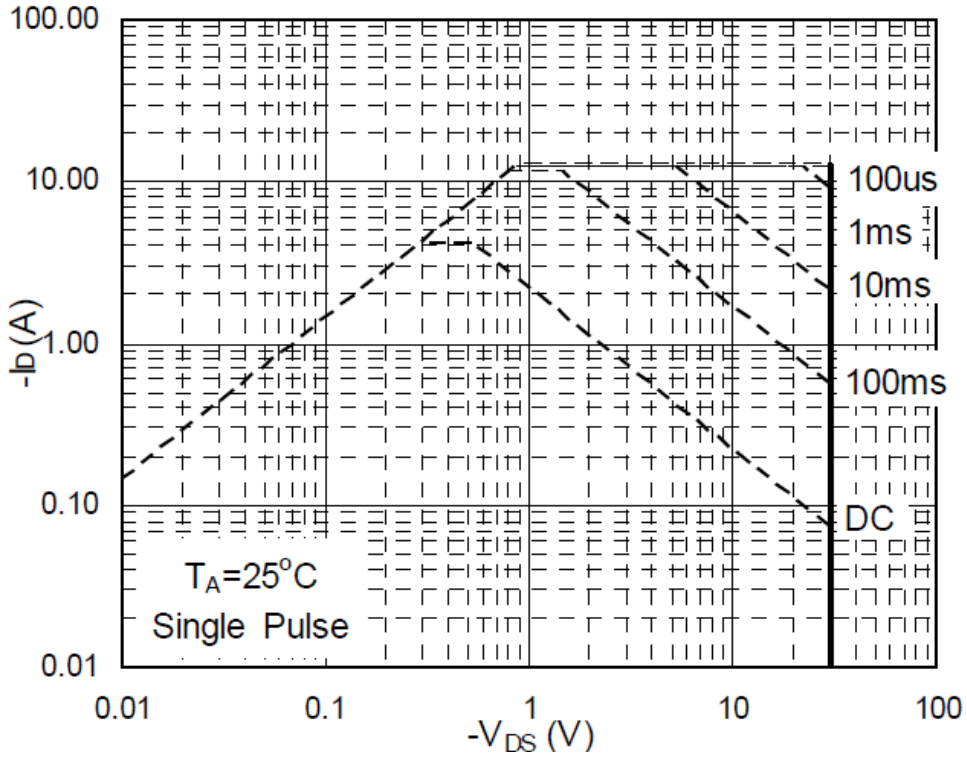


Figure 21: Safe Operating Area

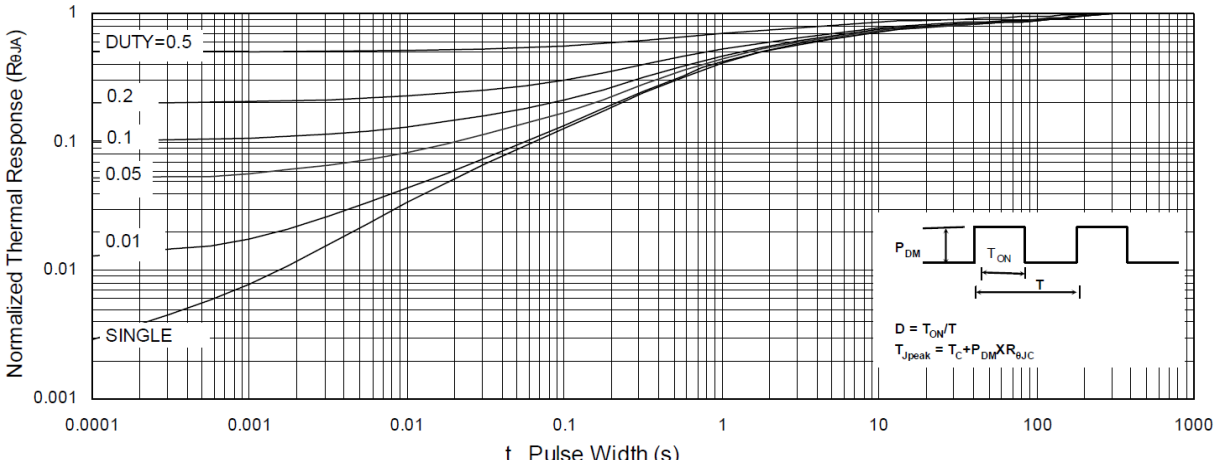


Figure 22: Normalized Maximum Transient Thermal Impedance

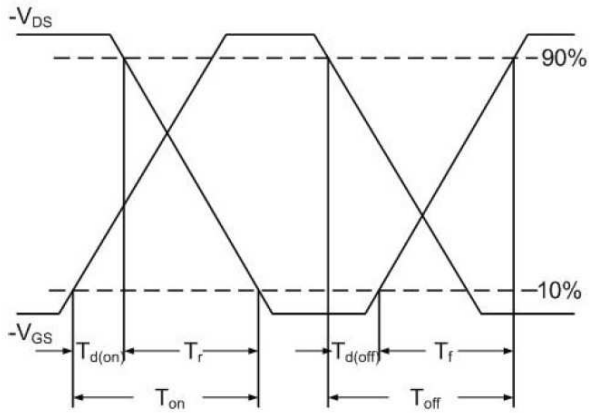


Figure 23: Switching Time Waveform

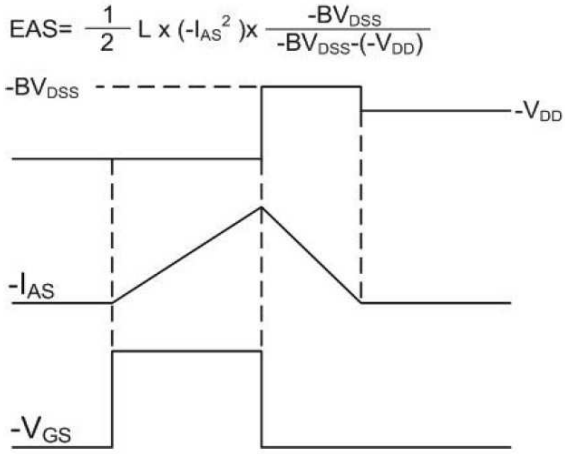
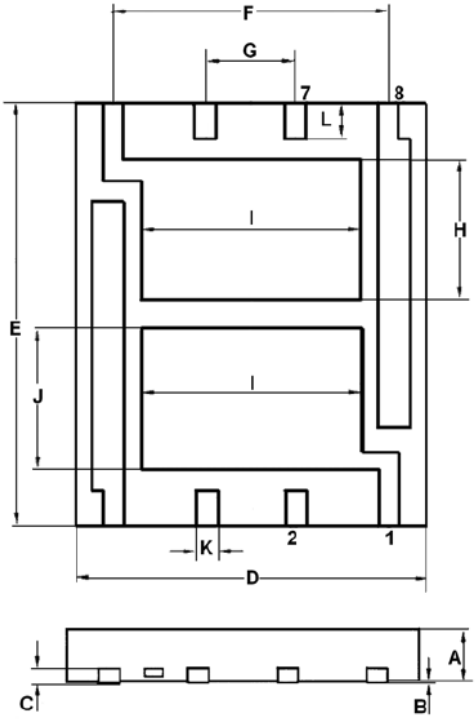


Figure 24: Unclamped Inductive Waveform

10. IC-Package

	Dimensions in mm		
	Min	Typ	Max
A	0.70	0.75	0.80
B	-	0.02	0.05
C	0.18	0.20	0.25
E	5.90	6.00	6.10
F	3.81 BSC		
G	1.28 BSC		
H	1.90	2.00	2.10
I	3.02	3.12	3.22
J	1.90	2.00	2.10
K	0.30	0.325	0.35
L	0.49	0.50	0.55



11. Ordering Information

AMG-PI004-IDF08R (DFN8L shipment in tape & reel)

12. IC-Marking

IC name = PI004

Date code = YYWW

Lot number = XXYYZZ

13. Notes and Cautions

13.1. ESD Protection

The Requirements for Handling Electrostatic Discharge Sensitive Devices are described in the JEDEC standard JESD625-A. Please note the following recommendations:

- When handling the device, operators must be grounded by wearing a for the purpose designed grounded wrist strap with at least 1MΩ resistance and direct skin contact.
- Operators must at all times wear ESD protective shoes or the area should be surrounded by for ESD protection intended floor mats.
- Opening of the protective ESD package that the device is delivered in must only occur at a properly equipped ESD workbench. The tape with which the package is held together must be cut with a sharp cutting tool, never pulled or ripped off.
- Any unnecessary contact with the device or any unprotected conductive points should be avoided.
- Work only with qualified and grounded tools, measuring equipment, casing and workbenches.
- Outside properly protected ESD-areas the device or any electronic assembly that it may be part of should always be transported in EGB/ESD shielded packaging.

13.2. Storage conditions

The AMG-PI004 corresponds to moisture sensitivity classification ML2 , according to JEDEC standard J-STD-020, and should be handled and stored according to J-STD-033.

14. Disclaimer

Information given in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed for the consequences of its use nor for any infringement of patents or other rights of third parties that may result from its use. alpha microelectronics GmbH does not authorize or warrant any of its products for use in life support system equipment.

The values stated in Absolute Maximum Ratings may under no circumstances be exceeded. No warranty is given for use in life support systems or medical equipment without the specific written consent of alpha microelectronics gmbh. For questions regarding the application please contact the publisher.

The declared data are only a description of the product. They are not guaranteed properties as defined by law. Examples are given without obligations and cannot give rise to any liability. Reprinting of this data sheet – or any part of it – is not allowed without the license of the publisher. Data sheets are subject to change without any notice.

15. Contact Information

This data sheet is published by alpha microelectronics gmbh. To order samples or inquire information please contact:

alpha microelectronics gmbh
Im Technologiepark 1
15236 Frankfurt (Oder)
Germany

am.info@alpha-microelectronics.de
www.alpha-microelectronics.de

+49-335-557-1750 (telephone)
+49-335-557-1759 (fax)