HES-7™ | ASIC Prototyping

Scalable, Flexible Solution

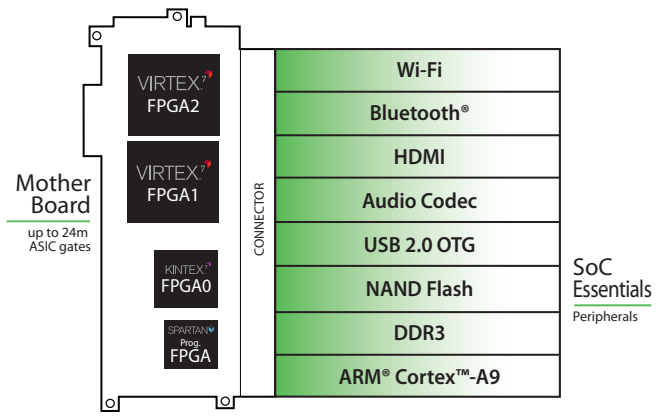
HES-7™ provides SoC/ASIC hardware verification and software validation teams with a scalable and high quality FPGA-based ASIC prototyping solution backed with an industry leading 1-year limited warranty. Each HES-7 board with dual Xilinx® Virtex®-7 2000T has 4 million FPGA logic cells or up to 24 million ASIC gates of capacity, not including the DSP and memory resources.

The HES-7 prototyping solution was architected to allow for easy implementation and expansion. Using only one or two large FPGAs, rather than multiple low density FPGAs, HES-7 does not require as much labor-intensive partitioning or tool expense. Using a non-proprietary HES-7 backplane connector, HES-7 can easily expand prototype capacity up to 96 million ASIC gates and can include the expansion of daughter boards.

Top Benefits

- **4 to 96 million Scalable ASIC Gate Capacity**
- **Easy To Use with Reduced Design Partitioning**
- **Expandable via Non-Proprietary Connector**
- **ARM® Cortex™ Support with Xilinx® Zynq™ All Programmable SoC**
- **Included SoC Peripherals: Media Interfaces, Memories, and Connectors**
- **Superior Quality Backed by Industry Leading 1-Year Warranty**
- **Supporting Systems:**   freeRTOS

HES-7™
ASIC Prototyping Platform



ARM Cortex Support

HES-7 supports ARM® dual-core Cortex™-A9 MPCore™ with Xilinx® Zynq™-7000 All Programmable SoC, allowing designers to leverage the serial processing capabilities of the Cortex-A9 processor for applications that require intensive computations and operating systems with the parallel processing capabilities of HES-7 ASIC prototyping platform to create applications across a diverse range of markets including: Video, Communications, Control Systems and Bridging.

The 4 to 96 million ASIC gate scalable capacity of HES-7, coupled with open-source Linux, Android, and FreeRTOS solutions available from Xilinx, delivers a powerful verification platform for HW/SW design teams.

Essential SoC Peripherals

HES-7 provides SoC Peripherals, allowing designers the ability to interface real-world stimuli to the design-under-test (DUT). Users can utilize gigabit Ethernet transceivers to develop networking applications, WLAN 802.11 b/g/n and Bluetooth® v2.1 to develop wireless systems, or High Performance HDMI Transmitter to develop home entertainment products. Memories and connectors provide additional data storage for read/write capability of today's popular memory interfaces, and the ability to connect external hardware with the HES-7.

Configuration		Capacity	FPGAs	FPGA I/O Connectivity		SoC Essentials
				(720 I/O/360 LVDS)	GTX (6.6 Gbps)	
SINGLEFPGA	**HES-7 XV690**	4m ASIC Gates	1 XC7VX690T	240/120 FPGA1	16 GTX FPGA1	Peripherals
	HES-7 XV2000	12m ASIC Gates	1 XC7V2000T	240/120 FPGA1	16 GTX FPGA1	Peripherals
DUAL FPGA	**HES-7 XV1380**	8m ASIC Gates	2 XC7VX690T	240/120 FPGA1 480/240 FPGA2	16 GTX FPGA1 28 GTX FPGA2	Peripherals/ ARM® Cortex™-A9
	HES-7 XV4000	24m ASIC Gates	2 XC7V2000T	240/120 FPGA1 480/240 FPGA2	16 GTX FPGA1 28 GTX FPGA2	Peripherals/ ARM® Cortex™-A9
	HES-7 Backplane	96m ASIC Gates	8 XC7V2000T	240/120 FPGA1 (3,5,7) 480/240 FPGA2 (4,6,8)	16 GTX FPGA1 (3,5,7) 28 GTX FPGA2 (4,6,8)	

Key Benefits

ARM Cortex Support:

- Utilize ARM® dual-core Cortex™-A9 MPCore™ Microprocessor
  - Maximum Frequency of up to 1 GHz
  - Enhanced with NEON Extension and Single & Double Precision Floating point unit
  - 32 kB Instruction & 32 kB Data L1 Cache
- Integrated processing platform with FPGA logic reduces bill-of-material (BOM) up to 40
- Free open-source Linux, Android, and FreeRTOS solutions available from Xilinx

I/O Connectivity:

- 322 high-speed inter-FPGA connections
  - FPGA0 ↔ FPGA1: 96/48 (SE/Diff)
  - FPGA1 ↔ FPGA2: 226/113 (SE/Diff)
- High-speed 25 Gbps connectors for expansion
  - Backplane and daughterboard interface
- 5 Global clock inputs connected to all FPGAs
- 89 special purpose global lines to all FPGAs
  - For programming, expanded debug, etc.

Customizable Clocking:

- 5 customizable, low skew, global clocks from backplane
  - User programmable PLLs (2KHz to 1.4GHz)
  - MMCX connectors for external clock inputs (0 - 450MHz)
- 60 differential global and local clock inputs from backplane
  - 20 multi-region and single region differential pairs to FPGA1
  - 40 multi-region and single region differential pairs to FPGA2

Memory:

- Up to 16GB of DDR3 memory supported with SO-DIMM sockets
- UP to 64GB of DDR3 with 4 HES-7 boards connected through backplane
- 8GB Flash memory connected to FPGA0
- Micro SD card socket available for stand-alone configuration

Peripheral Support:

- Media Interfaces: Ethernet PHY 10/100/1000, Wi-Fi and Bluetooth, USB 2.0 DEVICE, USB 2.0 HOST, USB 2.0 OTG, HDMI, and Audio Codec (Stereo Speaker and MIC Interfaces)
- Memories: SD Socket, SPI Flash, I2C Flash, NAND Flash, SO-DIMM DDR2
- Connectors: ARM Debug, RS232, I2C, SPI, and GPIO
- Additional 4x DDR3 Memory peripheral included with Xilinx Zynq

Protocol Support:

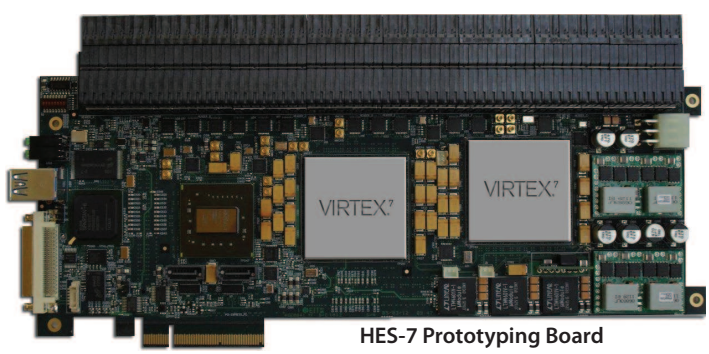
- PCI-Express finger connector for inside PC operation
- PCI-Express cable connector for outside PC operation
- USB 2.0/3.0 connector
- JTAG connector
- 2 SATA Connectors (Device/Host)

Diagnostics:

- Self diagnostic button and status LEDs for hardware diagnostic

Daughterboard Support:

- Leverages non-proprietary 25 Gbps backplane connectors
- Technical specification on the interface available for daughterboard development



HES-7 Prototyping Board

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