

DO-254 FPGA Level In-Target Testing

MIL/AERO



DO-254/CTS™

The Standard

RTCA DO-254/EUROCAE ED-80, "Design Assurance Guidance for Airborne Electronic Hardware" is currently recognized by the FAA via FAA AC 20-152 as a means of compliance and guidance for the design assurance of complex electronic hardware such as FPGAs, PLDs and ASICs in airborne systems.

The Challenges in Hardware Verification

Functional verification of digital designs in real hardware has been a serious undertaking when designing under DO-254 standard. Chapter 6.2 Verification Process of DO-254 specifies that requirements must be preserved and verified from RTL simulation stage to hardware verification stage. In doing this, designers are presented with significant challenges such as:

- Limited controllability and visibility of FPGA I/Os
- Ensuring RTL simulation and hardware testing results match
- Development of test vectors to cover all design requirements
- Results capturing and documentation
- Lack of automation in the verification cycle

The Solution

Aldec's DO-254/CTS is a certifiable at-speed in-target testing environment for Level A/B complex designs, and is dedicated to address the stringent guidelines of DO-254 Chapter 6.2 Verification Process. DO-254/CTS consists of a fully customized hardware and software package designed to replay RTL simulation during hardware testing without any changes to the DUT and testbench. It provides a single and automated environment to test all FPGA level requirements ideal for DO-254 hardware verification. The components of DO-254/CTS are:

- COTS Mother Board
- Custom Daughter Board
- Custom Software Package

Top Features

- At-Speed Design Verification in Target Devices
- For use with Altera®, Lattice®, Microsemi™ & Xilinx® devices
- Automatic Test Vector Generation for Target Devices
- Auto-Capture and Analysis of results at all Design Stages
- Easy Design Requirements Traceability
- Independent EDA Tool Assessment
- Significantly shortens Device Verification Time

The Flow

Step 1: Simulation of the DUT using the RTL simulator. DO-254/CTS provides a plug-in that generates two sets of vectors (no changes to design & testbench):

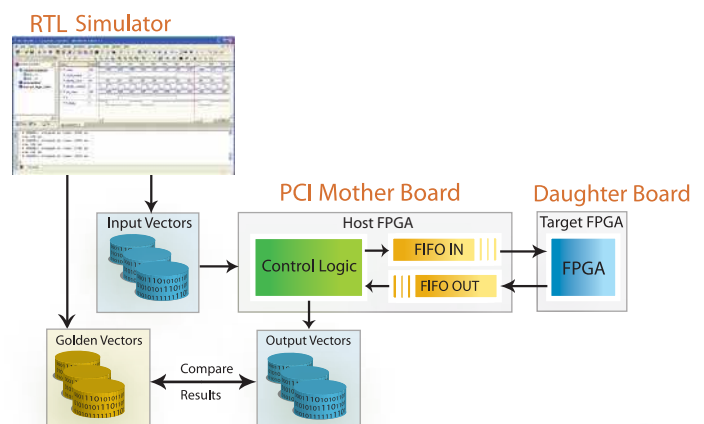
- **Input Vectors** - test vectors for hardware testing based on the testbench
- **Golden Vectors** - RTL simulation results which are used for comparison

Step 2: Programming of DUT bit file to the FPGA daughter board.

Step 3: In-target testing at full speed with the mother board and daughter board using the Input Vectors as test vectors.

Step 4: Capturing of in-target testing results called Output Vectors.

Step 5: Comparison of Output Vectors with Golden Vectors using waveform viewer.



Traditional Hardware Verification

DO-254 CTS Approach

Input Type	Real Data	RTL Test Vectors
Verification Type	At Speed	At Speed
Target Device	Yes	Yes
Test Data Generation	Manual Engineering Time Required	Automatic, No Additional Development Required
Test Environment Setup	Manual Connections of Wires and Cables	PCI/PCIe Based Hardware Boards
FPGA I/O Access	Limited Controllability	Complete Controllability & Visibility
Output Format	From Logic Analyzer, Oscilloscope	RTL Simulator Waveform Format
RTL and Hardware Results Comparison	Limited	Easy & Automated
FPGA Device Verification Time	Manual Process & Takes Years to Complete	Automated Process & Only Takes Weeks to Complete
Development Cost	Very High	Reduced Substantially

KEY Benefits

FPGA Level In-Hardware Verification

In compliance with the document FAA AC 20-152, verification at the FPGA level must be done to ensure completeness of testing. FPGA level verification is performed before system level verification. All FPGA level requirements verified using DO-254/CTS do not have to be verified again at the system level per RTCA/DO-254 specification sections 6.2 and 6.2.2.



DO-254/CTS Mother Board

Running at Required Operational Speed in excess of 250 MHz

Allows streaming of test vectors through the FPGA inputs at the required operational speed using real clocks in excess of 250 MHz. If the required simulation time is 500ms, then hardware testing completes within 500ms. Additional features to vary the frequency and voltage to $\pm 10\%$ can also be used for robustness.

Automatic Generation of Test Vectors for Hardware Testing

Development of test vectors for hardware testing for an average Level A/B design normally takes 6-12 months manual engineering time. DO-254/CTS is equipped with a utility that converts the testbench within minutes into test vectors to be used for hardware testing.

Hardware Testing Results Visualization with Waveform Viewer

Allows capturing and visualization of results using the simulator's standard waveform viewer, providing storage for waveform files of up to 16TB and capturing of results immediately after simulation.

Single-Environment to Verify all FPGA Level Requirements

It consists of custom hardware with PCIe interface and software providing a single-environment to test all FPGA level requirements, specifically designed to avoid manual bypasses of cables and wires which are typically prone to errors and bugs.

Automated In-Hardware Testing

DO-254/CTS is a "push-button" automated in-hardware testing environment to test all FPGA level requirements. It is equipped with a utility to automatically compare RTL simulation results with hardware testing results. The utility displays either a PASS or FAIL message in which results can be further investigated using a standard waveform viewer.

Target Device Testing

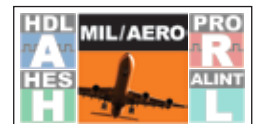
The design must be tested in the target device per RTCA/DO-254 specification sections 1.1 and 6.3.1. DO-254/CTS consists of a custom daughter board that contains the specific family/package or part number of the FPGA/PLD device from vendors such as Altera, Lattice, Microsemi (Actel) and Xilinx.



DO-254/CTS Custom Daughter Board

Integration with 3rd Party RTL Simulator, Synthesis and P&R

DO-254/CTS can be used with any 3rd party RTL Simulator, Synthesis and P&R tools.



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