HES Hardware Emulation Solutions

HES™ (Harware Emulation Solution) is a patented trasaction-level harware emulation system for large and complex SOC with ASIC or FPGA designs of up to 37 Million ASIC gates. HES is an affordable, versatile hardware-based verification platform that provides a unified platform for Simulation Acceleration, SoC Emulation, HW/SW Co-Verification, Software Validation, ESL Co-Emulation and Virtual Prototyping. HES combines speed, value and power with automatic design compilation, standard testing interface and integration with industry leading hardware/software debugging tools providing seamless trasformation of existing ASIC prototyping into dynamic emulation.

Top Features

- Verification of SoC (ASIC or FPGA)
- 4MHz Transaction & Gate level Emulation
- Bit-Level Simulation Acceleration
- SCE-MI 2.0, SystemC C/C++, BlueSpec®
- Extensive Debugging (static/dynamic probes, memory access using GUI and API)
- Fully Scriptable Environment
- HES-Prototyping API for MATLAB® Files
- RTL Simulation Interfaces: Active-HDL™, NC-Sim®, ModelSim®, Riviera-PRO™, QuestaSim® and VCS-MX ®
- Synopsys® HAPS™ Hardware support
- Linux and Windows® 7/Vista/XP/2003/2000 and 32/64 bit support

Emulation

HES Emulation provides high-speed functional verification of the entire design, driven by at-speed multi-FPGA hardware boards. Aldec HES supports designs up to 37 Million ASIC gates and includes Transaction-Level Modeling (TLM), SystemC/C/C++ and SCE-MI for fast-logic emulation. HES interfaces to hardware boards from Synopsys® HAPS™ and provides fully-automated design setup, clock conversion and design partioning with advanced debugging.

Acceleration

HES can speed-up simulation in excess of10X, and is equipped to accelerate functional simulation of popular industry-leading RTL simulators from Aldec, Cadence®, Mentor Graphics® and Synopsys®. Acceleration mode combines robust debugging capabilities of HDL simulators and speed of FPGA prototyping boards. Portions of the design which take most CPU resources are off-loaded in hardware while simulation is being controlled by testbench in the HDL simulator. HES feeds selected test points from hardware into waveform viewers of leading HDL simulators and can accelerate any simulation performance.

Prototyping

HES prototyping is a verification approach used for setting up full-speed hardware prototype of the design in the HES FPGA prototyping board. It is a stand-alone verification tool connected to external hardware and lab equipment which can be controlled from a host workstation. Prototyping with HES also supports MATLAB files.

FEATURES

PRODUCT CONFIGURATIONS

Software Features	Proto	Xcell	Elite
Design Verification Manager [DVM™] Software	●	●	●
Daughterboard Connection (Connection to external boards and/or devices)	●	●	●
Manual Design Partitioning (Manual mapping based on resource information)	●	●	●
Automatic Design Partitioning - with signal multiplexing using LVDS		option	●
User Directed Partitioning (Manual assignment of design units)		option	●
Black-Box Functionality (Excludes modules from acceleration)		●	●
Mirror-Box Functionality (Mirrors modules from hardware in HDL simulation)		●	●
Clock Conversion and Analysis (Convert multiple clock domains to one)		●	●
Static Debugging Probes (Preserving design internal signals for static probes)	●	●	●
Static Debugging with Xilinx ChipScope™ Pro	●		●
Static Debugging with Aldec Logic Analyzer (ALA for SCE-MI)			●
Dynamic Debugging (for SCE-MI)			●
Emulation Results Stored in Waveform (ASDB and VCD)			●
Memory Model Mapping (Maps user memory to on-board memory)		●	●
DVM Scripting	●	●	●
C/C++ Testbench Wrapper for Acceleration		●	●
SystemC Testbench Wrapper for Acceleration		●	●
Synthesis Tool Support		●	●
Multi-FPGA Boards Support	option	option	●
Server Farm Support for Design Setup (Gridengine and LSF)		option	●
MATLAB API	option	option	●
Operating System Support			
Linux 32/64, Windows® 2000/2003/XP/Vista/7	●	●	●
Runtime Features			
Vector Based Emulation			●
SCE-MI 2.0 Hardware/Software Infrastructure (SCE-MI API C++)			●
SCE-MI 2.0 Co-Simulation Interface (Choice of one: Riviera-Pro, Active-HDL, QuestaSim, ModelSim, NC-Sim or VCS-MX)			●
HDL Co-Simulation Interface (Choice of one: Riviera-Pro, Active-HDL, QuestaSim, ModelSim, NC-Sim or VCS-MX)		●	●
Prototyping API and function library (Interface with C++ domain)	●		●
Prototyping Testbench Co-Sim Interface (Choice of one: Riviera-Pro, Active-HDL, QuestaSim, ModelSim, NC-Sim or VCS-MX)	●		●
Runtime Features for Debugging			
Memory Viewer (READ/WRITE access to design memory instances in the board)		option	●
Hardware Debugger		option	●
Dynamic Debugging in SCE-MI			●
Static Debugging - ALA - in SCE-MI			●
Boards Interface Features			
Hardware Boards Interface (choice of one prototyping board - Aldec, Synopsys; includes OS drivers)	●	●	●
Processor Support			
ARM 720T, 920T, 926 or 946includes OS drivers)			option

STANDARDS

accellera

IEEE

SYSTEMC™

SystemVerilog

PARTNERS

ALTERA

ARM

cadence™

The MathWorks

Mentor Graphics

SYNOPSYS®

SpringSoft

XILINX®

HDL ALINT PRO HES MIL/AERO

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