IS31AP4832

DUAL 2.5W AUDIO POWER AMPLIFIER AND STEREO HEADPHONE DRIVER WITH TONE CONTROL AND 3D ENHANCEMENT

January 2012

GENERAL DESCRIPTION

The IS31AP4832 is a monolithic integrated circuit that provides tone (bass and treble) controls as well as a stereo audio power amplifier capable of delivering 2.5W (Typ.) into 4Ω or 1.7W (Typ.) into 8Ω with less than 10% THD with a 5V supply. The IS31AP4832 uses flexible I^2C control interface for multiple application requirements.

The IS31AP4832 also features 3D sound circuitry which can be externally adjusted via a simple RC network. The headphone amplifier features Output Capacitor-less (OCL) architecture that eliminates the output coupling capacitors required by traditional headphone amplifiers.

The IS31AP4832 features a 13 step tone control for the headphone and stereo outputs. The device mode select and Tone are controlled through an I^2C compatible interface.

Thermal shutdown protection prevents the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown.

FEATURES

- 3D enhancement
- Treble and Bass control
- I^2C control interface
- Thermal shutdown protection
- Minimum external components
- Click-and-Pop suppression
- Micro-power shutdown
- Software & Hardware control shutdown function
- QFN-28(4mm × 4mm) package

Applications

- Cell phones, PDA, MP4,PMP
- Portable and desktop computers
- Desktops audio system
- Multimedia monitors

TYPICAL APPLICATION CIRCUIT

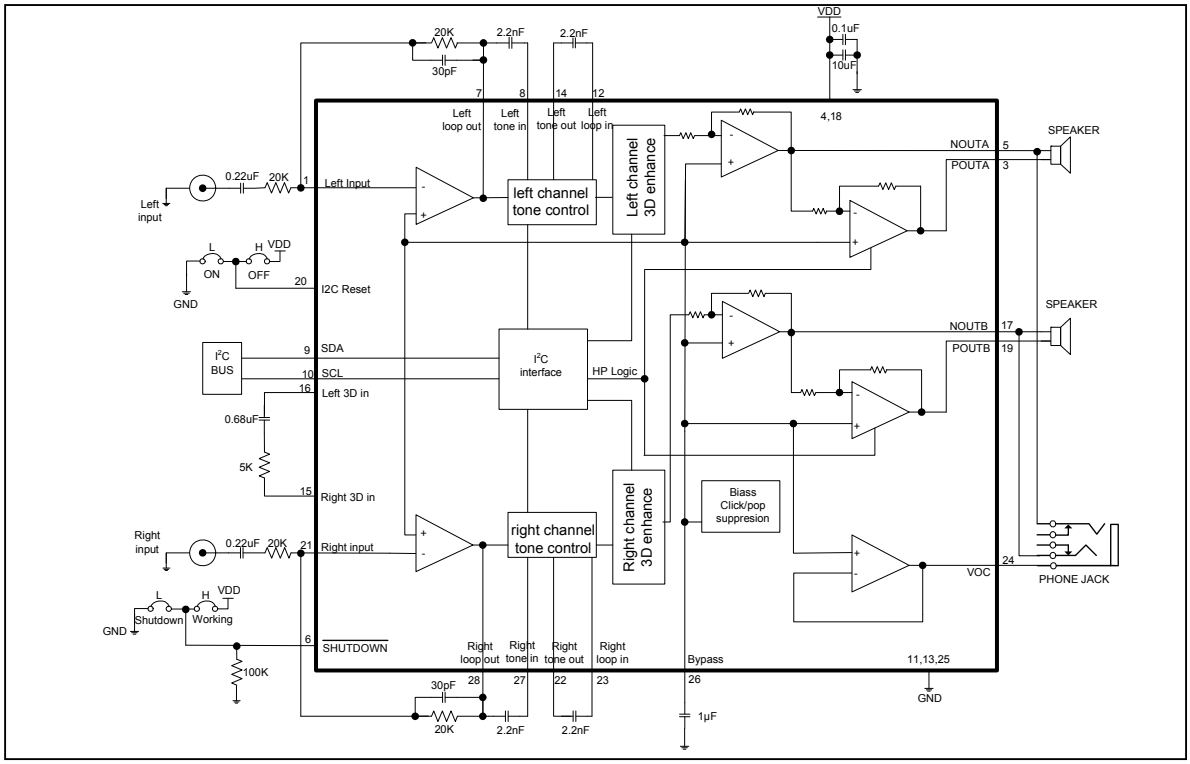
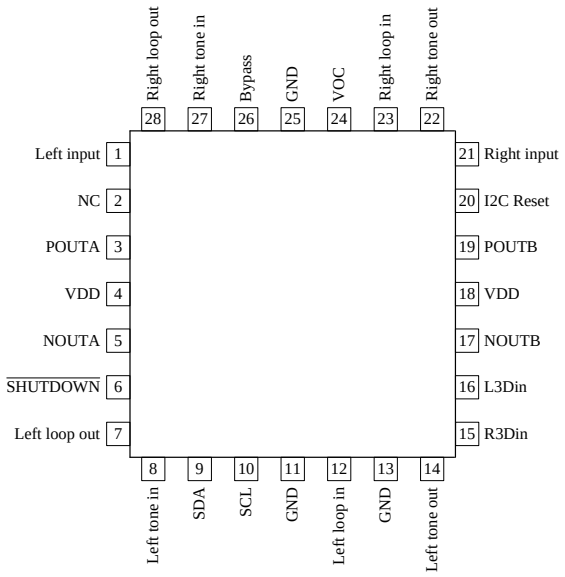


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-28	

PIN DESCRIPTION

No.	Pin	Description
1	Left input	Left channel input.
2	NC	Not connection.
3	POUTA	Left channel +output in BTL mode.
4,18	VDD	Supply voltage.
5	NOUTA	Left channel –output in BTL mode.
6	$\overline{\text{SHUTDOWN}}$	It will be into shutdown mode when pull low.
7	Left loop out	Left channel tone control loop out.
8	Left tone in	Left channel tone control in.
9	SDA	The input for the I2C data signal.
10	SCL	The input for the I2C clock signal.
11,13,25	GND	GND.
12	Left loop in	Left channel tone control loop in.
14	Left tone out	Left channel tone control out.
15	R3Din	Right channel 3D input.
16	L3Din	Left channel 3D input.
17	NOUTB	Right channel –output in BTL mode.
19	POUTB	Right channel +output in BTL mode.
20	I2C Reset	Reset chip logic and states. Internal pulled low to enable communication; pull high to reset IS31AP4832 to power on default mode and stop communication; a longer than 200ns high pulse can reset the chip.
21	Right input	Right channel input.
22	Right tone out	Right channel tone control out.
23	Right loop in	Right channel tone control loop in.
24	VOC	Reference (1/2 V_{DD}) of headphone.
26	Bypass	Bypass capacitor which provides the common mode voltage.
27	Right tone in	Right channel tone control in.
28	Right loop out	Right channel tone control loop out.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION
Industrial Range: -40℃ to +85℃

Order Part No.	Package	QTY/Reel
IS31AP4832-QFLS2-TR	QFN-28, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0.3V ~ +6.0V
Voltage at any input pin	−0.3V ~ V_{DD}+0.3V
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	−65°C ~ +150°C
Operating temperature range, T_A	−40°C ~ +85°C
Solder information, vapor phase (60s) infrared (15s)	215°C 220°C

Note:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{DD} = 5V, unless otherwise noted. Limits apply for T_A=25°C.

Symbol	Parameter	Condition	Typ.	Limit	Unit
V_{DD}	Supply voltage			3.0	V(min)
				5.5	V(max)
I_{DD}	Quiescent power supply current	V_{IN} = 0V, Io = 0A, BTL mode V_{IN} = 0V, Io = 0A, SE mode	8 5	11 7	mA(max) mA(max)
I_{SD}	Shutdown current	Standby mode	1.75	5	μA(max)
T_{WU}	Turn on time	C_{bp} = 1μF	130		ms
V_{OC}	inside ground for headphone	V_{IN} = 0	2.5		V
$V_{IL\ SD}$	Shutdown pin input low voltage			0.4	V(max)
$V_{IH\ SD}$	Shutdown pin input high voltage			1.4	V(min)
Bass Control					
A_R	Attenuator range	f = 100Hz, V_{IN} = 0.25V	±12		dB
As	Bass step size		2		dB
E_{SE}	Bass step size error		0.5		dB(max)
E_T	Bass tracking error		0.15		dB(max)
Treble Control					
A_R	Attenuator range	f = 10kHz, V_{IN} = 0.25V	±12		dB
As	Treble step size		2		dB
E_{SE}	Treble step size error		0.1		dB(max)
E_T	Treble tracking error		0.15		dB(max)
I^2C Bus Timing					
f_{max}	Maximum bus frequency			400	kHz
$T_{start;hold}$	Start signal: hold time before clock/data transitions			0.6	μs
$T_{d;setup}$	Data setup time			0.1	μs
$T_{c;high}$	Minimum high clock duration			0.6	μs
$T_{c;low}$	Minimum low clock duration			1.3	μs
$T_{stop;setup}$	Stop signal: setup time before clock/data transitions			0.6	μs
I^2C Bus Input And Output					
$V_{IL\ I2C}$	I^2C input low voltage			0.8	V(max)
$V_{IH\ I2C}$	I^2C input high voltage			1.6	V(min)
I_{IN}	Input current		0.15		μA
Vo	Output voltage—SDA acknowledge			0.2	V(max)

ELECTRICAL CHARACTERISTICS FOR BRIDGED-MODE OPERATION (5V)

Symbol	Parameter	Condition	Typ.	Limit	Unit
Vos	Output offset voltage	V_{IN} = 0V	5	25	mV(max)
Po	Output power	THD+N = 1%, f = 1kHz, R_L = 4Ω	1.9		W
		THD+N = 1%, f = 1kHz, R_L = 8Ω	1.2	1.0	W(min)
		THD+N = 10%, f = 1kHz , R_L = 4Ω	2.5		W
		THD+N = 10%, f = 1kHz, R_L = 8Ω	1.7		
THD+N	Total harmonic distortion +noise	1kHz A_{vd} = 2, R_L = 4Ω, Po = 0.5W	0.12		%
		1kHz A_{vd} = 2, R_L = 8Ω, Po = 0.2W	0.03		
PSRR	Power supply rejection ratio	Input grounded 217Hz, V_{ripple} = 200mV_{p-p} C_{bp} = 1μF, R_L = 8Ω	70		dB
		Input grounded 1kHz, V_{ripple} = 200mV_{p-p} C_{bp} = 1μF, R_L = 8Ω	64		dB
X_{talk}	Channel separation	f = 1kHz, C_{bp} = 1μF Stereo Enhanced control = Low	88		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	10		μV

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED OPERATION (5V)

Symbol	Parameter	Condition	Typ.	Limit	Unit
Po	Output power	THD+N = 0.5%,f = 1kHz, R_L = 32Ω	90	85	mW(min)
THD+N	Total harmonic distortion + noise	Po = 75mW,1kHz, R_L = 32Ω	0.015		%
PSRR	Power supply rejection raito	Input grounded 217Hz, V_{ripple} = 200mV_{p-p} C_{bp} = 1μF, R_L = 32Ω	75		dB
		Input grounded 1kHz, V_{ripple} = 200mV_{p-p} C_{bp} = 1μF, R_L = 32Ω	72		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	25		μV

ELECTRICAL CHARACTERISTICS FOR BRIDGED-MODE OPERATION (3V)

Symbol	Parameter	Condition	Typ.	Limit	Unit
Vos	Output offset voltage	V_{IN} = 0V	2.5		mV
Po	Output power	THD+N = 1%, f = 1kHz, R_L = 4Ω	0.7		W
		THD+N = 1%, f = 1kHz, R_L = 8Ω	0.45		
		THD+N = 10%, f = 1kHz, R_L = 4Ω	0.88		
		THD+N = 10%, f = 1kHz, R_L = 8Ω	0.55		
THD+D	Total harmonic distortion+noise	1kHz, A_{vd} = 2, R_L = 4Ω, Po = 0.35W	0.12		%
		1kHz, A_{vd} = 2, R_L = 8Ω, Po = 0.15W	0.08		
PSRR	Power supply rejection ratio	Input grounded 217Hz V_{ripple} = 200mV_{p-p}, C_{bp} = 1μF, R_L = 8Ω	71		dB
		Input grounded 1kHz V_{ripple} = 200mV_{p-p}, C_{bp} = 1μF, R_L = 8Ω	65		dB
V_{NO}	Output noise voltage	1kHz, A-weighted	10		μV

ELECTRICAL CHARACTERISTICS FOR SINGLE-ENDED OPERATION (3V)

Symbol	Parameter	Condition	Typ.	Limit	Unit
Po	Output power	THD+N = 0.5%,f = 1kHz, R_L = 32Ω	32		mW
THD+N	Total harmonic distortion+noise	Po = 25mW, 1kHz, R_L = 32Ω	0.02		%
V_{NO}	Output noise voltage	1kHz, A-weighted	25		μV

TYPICAL PERFORMANCE CHARACTERISTICS

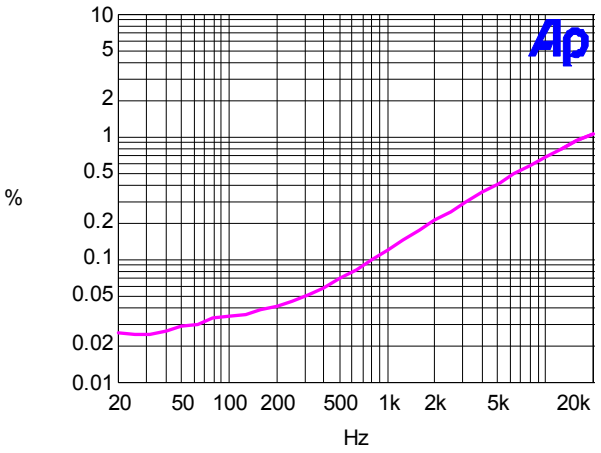


Figure 2 THD+N vs. Frequency VDD=3V, RL=4ohm, BTL, PO=350mW, Avd=2, BW=80kHz

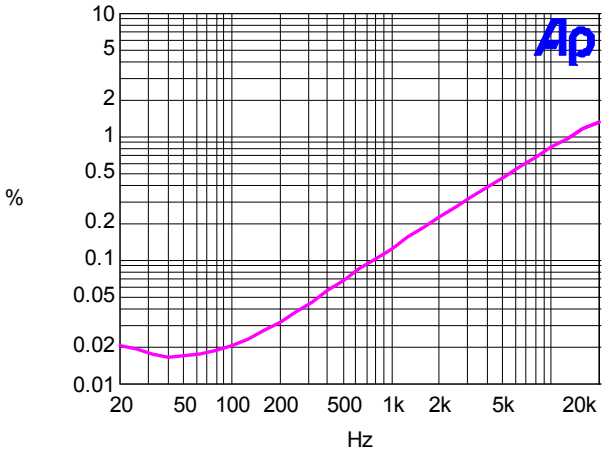


Figure 3 THD+N vs. Frequency VDD=5V, RL=4ohm, BTL, PO=500mW, Avd=2, BW=80kHz

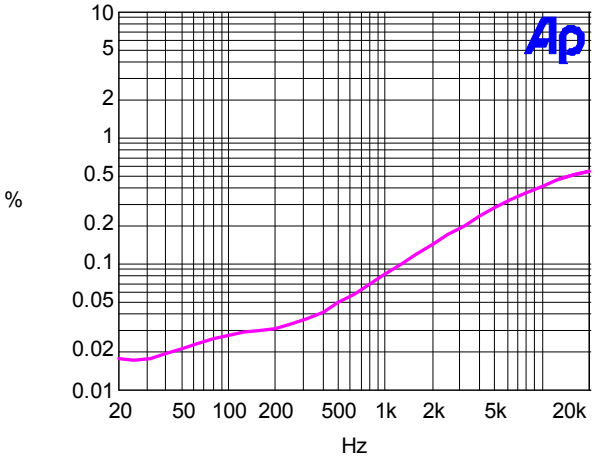


Figure 4 THD+N vs. Frequency VDD=3V, RL=8ohm, BTL, PO=150mW, Avd=2, BW=80kHz

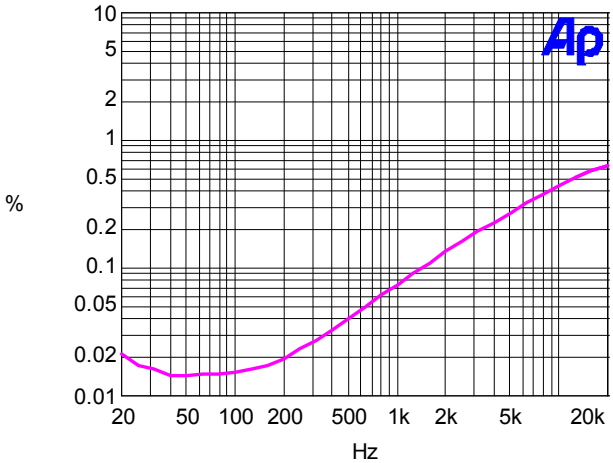


Figure 5 THD+N vs. Frequency VDD=5V, RL=8ohm, BTL, PO=200mW, Avd=2, BW=80kHz

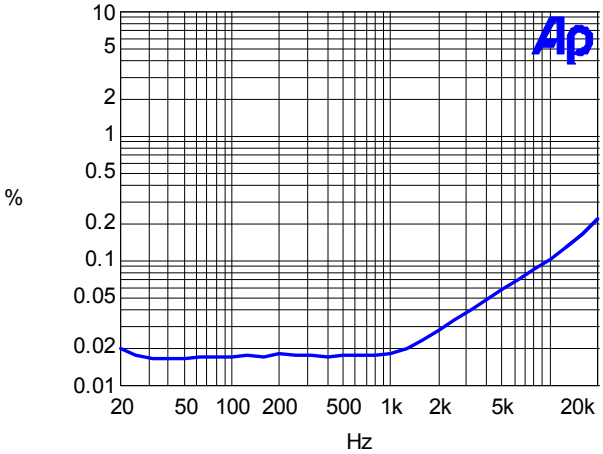


Figure 6 THD+N vs. Frequency VDD=3V, RL=32ohm, SE, PO=25mW, Avd=2, BW=80kHz

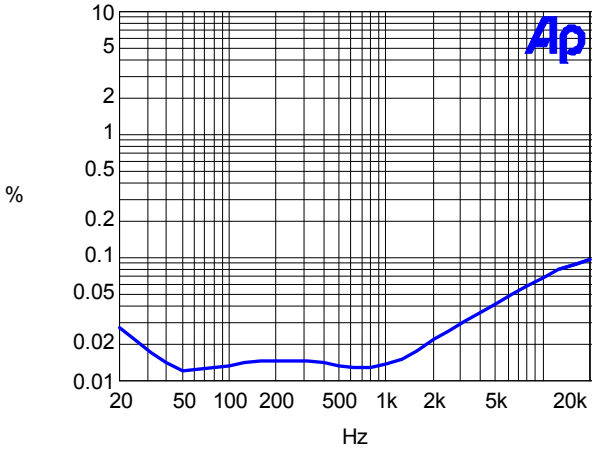


Figure 7 THD+N vs. Frequency VDD=5V, RL=32ohm, SE, PO=75mW, Avd=2, BW=80kHz

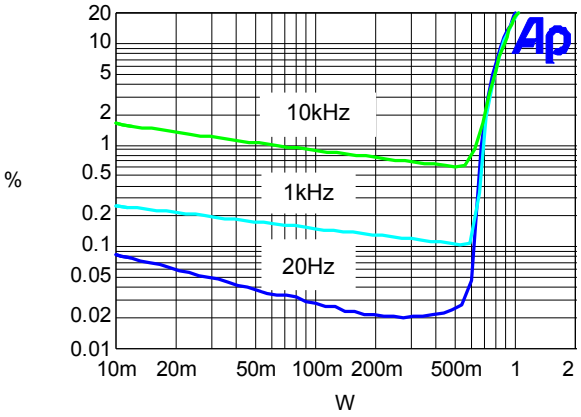


Figure 8 THD+N vs. Output Power VDD=3V, RL=4ohm, BTL, Avd=2, BW=80kHz

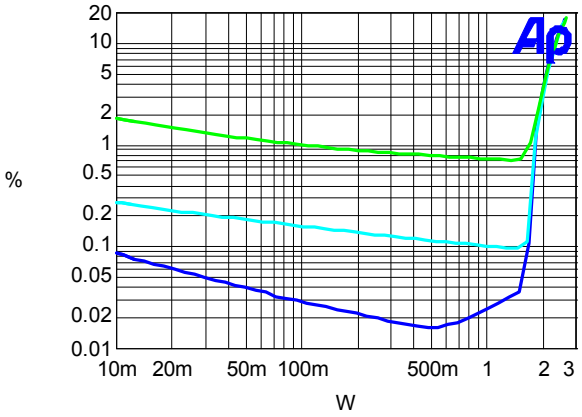


Figure 9 THD+N vs. Output Power VDD=5V, RL=4ohm, BTL, Avd=2, BW=80kHz

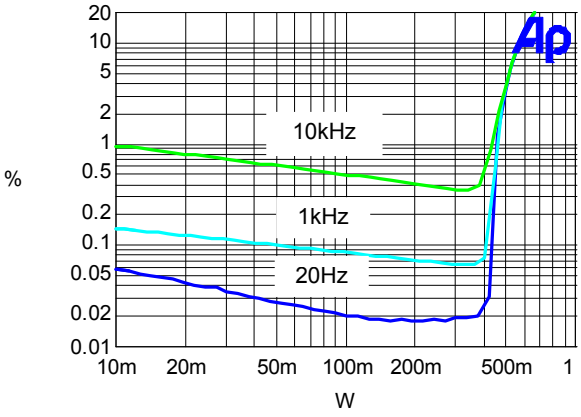


Figure 10 THD+N vs. Output Power VDD=3V, RL=8ohm, BTL, Avd=2, BW=80kHz

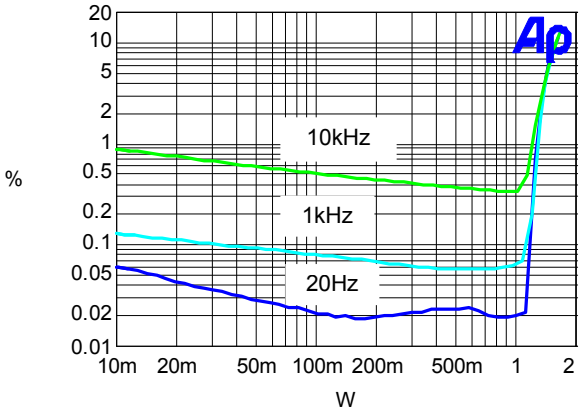


Figure 11 THD+N vs. Output Power VDD=5V, RL=8ohm, BTL, Avd=2, BW=80kHz

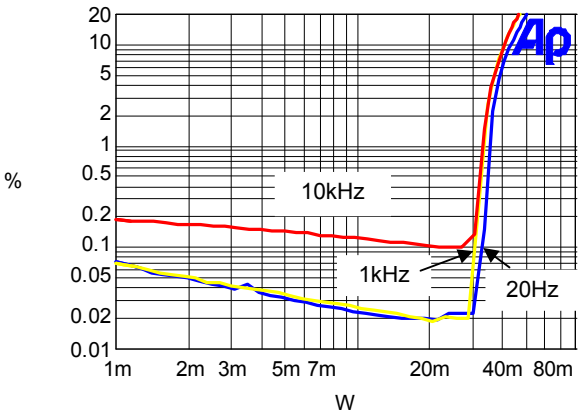


Figure 12 THD+N vs. Output Power VDD=3V, RL=32ohm, SE, Avd=2, BW=80kHz

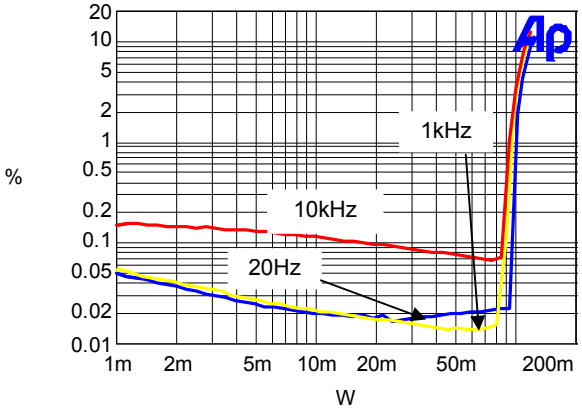


Figure 13 THD+N vs. Output Power VDD=5V, RL=32ohm, SE, Avd=2, BW=80kHz

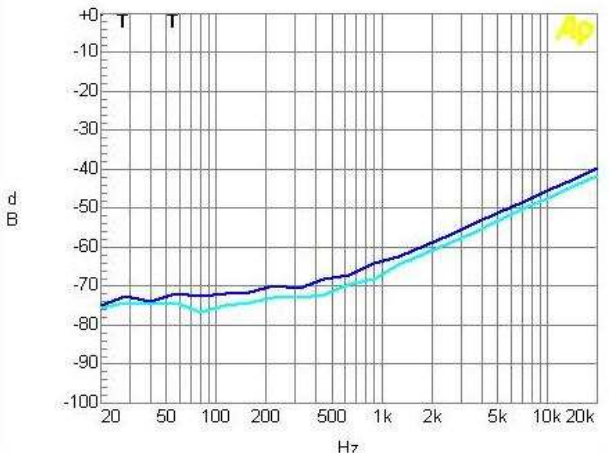


Figure 14 PSRR vs. Frequency VDD=3V, RL=8ohm, BTL, Input AC-grounded

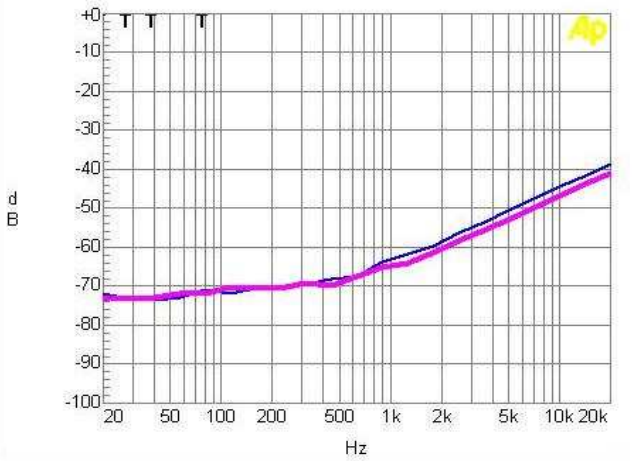


Figure 15 PSRR vs. Frequency VDD=5V, RL=8ohm, BTL, Input AC-grounded

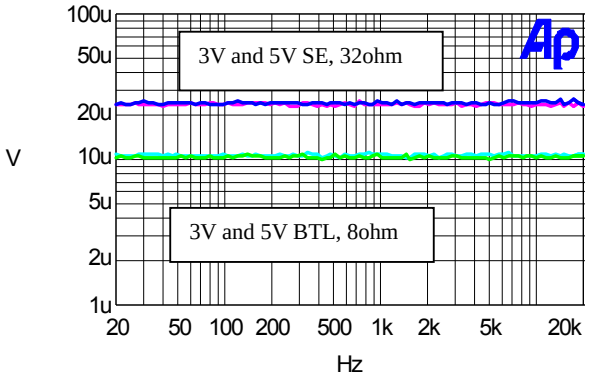


Figure 16 Noise Floor A-Weighted

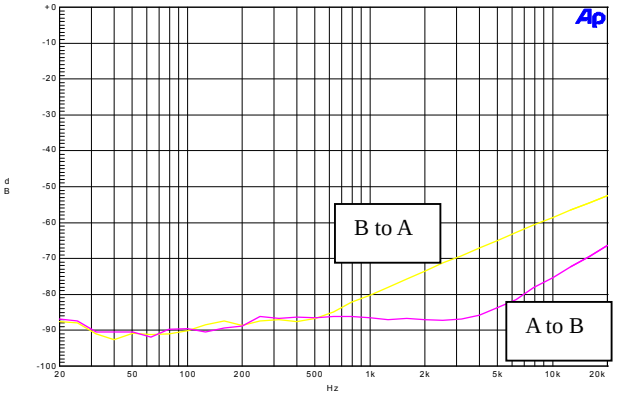


Figure 17 Crosstalk VDD=5V, RL=8ohm, BTL

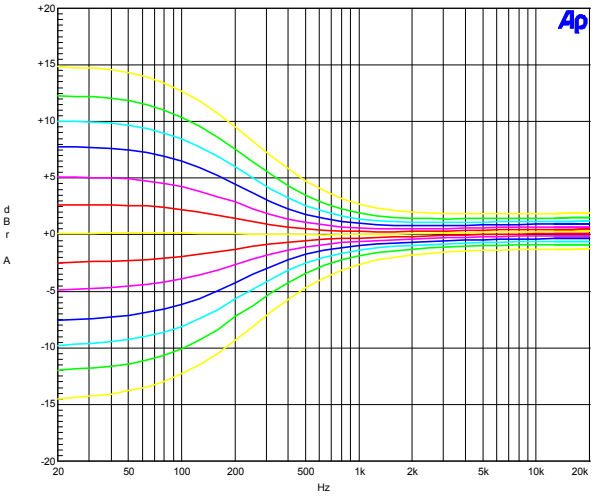


Figure 18 Base Response vs. Frequency VDD=5V, RL=8ohm, BTL

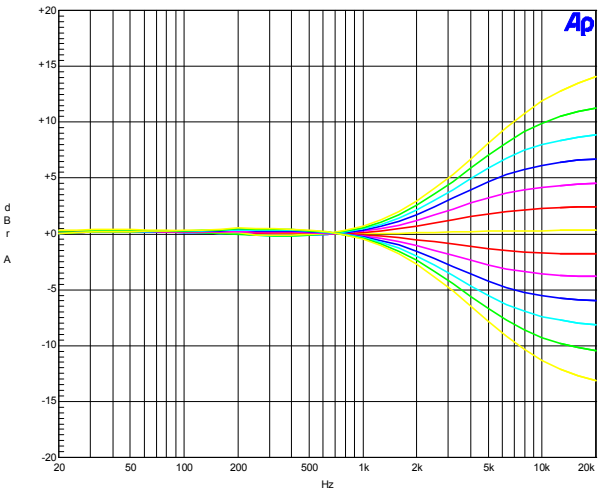


Figure 19 Treble Response vs. Frequency VDD=5V, RL=8ohm, BTL

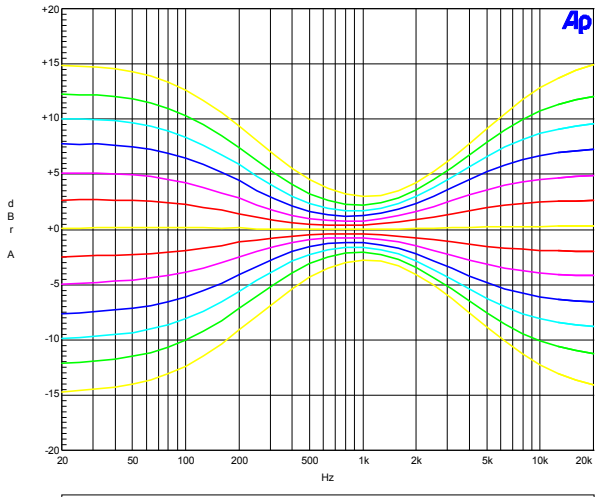


Figure 20 Bass and Treble Response vs. Frequency VDD=5V, RL=8ohm, BTL

TIMING DIAGRAMS

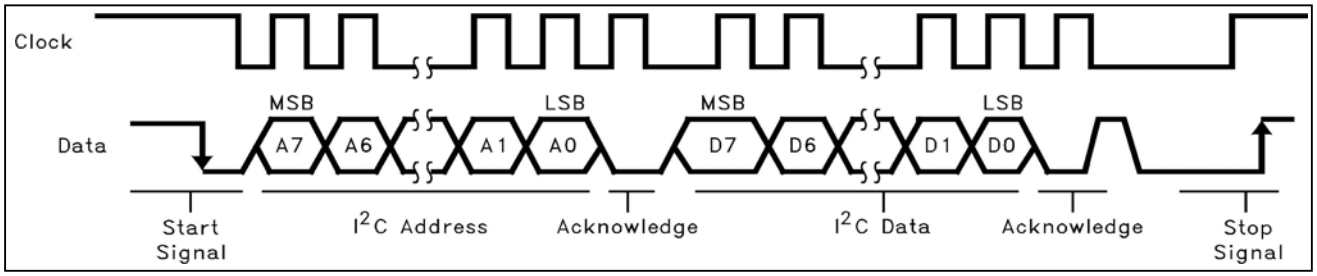


Figure 21 I2C Bus Format

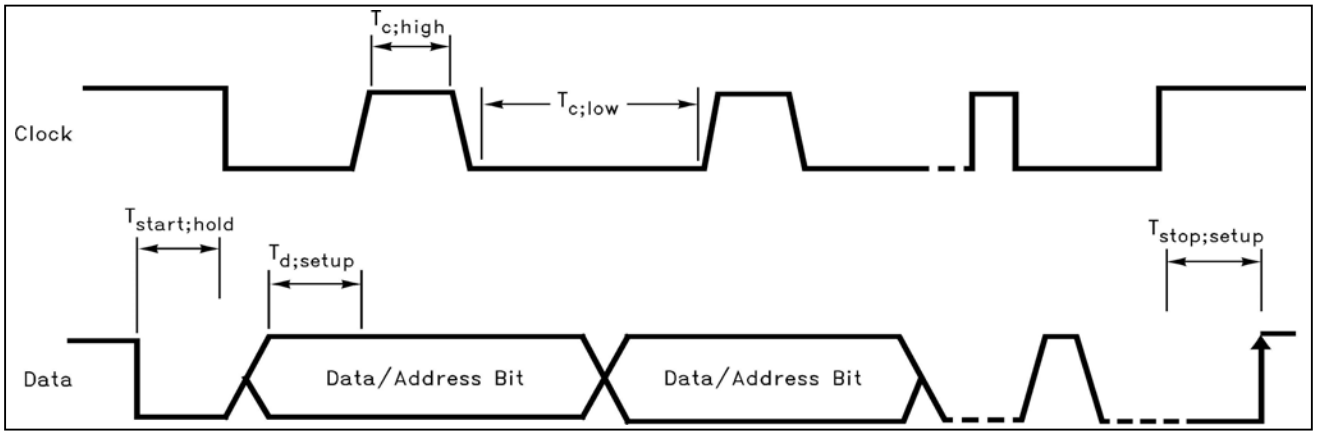


Figure 22 I2C Timing Diagram

See Electrical Characteristics section for timing specifications

TRUTH TABLES

SOFTWARE SPECIFICATION

Chip Address

MSB							LSB
1	0	0	0	0	0	0	0

Data Bytes (Brief Description)

MSB							LSB	Function
0	0	1	X	D3	D2	D1	D0	Bass Control
0	1	0	X	D3	D2	D1	D0	Treble Control
1	1	1	X	D3	D2	D1	D0	General Control

Bass Control

MSB							LSB	Level (dB)
0	0	1	X	0	0	0	0	−12
0	0	1	X	0	0	0	1	−10
0	0	1	X	0	0	1	0	−8
0	0	1	X	0	0	1	1	−6
0	0	1	X	0	1	0	0	−4
0	0	1	X	0	1	0	1	−2
0	0	1	X	0	1	1	0	0
0	0	1	X	0	1	1	1	2
0	0	1	X	1	0	0	0	4
0	0	1	X	1	0	0	1	6
0	0	1	X	1	0	1	0	8
0	0	1	X	1	0	1	1	10
0	0	1	X	1	1	0	0	12
Bass Control Power Up State			X	0	1	1	0	Bass Control is Flat

Treble Control

MSB							LSB	Level (dB)
0	1	0	X	0	0	0	0	−12
0	1	0	X	0	0	0	1	−10
0	1	0	X	0	0	1	0	−8
0	1	0	X	0	0	1	1	−6
0	1	0	X	0	1	0	0	−4
0	1	0	X	0	1	0	1	−2
0	1	0	X	0	1	1	0	0
0	1	0	X	0	1	1	1	2
0	1	0	X	1	0	0	0	4
0	1	0	X	1	0	0	1	6
0	1	0	X	1	0	1	0	8
0	1	0	X	1	0	1	1	10
0	1	0	X	1	1	0	0	12
Treble Control Power Up State			X	0	1	1	0	Treble Control is Flat

General Control

MSB							LSB	Function
1	1	1					0	Chip On
1	1	1					1	Chip Shutdown
1	1	1				0		Speaker Enable
1	1	1				1		Speaker Disable
1	1	1			0			Stereo Enhance Off
1	1	1			1			Stereo Enhance On
1	1	1	0					Mute Disable
1	1	1	1					Mute Enable
General Control Power Up State			0	0	0	0	0	

APPLICATION INFORMATION

LAYOUT

As stated in the Grounding section, placement of ground return lines is critical for maintaining the highest level of system performance. It is not only important to route the correct ground return lines together, but also important to be aware of where those ground return lines are routed in conjunction with each other. The output load ground returns should be physically located as far as reasonably possible from low signal level lines and their ground return lines. Critical signal lines are those relating to the microphone amplifier section, since these lines generally work at very low signal levels.

SUPPLY BYPASSING

As with all op amps and power op amps, the IS31AP4832 requires the supplies to be bypassed to avoid oscillation. To avoid high frequency instabilities, a 0.1µF metallized-film or ceramic capacitor should be used to bypass the supplies as close to the chip as possible. For low frequency considerations, a 10µF or greater tantalum or electrolytic capacitor should be paralleled with the high frequency bypass capacitor.

If power supply bypass capacitors are not sufficiently large, the current in the power supply leads, which is a rectified version of the output current, may be fed back into internal circuitry. This internal feedback signal can cause high frequency distortion and oscillation.

If power supply lines to the chip are long, larger bypass capacitors could be required. Long power supply leads have inductance and resistance associated with them that could prevent peak low frequency current demands from being met. The extra bypass capacitance will reduce the peak current requirements from the power supply lines.

POWER-UP STATUS

On power-up or after a hard reset, the IS31AP4832 registers will be initialized with the default values listed in the truth tables. By default, the tone controls are all flat, 3D Enhance is off, and the chip is in stereo mode.

CLICK-AND-POP CIRCUITRY

The IS31AP4832 contains circuitry to minimize turn-on transients or “click and pops”. In this case, turn-on refers to either power supply turn-on or the device coming out of shutdown mode. When the devices turn on, the amplifiers are internally configured as unity gain buffers. An internal current source charges the bypass capacitor on the bypass pin. Both the inputs and outputs ideally track the voltage at the bypass pin. The device will remain in buffer mode until the bypass pin has reached its half supply voltage, $1/2V_{DD}$. As soon as the bypass node is stable, the device will become fully operational.

Although the bypass pin current source cannot be modified, the size of the bypass capacitor, CB, can be changed to alter the device turn-on time and the amount of “click and pop”. By increasing CB, the amount of turn-on pop can be reduced. However, the trade-off for using a larger bypass capacitor is an increase in the turn-on time for the device. Reducing CB will decrease turn-on time and increase “click and pop”.

There is a linear relationship between the size of CB and the turn-on time. Some typical turn-on times for different values of CB are:

C_b	T_{ON}
0.1µF	50ms
1µF	130ms

In order to eliminate “click and pop”, all capacitors must be discharged before turn-on. Rapid on/off switching of the device or shutdown function may cause the “click and pop” circuitry to not operate fully, resulting in increased “click and pop” noise.

COUPLING CAPACITORS

Because the IS31AP4832 is a single supply circuit, all audio signals must be capacitor coupled to the chip to remove the 2.5 V_{DC} bias. All audio inputs have 20kΩ input impedances, so the AC-coupling capacitor will create a high-pass filter with

$$f_{-3dB} = 1/(2\pi \times 20k\Omega \times C_{IN})$$

POWER AMPLIFIER

The power amplifiers in the IS31AP4832 are designed to drive 8Ω or 32Ω loads at 1.2W (continuous) and 90mW (continuous), respectively, with 1% THD+N. As shown in the Typical Performance Characteristics, the power amplifiers typically drive 4Ω loads at 350mW, but with a slight increase in high-frequency THD. As discussed above, these outputs should be AC-coupled to the output load.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the IS31AP4832 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. External feedback resistors Rf and input resistors Ri set the closed-loop gain of Amp A (NOUTA) and Amp B (NOUTA) whereas two internal 20kΩ resistors set Amp A’s (POUTA) and Amp B’s (POUTA) gain at 1. The IS31AP4832 drives a load, such speaker, connected between the two amplifier outputs, NOUTA and POUTA.

Figure 1 shows that Amp A’s (NOUTA) output serves as Amp A’s (POUTA) input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between NOUTA and

POUTA and driven differentially (commonly referred to as “bridge mode”). This results in a differential gain of

$$A_{VD} = 2\times(Rf/Ri) \qquad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier’s output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A’s and channel B’s outputs at half-supply. This eliminates the coupling capacitor that single supply, single ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier’s half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

I2C INTERFACE

The IS31AP4832 uses a serial bus, which conforms to the I^2C protocol, to control the chip’s functions with two wires: clock and data. The clock line is uni-directional. The data line is bi-directional (open-collector) with a pull-up resistor (typically 10kΩ).The maximum clock frequency specified by the I^2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31AP4832.

The timing diagram for the I^2C is shown in Figure *22*. The data is latched in on the stable high level of the clock and the data line should be held high when not in use. The timing diagram is broken up into six major sections:

The “start” signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I^2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the clock level is high.

After the last bit of the address is sent, the master checks for the IS31AP4832’s acknowledge. The master releases the data line high (through a pull-up resistor). Then the master sends a clock pulse. If the IS31AP4832 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not low, then the master should send a “stop” signal (discussed later) and abort the transfer.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must generate another acknowledge seeing if the IS31AP4832 received the data.

If the master has more data bytes to send to the IS31AP4832, then the master can repeat the previous two steps until all data bytes have been sent.

The “stop” signal ends the transfer. To signal “stop”, the data signal goes high while the clock signal is high.

3D AUDIO ENHANCEMENT

The IS31AP4832 has a 3D audio enhancement effect that helps improve the apparent stereo channel separation when, because of cabinet or equipment limitations, the left and right speakers are closer to each other than optimal.

An external RC network is required to enable the effect. The amount of the effect is set by the 5kΩ resistor. A 220nF capacitor is used to reduce the effect at frequencies below 140Hz. Increasing the value of the capacitor will decrease the low cutoff frequency at which the Stereo Enhanced effect starts to occur as shown below

$$F_{(-3dB)} = 1/2\pi\ R_{3D}\times C_{3D}$$

Decreasing the resistor size will make the 3D effect more pronounced and decreasing the capacitor size will raise the cutoff frequency for the effect.

TONE CONTROL RESPONSE

Bass and treble tone controls are included in the IS31AP4832. The tone controls use two external capacitors for each stereo channel. Each has a corner frequency determined by the value of C1 (connected between loop out and tone in) and C2 (connected between tone out and loop in) and internal resistors in the feedback loop of the internal tone amplifier.

Typically, C1 = C2 and for 100 Hz and 10kHz corner frequencies, C1 = C2 = 2.2nF. Altering the ratio between C1 and C2, changes the midrange gain. For example, if C1 = 2(C2), then the frequency response will be flat at 20Hz and 20kHz, but will have a 6dB peak at 1kHz.

With C = C1 = C2, the treble turn-over frequency is nominally

$$f_{TT} = 1/(2\pi C(56k\Omega))$$

and the bass turn-over frequency is nominally

$$f_{BT} = 1/(2\pi C(113.3k\Omega)),$$

when maximum boost is chosen. The inflection points (the frequencies where the boost or cut is within 3dB of the final value) are, for treble and bass respectively,

$$f_{TI} = 1/(2\pi C(7.1k\Omega))$$

$$f_{BI} = 1/(2\pi C(631.7k\Omega))$$

Increasing the values of C1 and C2 decreases the

turnover and inflection frequencies: i.e., the Tone Control Response Curves shown in Typical Performance Section will shift left when C1 and C2 are increased and shift right when C1 and C2 are decreased. With C1 = C2 = 0.0022μF, 2dB steps are achieved at 100Hz and 10kHz. Changing C1 and C2 to 0.001μF shifts the 2dB step frequency to 220Hz and 25kHz. If the tone control capacitors' size is decreased these frequencies will increase. With C1 = C2 = 0.0033μF the 2dB steps take place at 68Hz and 7.6kHz.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

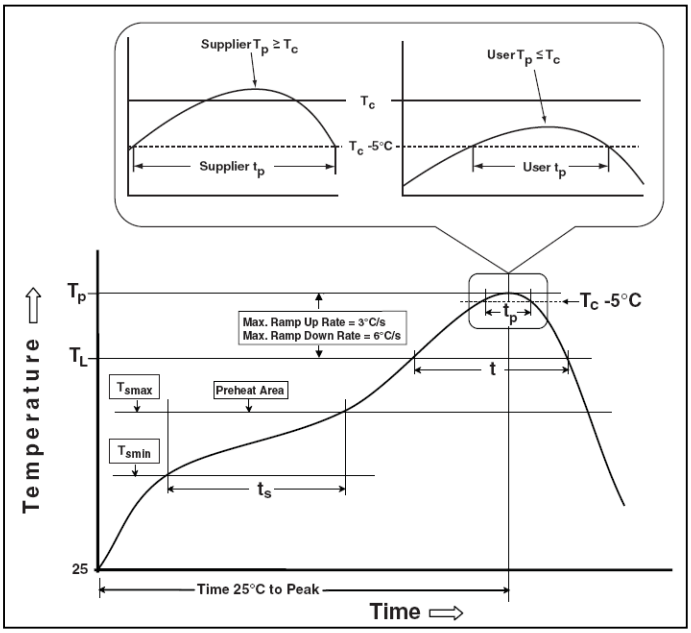
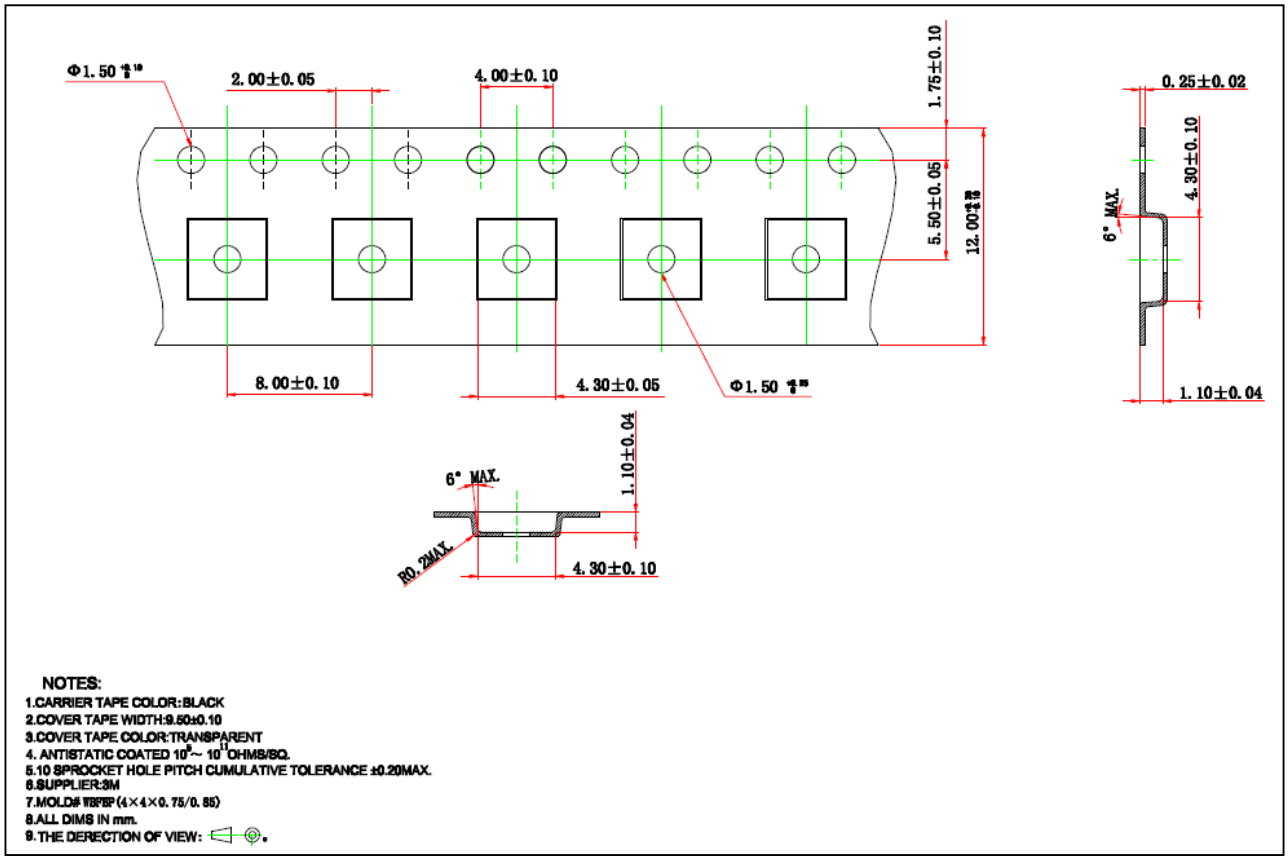


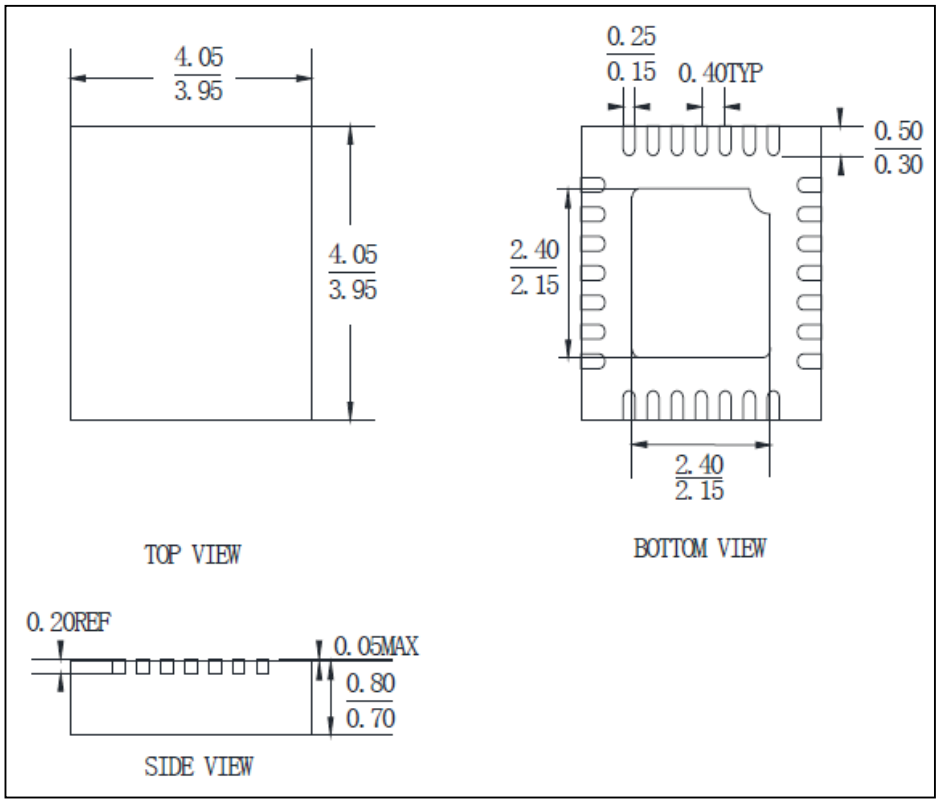
Figure 23 Classification Profile

TAPE AND REEL INFORMATION



PACKAGE INFORMATION

QFN-28



Note: All dimensions in millimeters unless otherwise stated.