IS62C5128BL, IS65C5128BL

512K x 8 HIGH-SPEED CMOS STATIC RAM

JULY 2011

FEATURES

- High-speed access time: 45ns
- Low Active Power: 50 mW (typical)
- Low Standby Power: 10 µW (typical) CMOS standby
- TTL compatible interface levels
- Single 5V ± 10% power supply
- Fully static operation: no clock or refresh required
- Available in 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

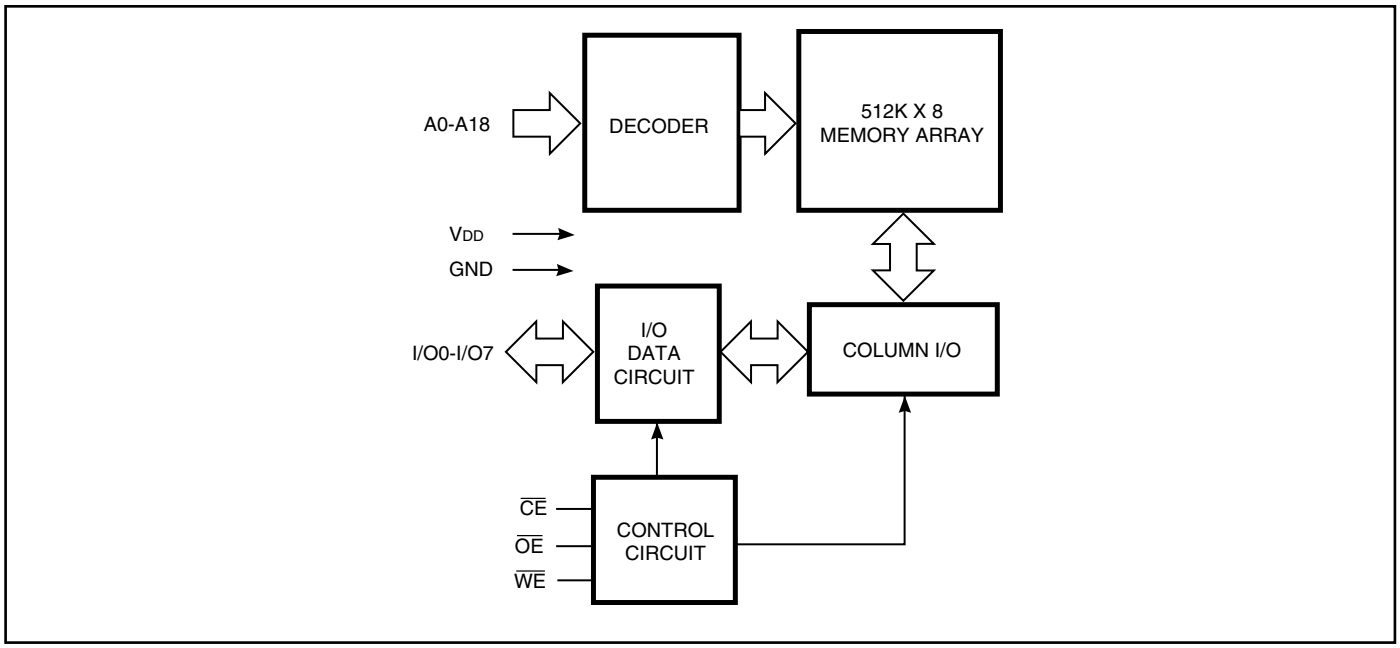
The *ISSI* IS62C5128BL and IS65C5128BL are high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 45ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

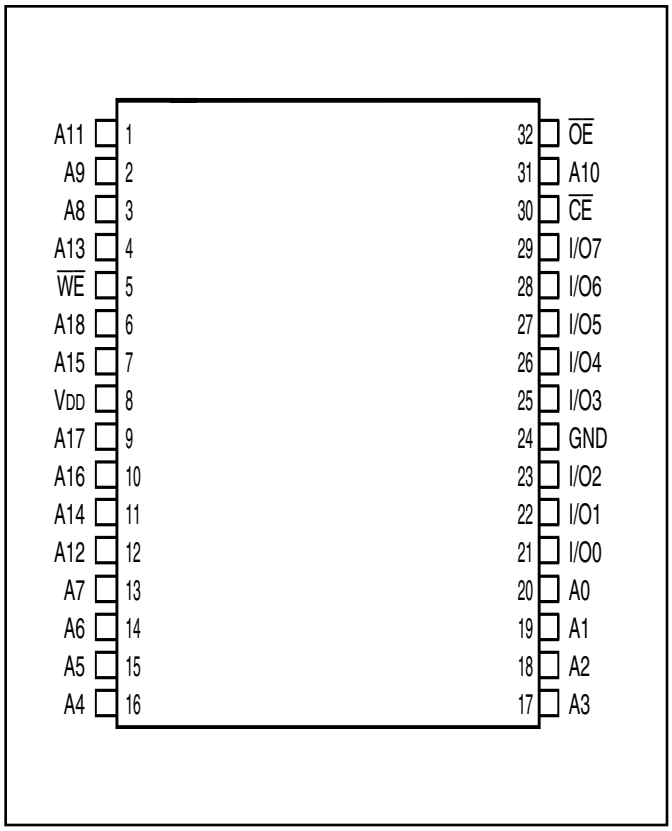
The IS62C5128BL and IS65C5128BL are packaged in the JEDEC standard 32-pin sTSOP-I, 32-pin SOP and 32-pin TSOP-II packages

FUNCTIONAL BLOCK DIAGRAM

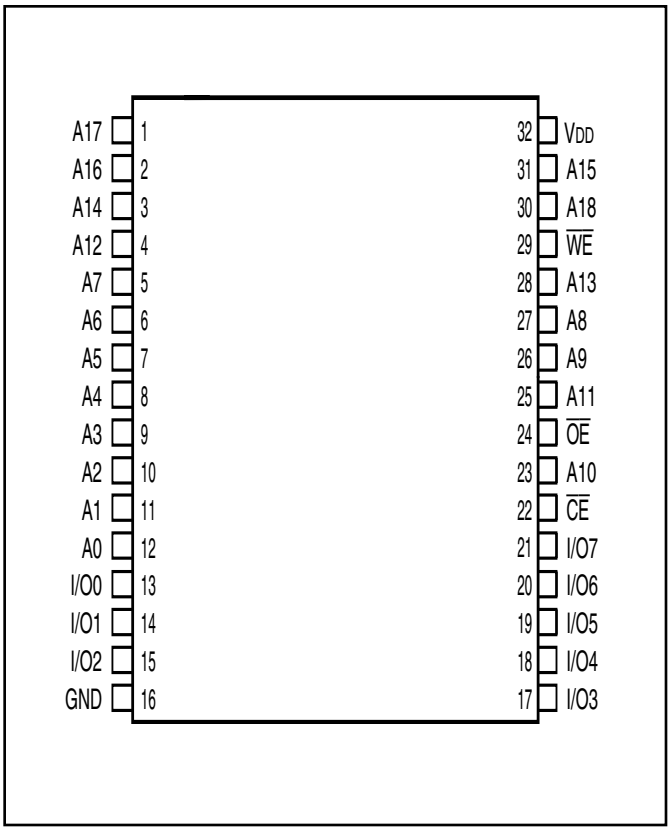


PIN CONFIGURATION

32-pin sTSOP (TYPE I)



32-pin SOP
32-pin TSOP (TYPE II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
$\overline{CE}$	Chip Enable 1 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O0-I/O7	I/O PIN V_{DD} Current
Not Selected	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2.1 mA		—	0.4	V
V_{IH}	Input HIGH Voltage[1]			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
			Auto.	–5	5	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}	Com.	–1	1	µA
		Outputs Disabled	Ind.	–2	2	
			Auto.	–5	5	

Note:
1. V_{ILL} (min) = -2.0V AC (pulse width <10 ns). Not 100% tested.
   V_{IHH} (max) = V_{DD} + 2.0V AC (pulse width <10 ns). Not 100% tested.

OPERATING RANGE

Range	Ambient Temperature	V_{DD}	Speed (ns)
Commercial	0°C to +70°C	5V ± 10%	45
Industrial	-40°C to +85°C	5V ± 10%	45
Automotive	-40°C to +125°C	5V ± 10%	45

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-45 ns Min.	-45 ns Max.	Unit
I_{CC}	Average operating Current	$\overline{CE}$ = V_{IL}, V_{DD} = Max. I_{OUT}= 0 mA, f= 0	Com. Ind. Auto.	— — —	10 10 10	mA
I_{CC1}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind. Auto. typ.[2]	— — — 	15 20 25 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ ≥ V_{IH}, f = 0	Com. Ind. Auto.	— — —	1 1.5 2	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE}$ ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ V_{SS} + 0.2V, f = 0	Com. Ind. Auto. typ.	— — — 	10 15 35 4	µA

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-45		
Symbol	Parameter	Min.	Max.	Unit
t_{RC}	Read Cycle Time	45	—	ns
t_{AA}	Address Access Time	—	45	ns
t_{OHA}	Output Hold Time	3	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	45	ns
t_{DOE}	$\overline{OE}$ Access Time	—	20	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	15	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	0	15	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	5	—	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

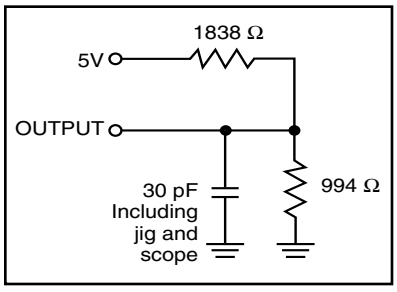


Figure 1

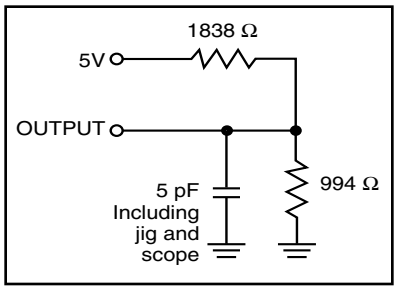
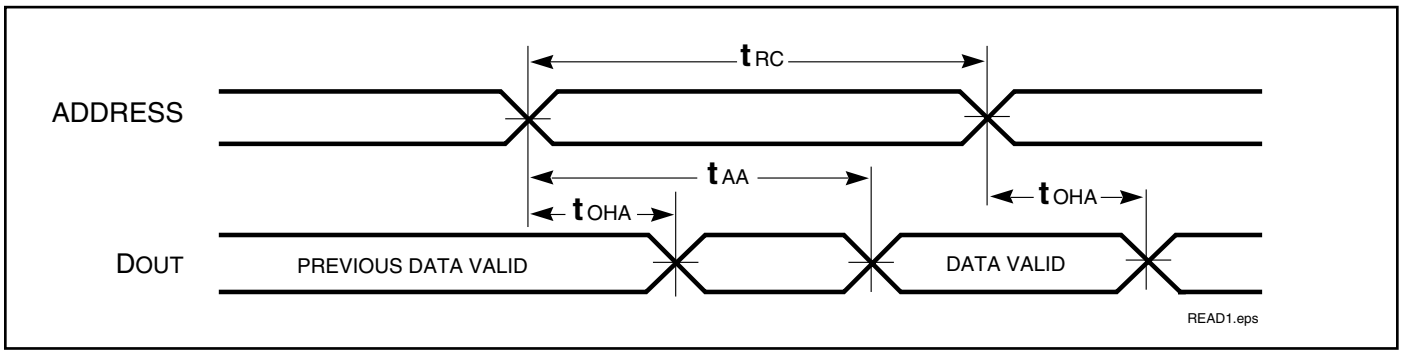


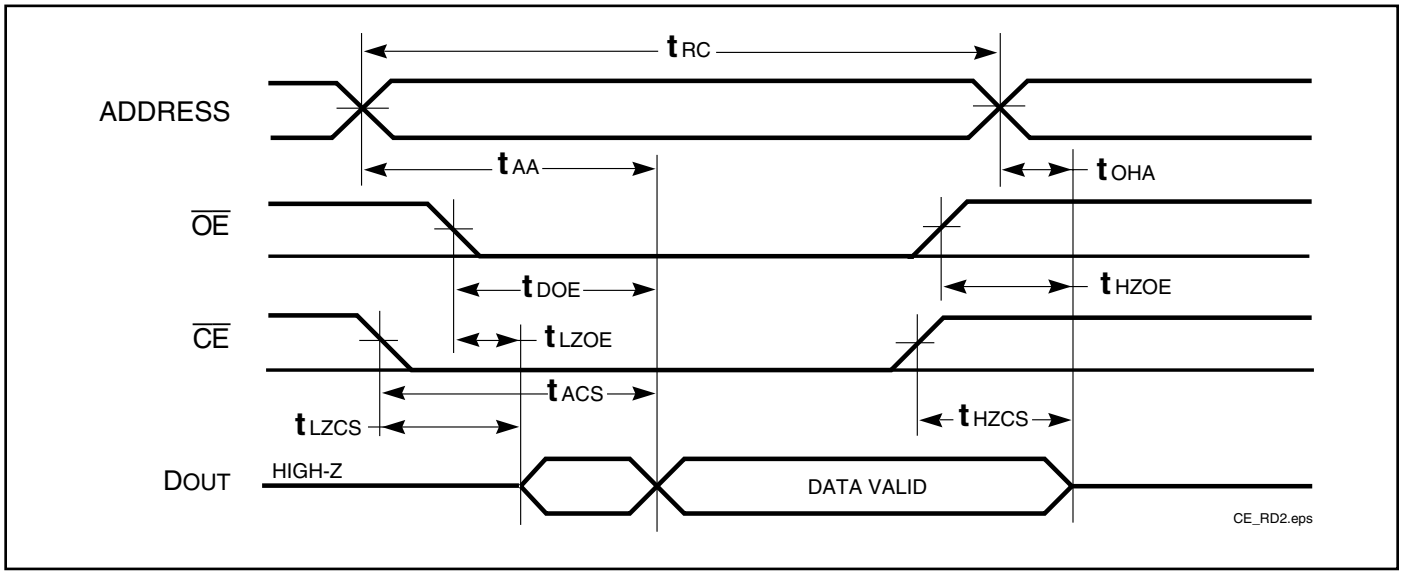
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



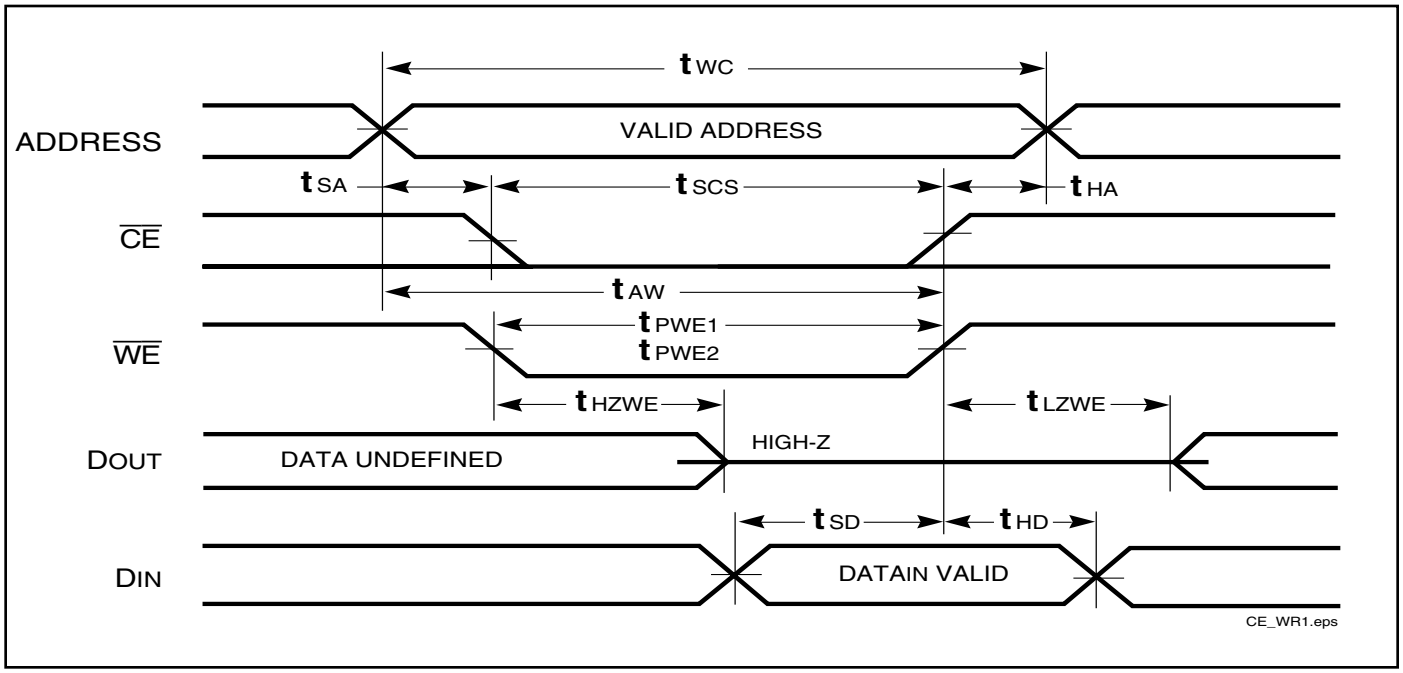
Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

Symbol	Parameter	-45 Min.	-45 Max.	Unit
t_{WC}	Write Cycle Time	45	—	ns
t_{SCE}	$\overline{CE}$ to Write End	35	—	ns
t_{AW}	Address Setup Time to Write End	35	—	ns
t_{HA}	Address Hold from Write End	0	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ =High)	35	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$=Low)	35	—	ns
t_{SD}	Data Setup to Write End	25	—	ns
t_{HD}	Data Hold from Write End	0	—	ns
t_{HZWE}[2]	$\overline{WE}$ LOW to High-Z Output	—	15	ns
t_{LZWE}[2]	$\overline{WE}$ HIGH to Low-Z Output	5	—	ns

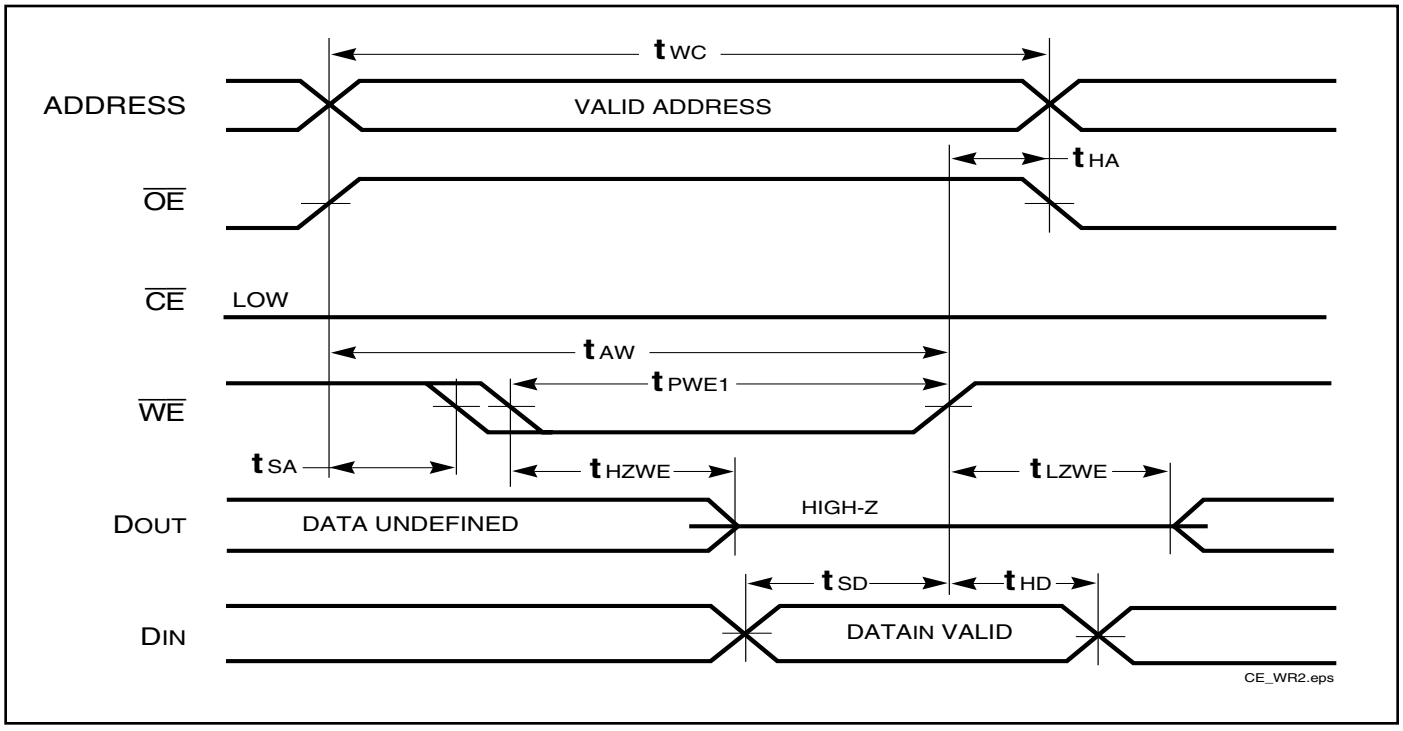
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS
WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)[1,2]

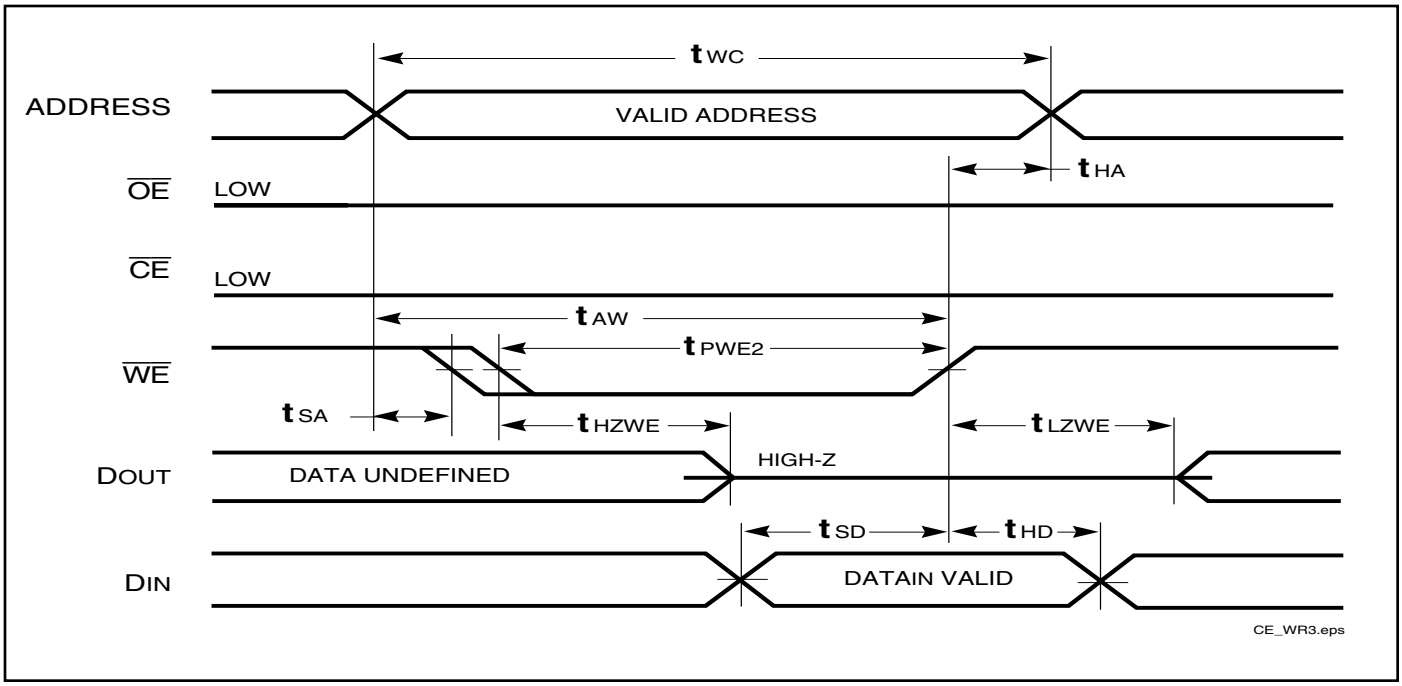


Notes:
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) [1,2]



WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.

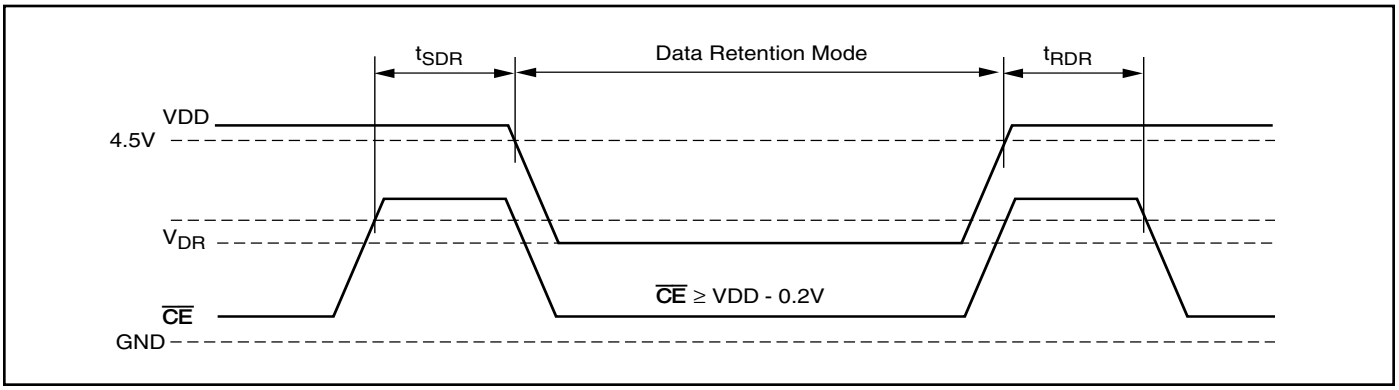
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	5.5	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	10	µA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	15	
			Auto.	—	35	
			typ. (1)	2		
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}	—	ns

Note:

1. Typical Values are measured at V_{DD} = 5V, T_A = 25°C and not 100% tested.

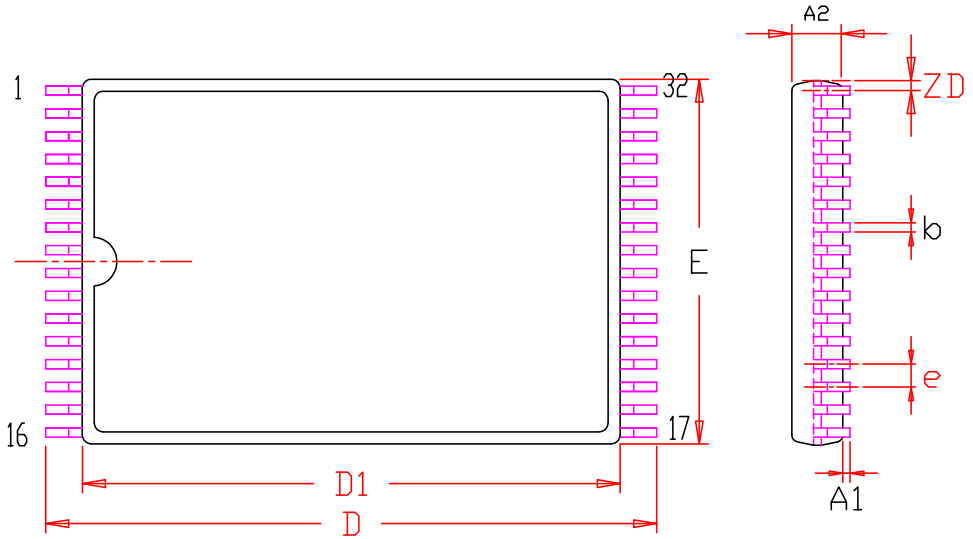
DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)

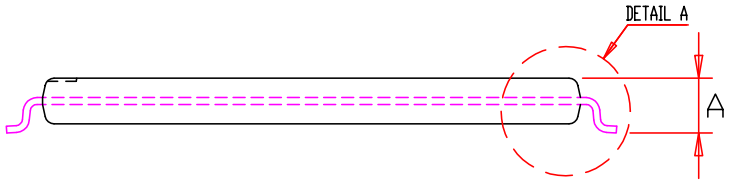


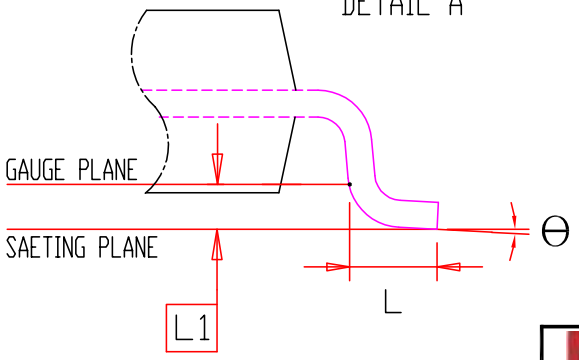
ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62C5128BL-45QI	450-mil Plastic SOP
	IS62C5128BL-45QLI	450-mil Plastic SOP, Lead-free
	IS62C5128BL-45HI	32-pin STSOP-I
	IS62C5128BL-45HLI	32-pin STSOP-I, Lead-free
	IS62C5128BL-45TI	32-pin TSOP-II
	IS62C5128BL-45TLI	32-pin TSOP-II, Lead-free





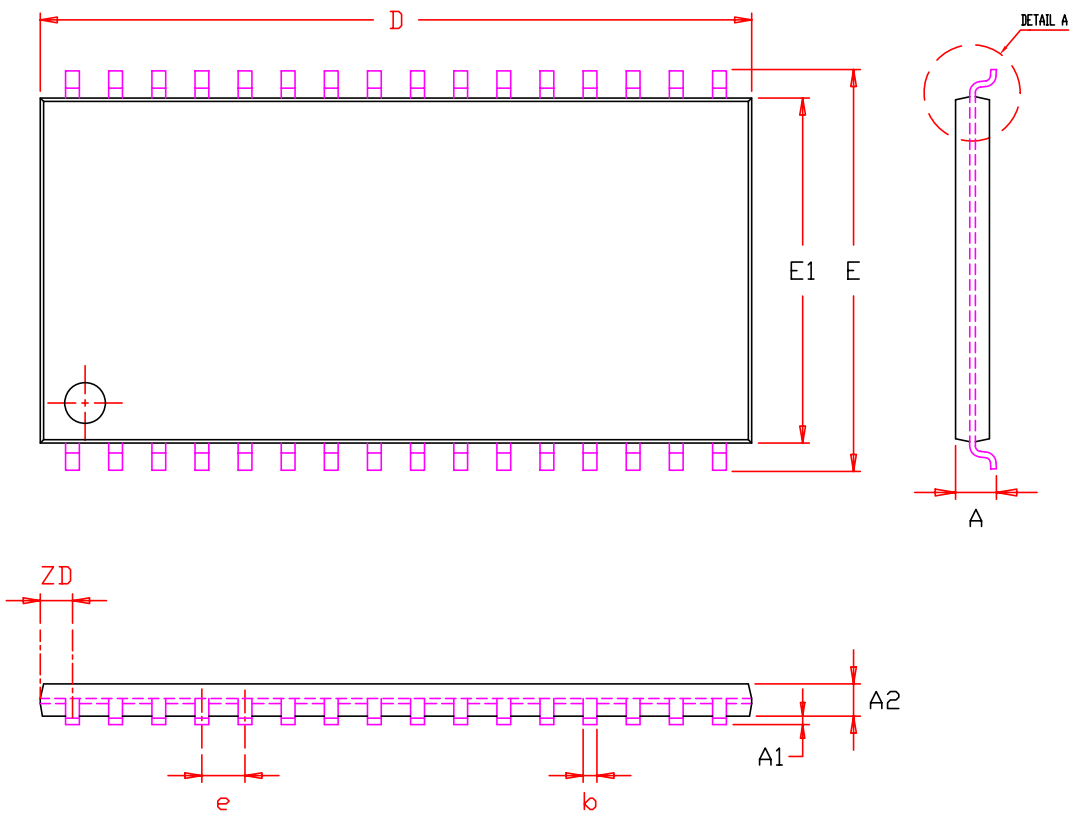


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

	TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	E	DATE	04/24/2009

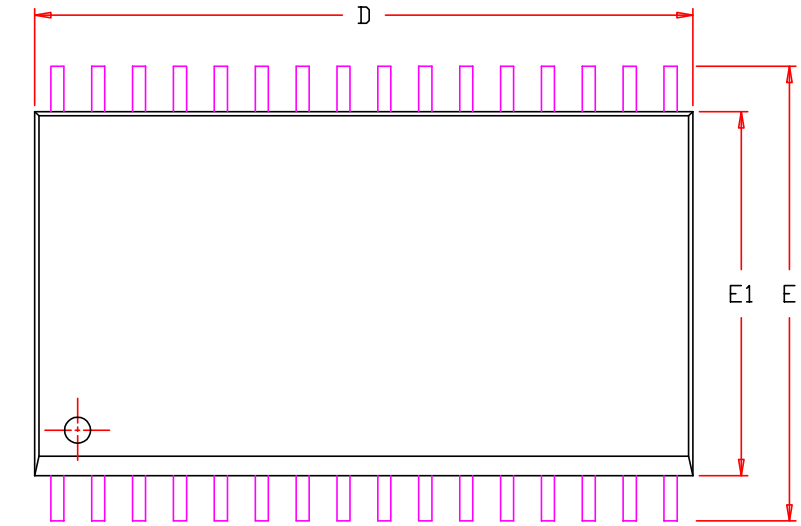


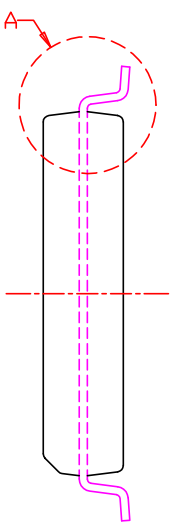
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.52	0.012		0.020
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	1.27 BSC.			0.050 BSC.		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BSC.			0.010 BSC.		
ZD	0.95 REF.			0.037 REF.		
θ	0		8°	0		8°

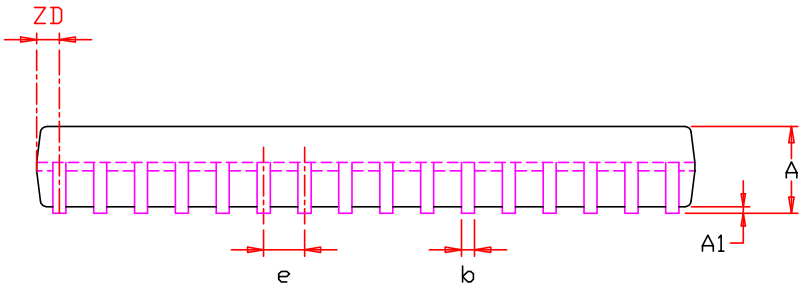
NOTE :

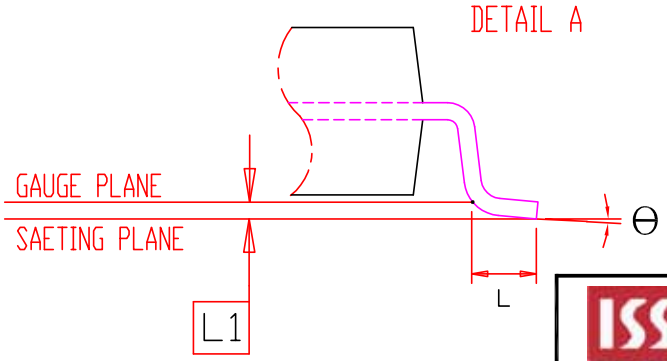
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	32L 400mil TSOP-2 Package Outline	REV.	E	DATE	06/23/2009









SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.62	—	3.12	0.103	—	0.123
A1	0.05	—	0.30	0.002	—	0.012
b	0.33	—	0.51	0.013	—	0.020
D	20.24	—	20.75	0.797	—	0.817
E	13.79	—	14.45	0.543	—	0.569
E1	11.18	—	11.43	0.440	—	0.450
e	1.27 BSC.			0.050 BSC.		
L	0.38	—	1.27	0.015	—	0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.725 REF.			0.029 REF.		
θ	0	—	8°	0	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

	TITLE	32L 450mil SOP Package Outline	REV.	D	DATE	04/20/2009