Semicustom Products

UT90nHBD Hardened-by-Design (HBD) Standard Cell

Advanced Data Sheet
February 2012
www.aeroflex.com/RadHardASIC

FEATURES

- Up to 30,000,000 usable equivalent gates with a 1.0V Core using standard cell architecture
- Toggle rates up to 5.0 GHz
- Advanced 90nm silicon gate CMOS processed in a commercial fab
- Operating voltage 2.5V and 1.8V I/O and 1.0V core
- Radiation hardened from 100 krads(Si) to 1 Mrads(Si) total dose available
- Comprehensive set of core standard cells with multiple V_t options for optimizing speed and power
- Design support for Mentor Graphics®, Synopsys®, in Verilog and VHDL design languages on Sun(TM) and Linux workstations
- Power dissipation of 0.2nW/MHz/gate at V_{DDCORE} 1.0V and 20% duty cycle
- External chip capacitor attachment option available to space quality levels (for improved SSO response)

PRODUCT DESCRIPTION

The high-performance UT90nHBD Hardened-by-Design ASIC standard cell family features densities up to 30,000,000 equivalent NAND2 gates.

The deep submicron ASIC family uses a highly efficient standard cell architecture for the internal cell instantiation. Combined with state-of-the-art placement and routing tools, the area utilization and signal interconnect of transistors is maximized using eight levels of copper metal interconnect.

Extensive Cell Library

The UT90nHBD standard cell family is supported by an extensive cell library over 900 elements. User selectable options for cell configurations include scan for all register elements, as well as output drive strengths (1x to 30x) and transistor threshold voltages (LV_t, RV_t). Refer to Aeroflex's UT90nHBD Design Manual for complete cell listing and details.

- Aeroflex Gaisler

We offer Aeroflex Gaisler LEON3 and other IP which can be reviewed at www.gaisler.com/CMS

I/O Buffers

The UT90nHBD standard cell family offers extensive I/O cell options. The I/O library contains 36 different general purpose CMOS functional I/O pads, power and ground pads.

Other I/O buffer features and options include:

- Basic Input or Output
- 9mA and 18mA drive strength
- Slew rate control
- Bi-directional
- Schmitt Trigger
- Tri-State
- Open Drain
- SSTL 1.8V/2.5V

Macro Cells

The UT90nHBD library offering includes a macro cell library that enables system-on-a-chip (SOC) design. The following macros are currently available, with more to come:

- Clock Generator PLL
- SerDes 10GBPS

Embedded SRAM

Aeroflex offers a comprehensive set of compiled embedded memories to meet your ASIC architectural needs. Some features include:

- Single and Dual Port SRAM
- Single and Two Port Register File
- Operating frequency 400MHz and higher
- Optional EDAC RTL generation: 1 or 2 bit detect, 1 bit correct
- Configurable word write mask
- Optional integrated BIST Mux/Collar
- All standard EDA views supported

Clock Driver Distribution

Aeroflex design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

Speed and Performance

Aeroflex specializes in high-performance circuits designed to operate in harsh military and radiation environments. The UT90nHBD library offers cells in both regular Vt and low Vt allowing the user to trade speed for power. The cells can be mixed on the same die providing local solutions for critical paths without sacrificing full chip power consumption. In a radiation environment, additional performance variances must be considered. The UT90nHBD standard cell family simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

Power Dissipation

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. Radiation-tolerant processes exhibit power dissipation that is typical of CMOS processes. For a rigorous power estimating methodology, refer to the Aeroflex UT90nHBD Design Manual or consult with a Aeroflex Applications Engineer.

Typical Power Dissipation

0.2nW/Gate-MHz@1.0V	20% duty cycle

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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A passion for performance.

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