

# PS51259-A

TRANSFER-MOLD TYPE  
INSULATED TYPE

## PS51259-A



### INTEGRATED POWER FUNCTIONS

- Single phase AC input, DC output IGBT/FWD converter bridge
- 600V, 20Arms (Input current)

### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

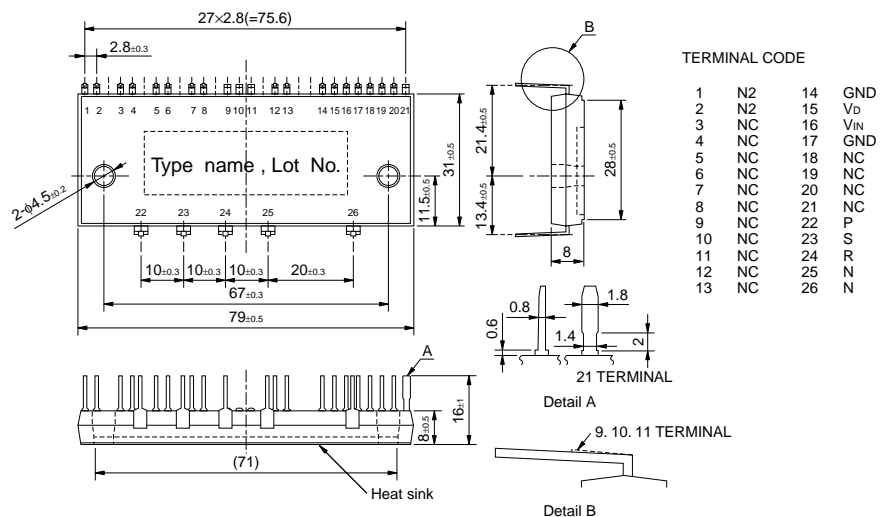
- IGBTs driver circuit
- Control supply under-voltage (UV) protection
- Input interface : 5~15V line CMOS/TTL compatible, Schmitt Trigger receiver circuit (Active high)

## APPLICATION

AC100~200V Active-Converter for PFC (Power Factor Correction), of Air-conditioner and so on.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



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**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

**MAIN CIRCUIT PART**

Symbol	Parameter	Conditions	Ratings	Unit
$V_i$	Supply Voltage	Applied between : S-R	264	$V_{rms}$
$V_{i(surge)}$	Supply Voltage (surge)	Applied between : S-R, Surge value, Non-operating	500	V
$V_o$	Output Voltage	Applied between : P-N	450	V
$V_{o(surge)}$	Output Voltage (surge)	Applied between : P-N, Surge value, Non-operating	500	V
$V_{CES}$	Collector-Emitter Voltage	—	600	V
$V_{RRM}$	Repetitive Peak Reverse Voltage	—	600	V
$I_i$	Input Current (100% Load)	$T_c \leq +90^\circ\text{C}$ , $V_i = 200\text{V}$ , $V_o = 300\text{V}$ , $f_{PWM} = 20\text{kHz}$	20	$A_{rms}$
$I_i(125\%)$	Input Current (125% Load)	$T_c \leq +90^\circ\text{C}$ , $V_i = 200\text{V}$ , $V_o = 300\text{V}$ , $f_{PWM} = 20\text{kHz}$ , 1 min Non-repetitive	25	$A_{rms}$
$I^2t$	$I^2t$ for $F_u$ sing	Value for 1msec of Surge Current	120	$A^2s$
$T_j$	Junction Temperature	(Note 1)	-20~+125	$^\circ\text{C}$

**Note 1 :** The maximum junction temperature rating of the power chips integrated within the DIP-PFC is  $150^\circ\text{C}$  (@  $T_c \leq 100^\circ\text{C}$ ) however, to ensure safe operation of the DIP-PFC, the average junction temperature should be limited to  $T_{j(ave)} \leq 125^\circ\text{C}$  (@  $T_c \leq 100^\circ\text{C}$ ).

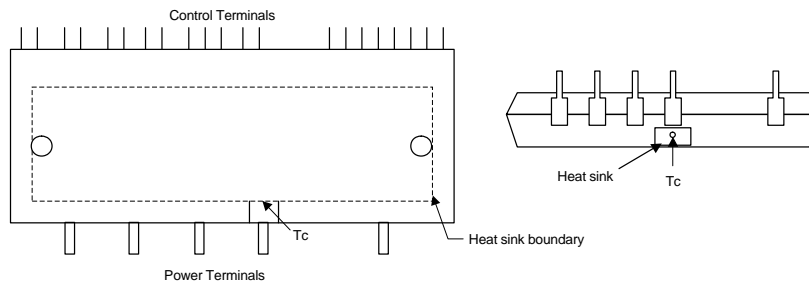
**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Ratings	Unit
$V_D$	Control supply voltage	Applied between : $V_D$ -GND	20	V
$V_{IN}$	Control input voltage	Applied between : $V_{IN}$ -GND	0~ $V_D+0.5$	V

**TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
$T_c$	Module case operation temperature	(Note 2)	-20~+100	$^\circ\text{C}$
$T_{stg}$	Storage temperature		-40~+125	$^\circ\text{C}$
$V_{iso}$	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	$V_{rms}$

**Note 2 :  $T_c$  MEASUREMENT POINT**



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**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
Rth(j-c)Q	Junction to case thermal resistance	Inverter IGBT part	—	—	1.55	°C/W
Rth(j-c)F		Inverter FWDi part	—	—	1.90	°C/W
Rth(c-f)	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.067	°C/W

**ELECTRICAL CHARACTERISTICS** (T<sub>j</sub> = 25°C, unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	V <sub>D</sub> = 15V, V <sub>IN</sub> = 5V, I <sub>C</sub> = 50A	—	1.8	2.4	V
V <sub>F</sub>	Forward voltage	I <sub>F</sub> = 50A	—	2.1	2.6	V
t <sub>on</sub>	Switching times	V <sub>CC</sub> = 300V, V <sub>D</sub> = 15V I <sub>C</sub> = 30A, T <sub>j</sub> = 125°C, V <sub>IN</sub> = 5V ↔ 0V Inductive load	—	0.29	—	μs
t <sub>r</sub>			—	0.13	—	μs
t <sub>c(on)</sub>			—	0.15	—	μs
t <sub>off</sub>			—	0.46	—	μs
t <sub>c(off)</sub>			—	0.17	—	μs
I <sub>CES</sub>	Collector-emitter cut-off current	V <sub>CE</sub> = 600V				mA
		T <sub>j</sub> = 25°C	—	—	1	
		T <sub>j</sub> = 125°C	—	—	10	
I <sub>R</sub>	Reverse current	V <sub>R</sub> = 600V				mA
		T <sub>j</sub> = 25°C	—	—	1	
		T <sub>j</sub> = 125°C	—	—	10	
I <sub>rr</sub>	FWDi reverse recovery current	V <sub>CC</sub> = 300V, V <sub>D</sub> = 15V, I <sub>C</sub> = 30A, T <sub>j</sub> = 25°C	—	13	—	A

**CONTROL (PROTECTION) PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V <sub>D</sub>	Control supply voltage	Applied between : V <sub>D</sub> -GND	13.5	15.0	16.5	V
I <sub>D</sub>	Circuit current	Applied between : V <sub>D</sub> -GND				mA
		V <sub>D</sub> = 15V, V <sub>IN</sub> = 5V	—	0.8	3.0	
		V <sub>D</sub> = 15V, V <sub>IN</sub> = 0V	—	0.7	3.0	
I <sub>IN</sub>	Control input current	V <sub>D</sub> = 15V, V <sub>IN</sub> = 5V	—	0.3	0.45	mA
V <sub>th(on)</sub>	ON threshold voltage	Applied between : V <sub>IN</sub> -GND	—	3.0	3.7	V
V <sub>th(off)</sub>	OFF threshold voltage		1.3	2.0	—	V
U <sub>VDt</sub>	Supply circuit under-voltage protection	T <sub>j</sub> ≤ 125°C	Trip level			V
U <sub>VDr</sub>			Reset level		10.3	—
			10.8	—	13.0	V

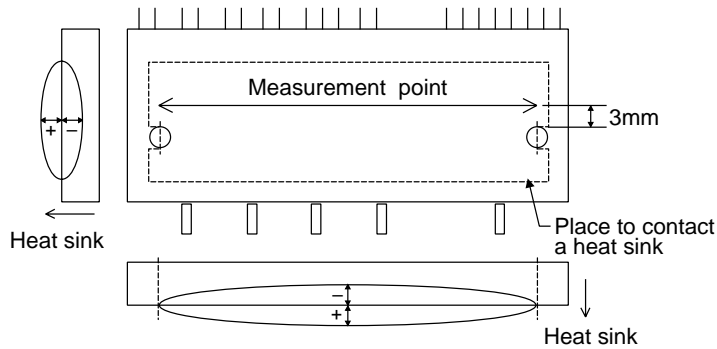
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**MECHANICAL CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting screw : M4	0.98	1.18	1.47	N·m
—	Weight		—	54	—	g
—	Heat-sink flatness	(Note 3)	-50	—	100	μm

**Note 3: Measurement point of heat-sink flatness**



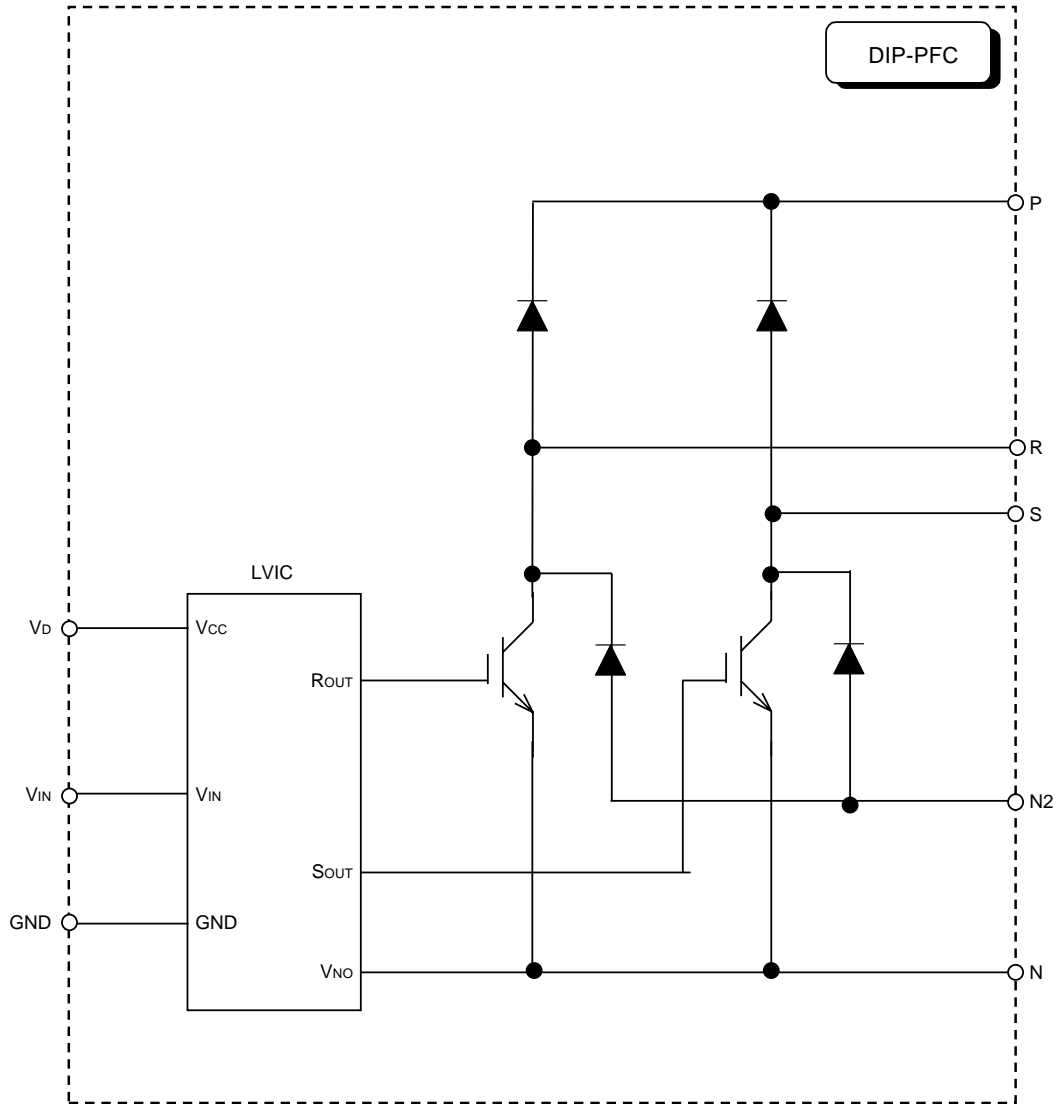
**RECOMMENDED OPERATION CONDITIONS**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_i$	Supply voltage	Applied between : S-R	90	—	264	V <sub>rms</sub>
$V_D$	Control supply voltage	Applied between : V <sub>D</sub> -GND	13.5	15.0	16.5	V
$\Delta V_D$	Control supply variation		-1	—	1	V/μs
$f_{PWM}$	PWM input frequency	$T_c \leq 100^\circ\text{C}$ , $T_j \leq 125^\circ\text{C}$	—	20	—	kHz
$V_{IN(on)}$	Input ON threshold voltage	Applied between : V <sub>IN</sub> -GND	4.0~V <sub>D</sub>			V
$V_{IN(off)}$	Input OFF threshold voltage		0~1.0			V

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Fig. 2 THE DIP-PFC INTERNAL CIRCUIT



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## DIP-PFC Wiring Guidelines

Because DIP-PFC switches large current at a very high speed, considerable large surge voltage is generated easily between P and N terminals. Please pay attention to the following items:

- The area of P-Co-N shown in Fig. 3 should be as small as possible because the rectangle shaped switching current flows on this route. In addition, please add a bypass condenser  $Co'$  with good frequency response such as a polypropylene film condenser closely to the P and N terminals.
- The two IGBT emitters are connected to the VNO terminal of LVIC inside the DIP-PFC. If the internal wiring inductance shown as  $L1$  and  $L2$  in Fig. 4 is too large, large surge voltage will be generated by  $di/dt$ . Especially, the lower the temperature, the faster the switching speed, therefore the larger the  $di/dt$ . This surge voltage applies to the VNO and N terminals, which is possible to destruct LVIC.
- In order to suppress the surge voltage, the external wiring method shown in Fig. 4 is recommended. To reduce the parasitic wiring inductance, the wiring of the external terminals of N(N-1) and N(N-2) should be made as short as possible.
- Please mount a fast clamp diode (EG01Y@Sanken) between N and control GND terminals to prevent control GND potential variation from the minus voltage of N terminal.

Fig. 3 DIP-PFC INTERFACE

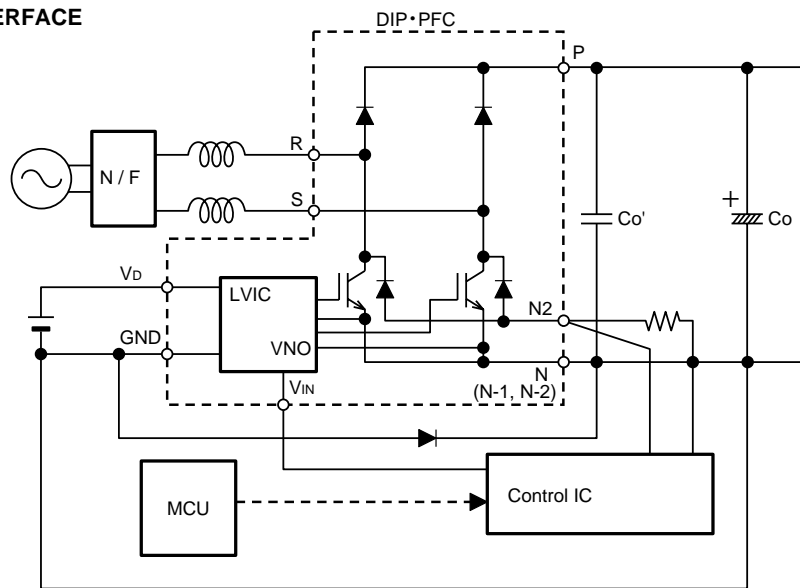


Fig. 4 RECOMMENDED WIRING METHOD

