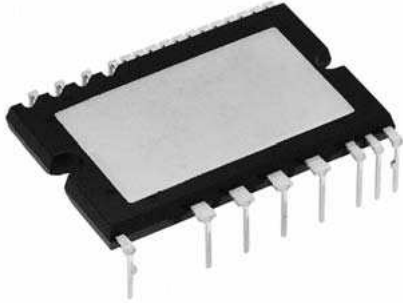# PS21993-4/-4A/-4C/-4W

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21993-4

INTEGRATED POWER FUNCTIONS

600V/10A low-loss CSTBT inverter bridge for three phase DC-to-AC power conversion

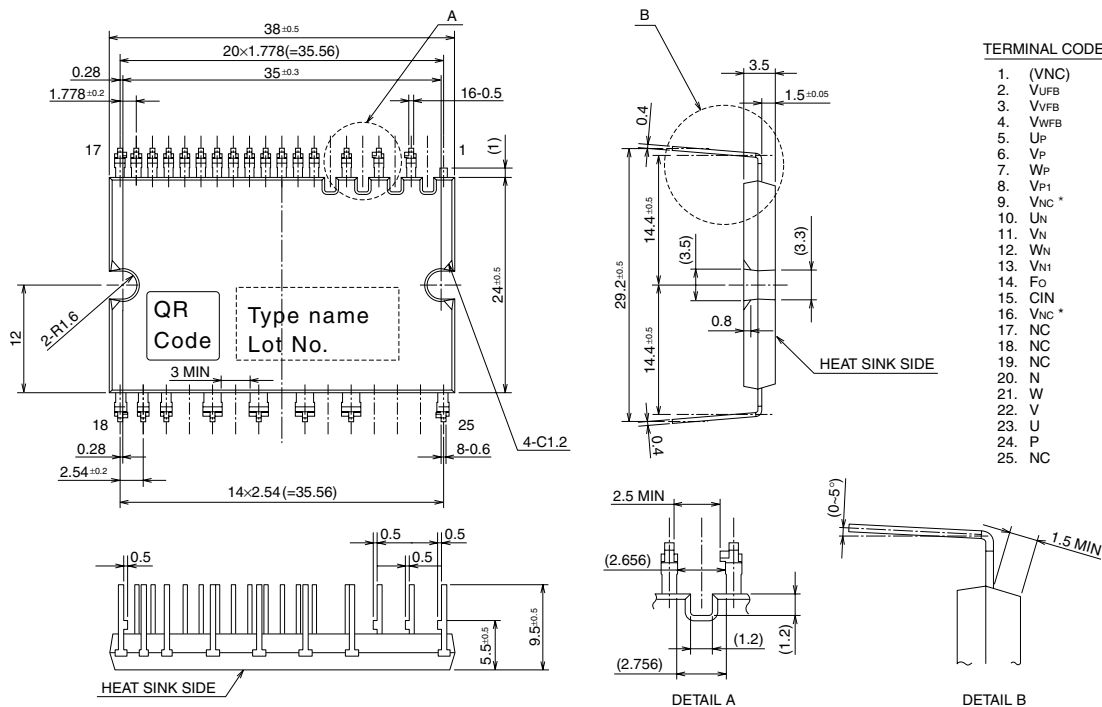### INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to a SC fault (N-side IGBT), a UV fault (N-side supply).
- Input interface : 3~5V line (High Active).
- UL Recognized : Yellow Card No. E80276

APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES (PS21993-4)

Dimensions in mm

TERMINAL CODE
1. (VNC)
2. V_{UFB}
3. V_{VFB}
4. V_{WFB}
5. U_P
6. V_P
7. W_P
8. V_{P1}
9. V_{NC} *
10. U_N
11. V_N
12. W_N
13. V_{N1}
14. F_O
15. CIN
16. V_{NC} *
17. NC
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

HEAT SINK SIDE

DETAIL A

DETAIL B

*) Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.
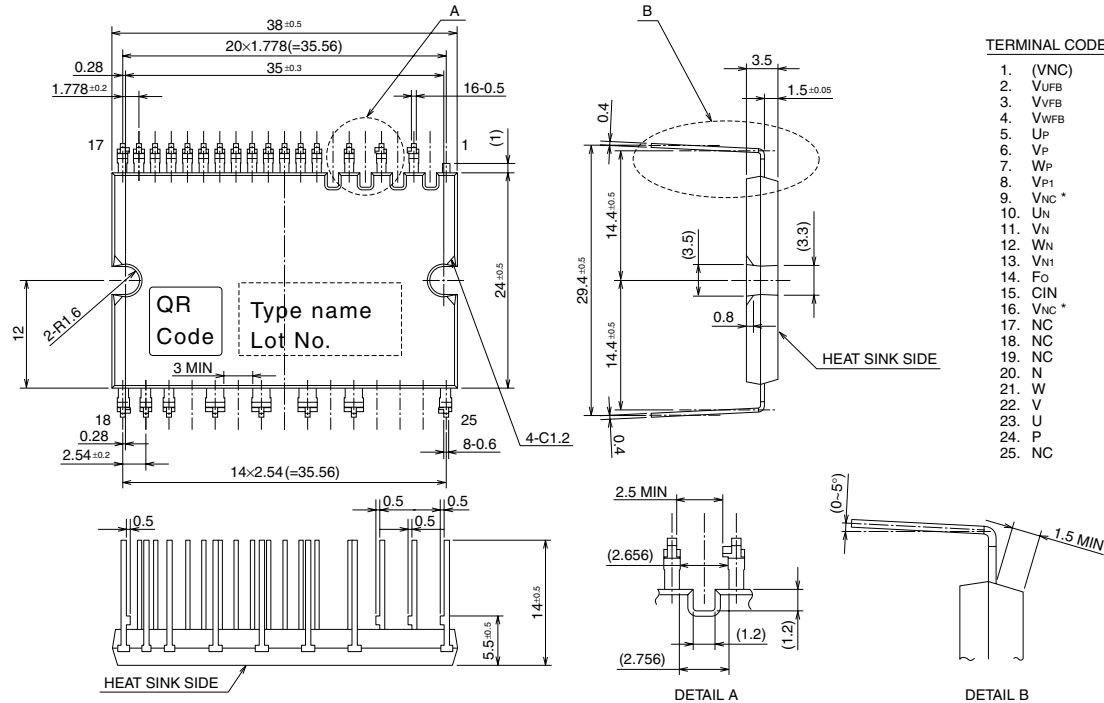
Note : CSTBT is registered trademark of MITSUBISHI ELECTRIC CORPORATION in Japan.

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Fig. 2 LONG TERMINAL TYPE PACKAGE OUTLINES (PS21993-4A)

Dimensions in mm

TERMINAL CODE
1. (VNC)
2. V_{UFB}
3. V_{VFB}
4. V_{WFB}
5. U_P
6. V_P
7. W_P
8. V_{P1}
9. V_{NC} *
10. U_N
11. V_N
12. W_N
13. V_{N1}
14. F_O
15. CIN
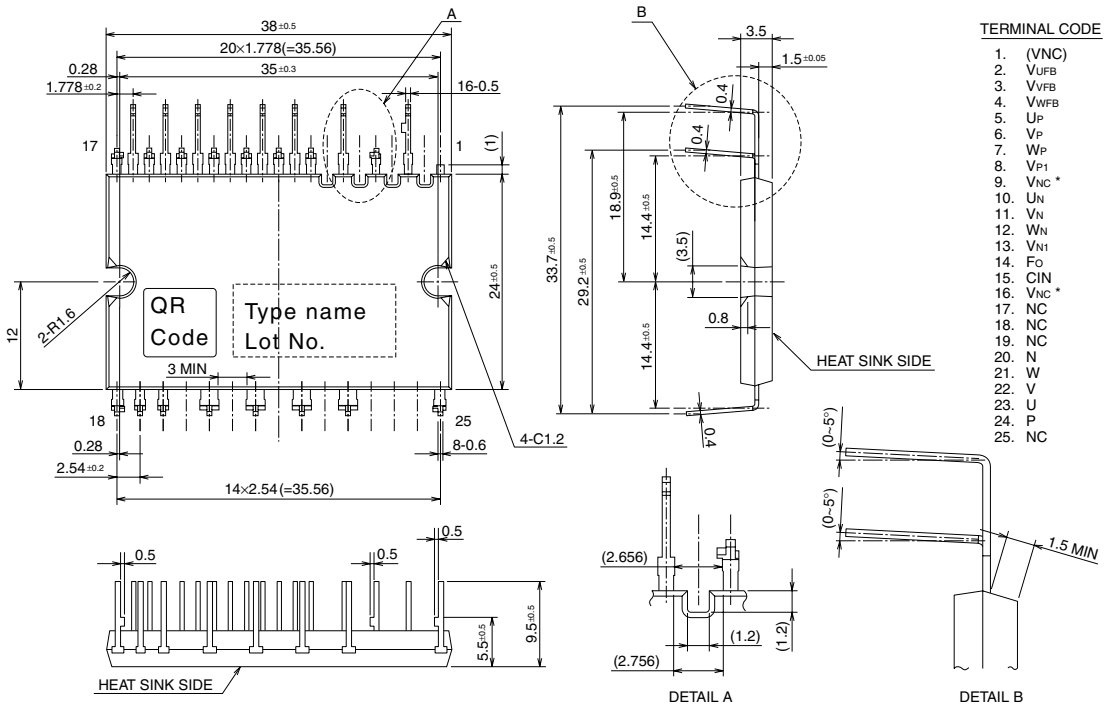16. V_{NC} *
17. NC
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

*) Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.

Fig. 3 ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21993-4C)
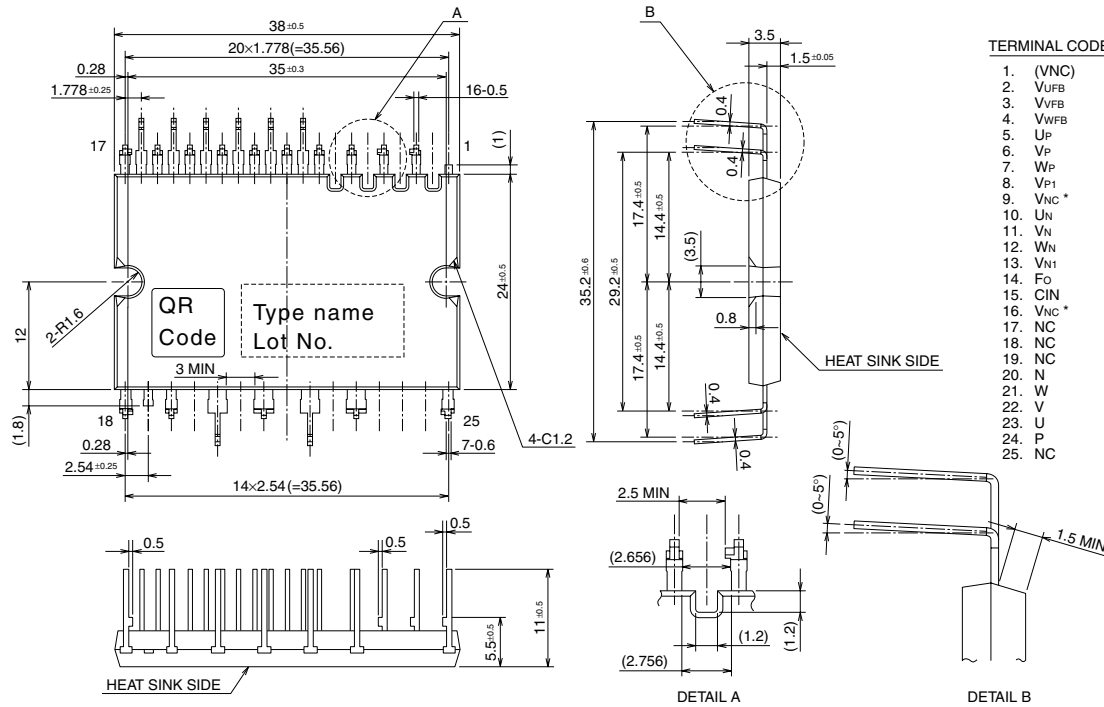
Dimensions in mm

TERMINAL CODE
1. (VNC)
2. V_{UFB}
3. V_{VFB}
4. V_{WFB}
5. U_P
6. V_P
7. W_P
8. V_{P1}
9. V_{NC} *
10. U_N
11. V_N
12. W_N
13. V_{N1}
14. F_O
15. CIN
16. V_{NC} *
17. NC
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

*) Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.

Fig. 4 BOTH SIDES ZIGZAG TERMINAL TYPE PACKAGE OUTLINES (PS21993-4W)

Dimensions in mm

TERMINAL CODE

1. (VNC)
2. V_{UFB}
3. V_{VFB}
4. V_{WFB}
5. U_P
6. V_P
7. W_P
8. V_{P1}
9. V_{NC} *
10. U_N
11. V_N
12. W_N
13. V_{N1}
14. F_O
15. CIN
16. V_{NC} *
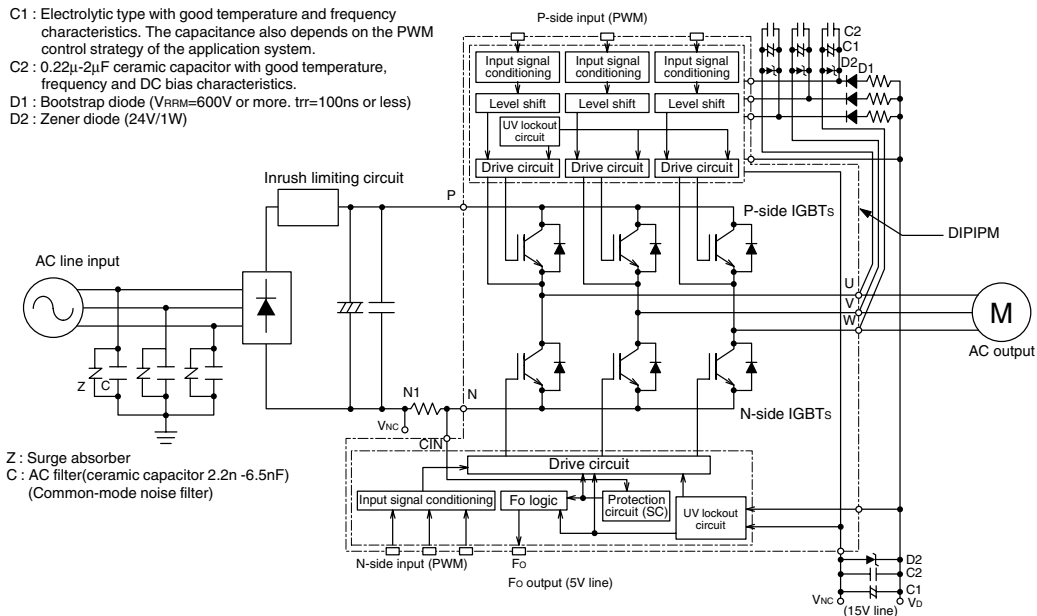17. NC
18. NC
19. NC
20. N
21. W
22. V
23. U
24. P
25. NC

*) Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.

QR Code is registered trademark of DENSO WAVE INCORPORATED in JAPAN and other countries.

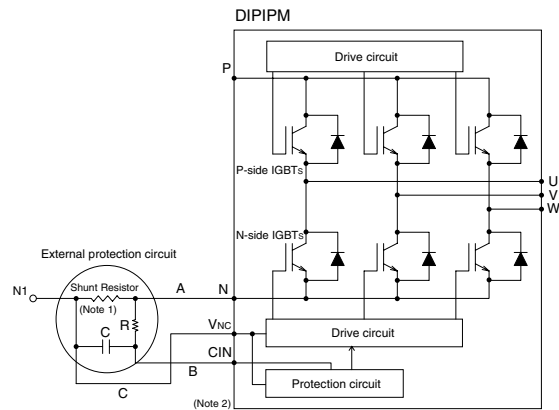## Fig. 5 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

C1 : Electrolytic type with good temperature and frequency characteristics. The capacitance also depends on the PWM control strategy of the application system.
C2 : 0.22µ-2µF ceramic capacitor with good temperature, frequency and DC bias characteristics.
D1 : Bootstrap diode (V_{RRM}=600V or more. trr=100ns or less)
D2 : Zener diode (24V/1W)

Z : Surge absorber
C : AC filter(ceramic capacitor 2.2n -6.5nF) (Common-mode noise filter)

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Fig. 6 EXTERNAL PART OF THE DIPIPM PROTECTION CIRCUIT

DIPIPM

Drive circuit

P

P-side IGBTs

U
V
W

N-side IGBTs

External protection circuit

Shunt Resistor
(Note 1)

N1   A   N

C   R

V$_{NC}$

CIN

C   B

(Note 2)

Drive circuit

Protection circuit

Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the N-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit).
When the sensed shunt voltage exceeds the SC trip-level, all the N-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.

I$_C$ (A)

SC Protection
Trip Level

Collector current
waveform

0   2   t$_w$ (μs)

Note1: In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0μs.
2: To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.
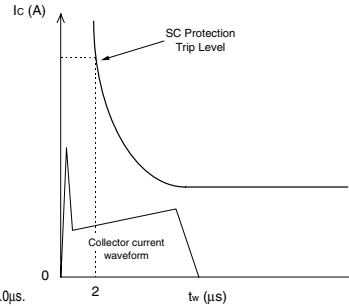
MAXIMUM RATINGS (T$_j$ = 25°C, unless otherwise noted)
INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V$_{CC}$	Supply voltage	Applied between P-N	450	V
V$_{CC(surge)}$	Supply voltage (surge)	Applied between P-N	500	V
V$_{CES}$	Collector-emitter voltage		600	V
±I$_C$	Each IGBT collector current	T$_C$ = 25°C	10	A
±I$_{CP}$	Each IGBT collector current (peak)	T$_C$ = 25°C, less than 1ms	20	A
P$_C$	Collector dissipation	T$_C$ = 25°C, per 1 chip	27.0	W
T$_j$	Junction temperature	(Note 1)	−20~+125	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIPIPM is 150°C (@ T$_C$ ≤ 100°C). However, to ensure safe operation of the DIPIPM, the average junction temperature should be limited to T$_{j(ave)}$ ≤ 125°C (@ T$_C$ ≤ 100°C).

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V$_D$	Control supply voltage	Applied between V$_{P1}$-V$_{NC}$, V$_{N1}$-V$_{NC}$	20	V
V$_{DB}$	Control supply voltage	Applied between V$_{UFB}$-U, V$_{VFB}$-V, V$_{WFB}$-W	20	V
V$_{IN}$	Input voltage	Applied between U$_P$, V$_P$, W$_P$, U$_N$, V$_N$, W$_N$-V$_{NC}$	−0.5~V$_D$+0.5	V
V$_{FO}$	Fault output supply voltage	Applied between F$_O$-V$_{NC}$	−0.5~V$_D$+0.5	V
I$_{FO}$	Fault output current	Sink current at F$_O$ terminal	1	mA
V$_{SC}$	Current sensing input voltage	Applied between CIN-V$_{NC}$	−0.5~V$_D$+0.5	V

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TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (short circuit protection capability)	V_D = 13.5~16.5V, Inverter part T_j = 125°C, non-repetitive, less than 2μs	400	V
T_C	Module case operation temperature	(Note 2)	−20~+100	°C
T_{stg}	Storage temperature		−40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, 1 minute, Between pins and heat sink plate	1500	V_{rms}

Note 2: T_C measurement point
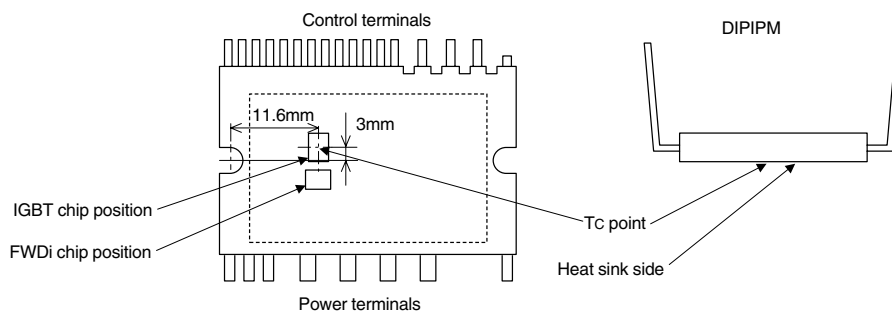
THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	—	—	3.7	°C/W
$R_{th(j-c)F}$		Inverter FWDi part (per 1/6 module)	—	—	4.5	°C/W

Note 3 : Grease with good thermal conductivity and long-term quality should be applied evenly with +100μm~+200μm on the contacting surface of DIPIPM and heat sink.
The contacting thermal resistance between case and heat sink ($R_{th(c-f)}$) is determined by the thickness and the thermal conductivity of the applied grease.
For reference, $R_{th(c-f)}$ (per 1/6 module) is about 0.3°C/W when the grease thickness is 20μm and the thermal conductivity is 1.0W/mK.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)
INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB}$ = 15V V_{IN} = 5V	I_C = 10A, T_j = 25°C	—	1.60	2.10	V
			I_C = 10A, T_j = 125°C	—	1.70	2.20	
V_{EC}	FWDi forward voltage	T_j = 25°C, −I_C = 10A, V_{IN} = 0V		—	1.70	2.20	V
t_{on}	Switching times	V_{CC} = 300V, $V_D = V_{DB}$ = 15V I_C = 10A, T_j = 125°C, V_{IN} = 0 ↔ 5V Inductive load (upper-lower arm)		0.60	1.10	1.70	μs
t_{rr}				—	0.30	—	μs
$t_{c(on)}$				—	0.40	0.60	μs
t_{off}				—	1.50	2.35	μs
$t_{c(off)}$				—	0.40	1.00	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition			Limits			Unit
					Min.	Typ.	Max.	
I_D	Circuit current	$V_D = V_{DB} = 15V$	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}		—	—	2.80	mA
		$V_{IN} = 5V$	V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		—	—	0.55	mA
		$V_D = V_{DB} = 15V$	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}		—	—	2.80	mA
		$V_{IN} = 0V$	V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		—	—	0.55	mA
V_{FOH}	Fault output voltage	$V_{SC} = 0V$, F_O terminal pull-up to 5V by $10k\Omega$			4.9	—	—	V
V_{FOL}		$V_{SC} = 1V$, $I_{FO} = 1mA$			—	—	0.95	V
$V_{SC(ref)}$	Short circuit trip level	$V_D = 15V$		(Note 4)	0.43	0.48	0.53	V
I_{IN}	Input current	$V_{IN} = 5V$			0.70	1.00	1.50	mA
UV_{DBt}	Control supply under-voltage protection	$T_j \leq 125°C$	Trip level		10.0	—	12.0	V
UV_{DBr}			Reset level		10.5	—	12.5	V
UV_{Dt}			Trip level		10.3	—	12.5	V
UV_{Dr}			Reset level		10.8	—	13.0	V
t_{FO}	Fault output pulse width		(Note 5)		20	—	—	µs
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}			—	2.1	2.6	V
$V_{th(off)}$	OFF threshold voltage				0.8	1.3	—	V
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage				0.35	0.65	—	V

Note 4 : Short circuit protection works only for the N-side. Please select the external shunt resistance such that the SC trip-level is up to 1.7 times of the current rating.

5 : Fault signal is asserted only corresponding to a SC or a UV failure at N-side, and the Fo pulse width is different for each failure modes. For SC failure, Fo output is with a fixed width of 20µs(min), but for UV failure, Fo outputs continuously during the whole UV period, however, the minimum Fo pulse width is 20µs(min) for very short UV period less than 20µs.

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 6)	Recommended : 0.69 N·m	0.59	—	0.78	N·m
Weight			—	10	—	g
Heat-sink flatness		(Note 7)	−50	—	100	µm

Note 6 : Plain washers (ISO 7089~7094) are recommended.

Note 7: Flatness measurement position

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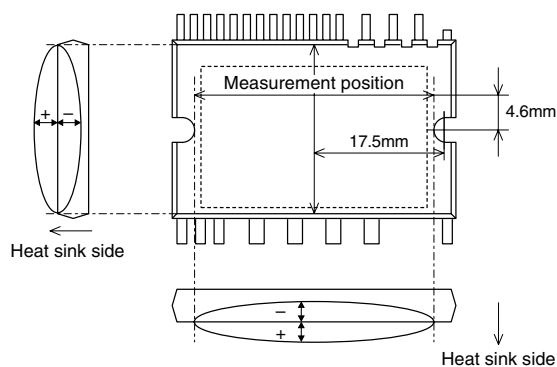
PS21993-4/-4A/-4C/-4W

TRANSFER-MOLD TYPE
INSULATED TYPE

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied between P-N		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			−1	—	1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal, $T_C \le 100°C$		1.5	—	—	μs
f_{PWM}	PWM input frequency	$T_C \le 100°C$, $T_j \le 125°C$		—	—	20	kHz
I_O	Allowable rms current	$V_{CC} = 300V$, $V_D = V_{DB} = 15V$, P.F = 0.8, sinusoidal PWM, $T_j \le 125°C$, $T_C \le 100°C$ (Note 8)	$f_{PWM} = 5kHz$	—	—	5.5	Arms
			$f_{PWM} = 15kHz$	—	—	3.5	
PWIN(on)	Allowable minimum input pulse width			0.5	—	—	μs
PWIN(off)		(Note 9)		0.5	—	—	
V_{NC}	V_{NC} variation	Between V_{NC}-N (including surge)		−5.0	—	5.0	V

Note 8 : The allowable rms current value depends on the actual application conditions.
9 : IPM might not make response if the input signal pulse width is less than the recommended minimum value.
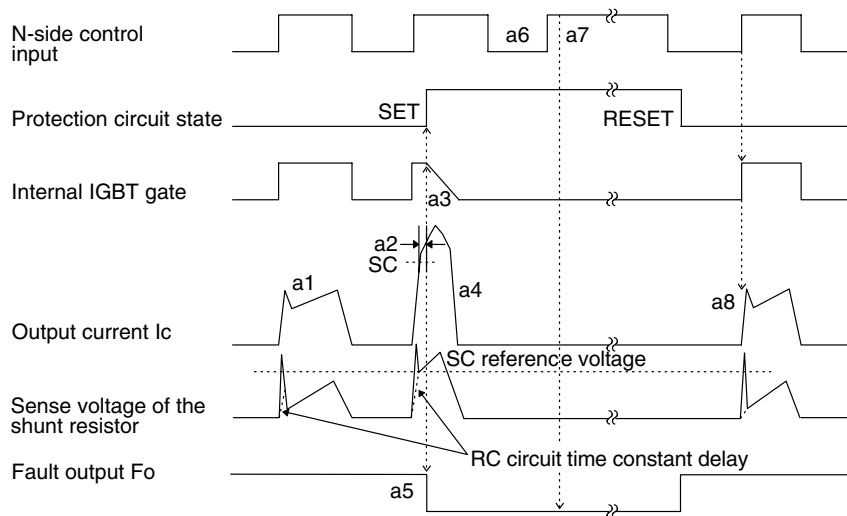
Fig. 7 THE DIPIPM INTERNAL CIRCUIT

MITSUBISHI ELECTRIC
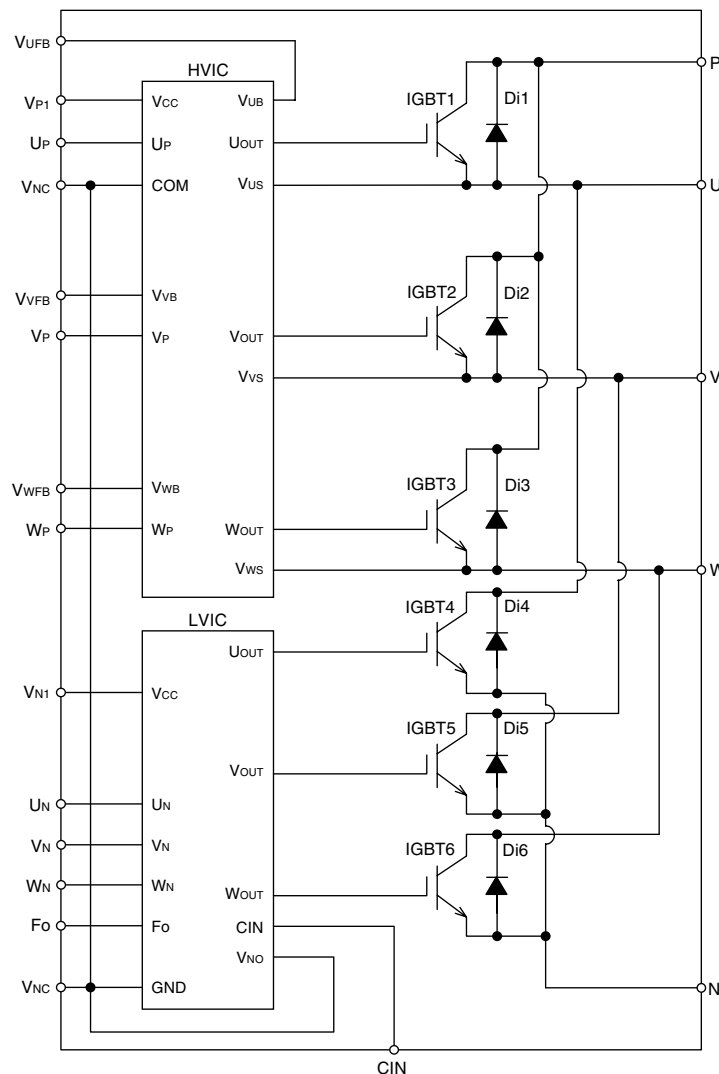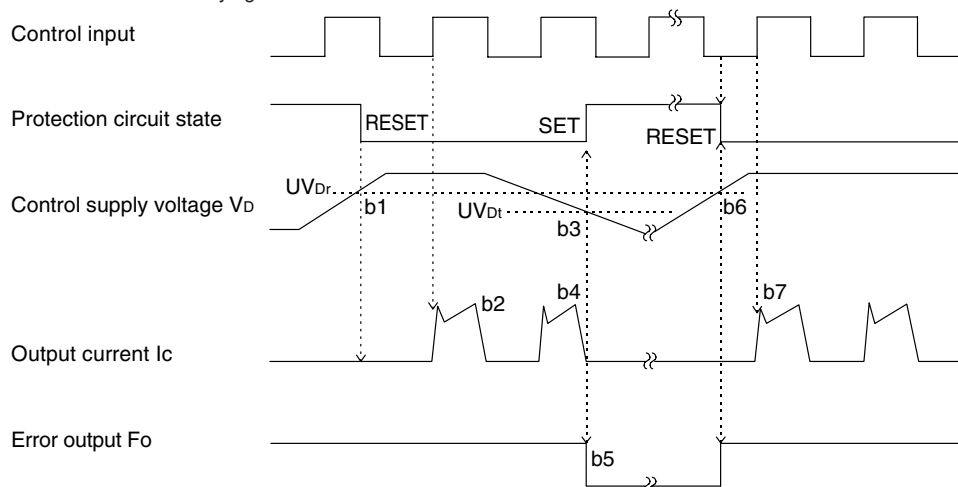
Fig. 8 TIMING CHART OF THE PROTECTIVE FUNCTIONS

[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation : IGBT ON and carrying current.
a2. Short circuit is detected (SC trigger).
a3. All N-side IGBTs' gates are hard interrupted.
a4. All N-side IGBTs turn OFF.
a5. F_O is output ($t_{FO(min)} = 20\mu s$).
a6. Input "L".
a7. Input "H". But IGBT is still OFF state during outputting F_O.
a8. IGBT turns ON when L→H signal is input after F_O is reset.

N-side control input

a6   a7

Protection circuit state   SET   RESET

Internal IGBT gate   a3

a2 → SC

a1   a4   a8

Output current Ic

SC reference voltage

Sense voltage of the shunt resistor

RC circuit time constant delay

Fault output Fo

a5

[B] Under-Voltage Protection (N-side, UV_D)

b1. Control supply voltage V_D rises : After V_D level rises over under voltage reset level (UV_{Dr}), the circuits start to operate when next input is applied.
b2. Normal operation : IGBT ON and carrying current.
b3. V_D level dips to under voltage trip level. (UV_{Dt}).
b4. All N-side IGBTs turn OFF in spite of control input condition.
b5. F_O is output. ($t_{FO} \geq 20\mu s$ and F_O outputs continuously during UV period).
b6. V_D level rises over UV_{Dr}.
b7. Normal operation : IGBT ON and carrying current.

Control input

Protection circuit state   RESET   SET   RESET

Control supply voltage V_D UV_{Dr} b1 UV_{Dt} b3   b6

Output current Ic   b2   b4   b7

Error output Fo   b5

[C] Under-Voltage Protection (P-side, UV$_{DB}$)

c1. Control supply voltage V$_{DB}$ rises : After V$_{DB}$ level rises over under voltage reset level (UV$_{DBr}$), the circuits start to operate when next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. V$_{DB}$ level dips to under voltage trip level. (UV$_{DBt}$).
c4. P-side IGBT turns OFF in spite of control input signal level, but there is no F$_O$ signal output.
c5. V$_{DB}$ level rises over UV$_{DBr}$.
c6. Normal operation : IGBT ON and carrying current.
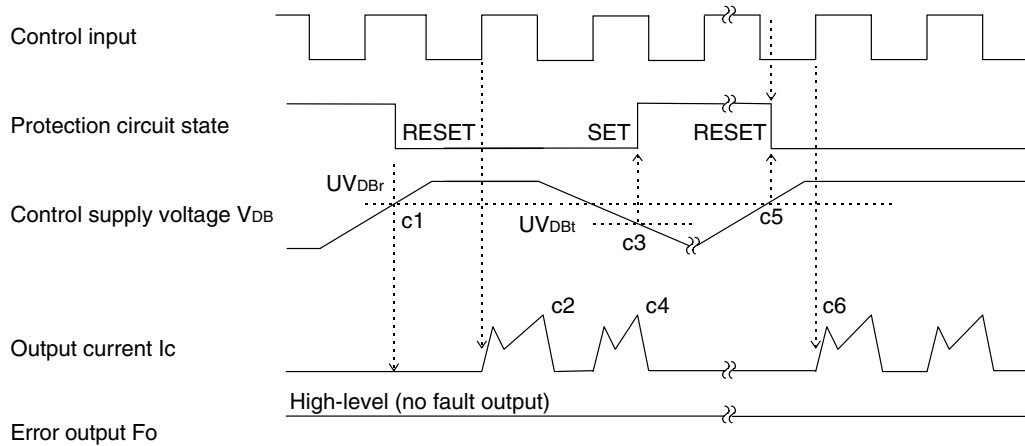
Fig. 9 AN INSTANCE OF INTERFACE CIRCUIT
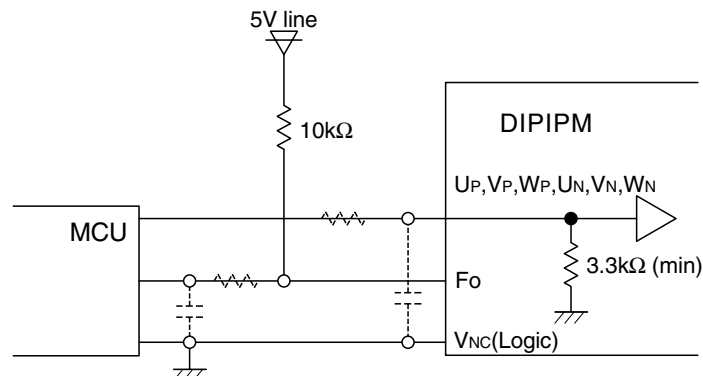
Note : The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.
Input circuit integrates a 3.3kΩ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.
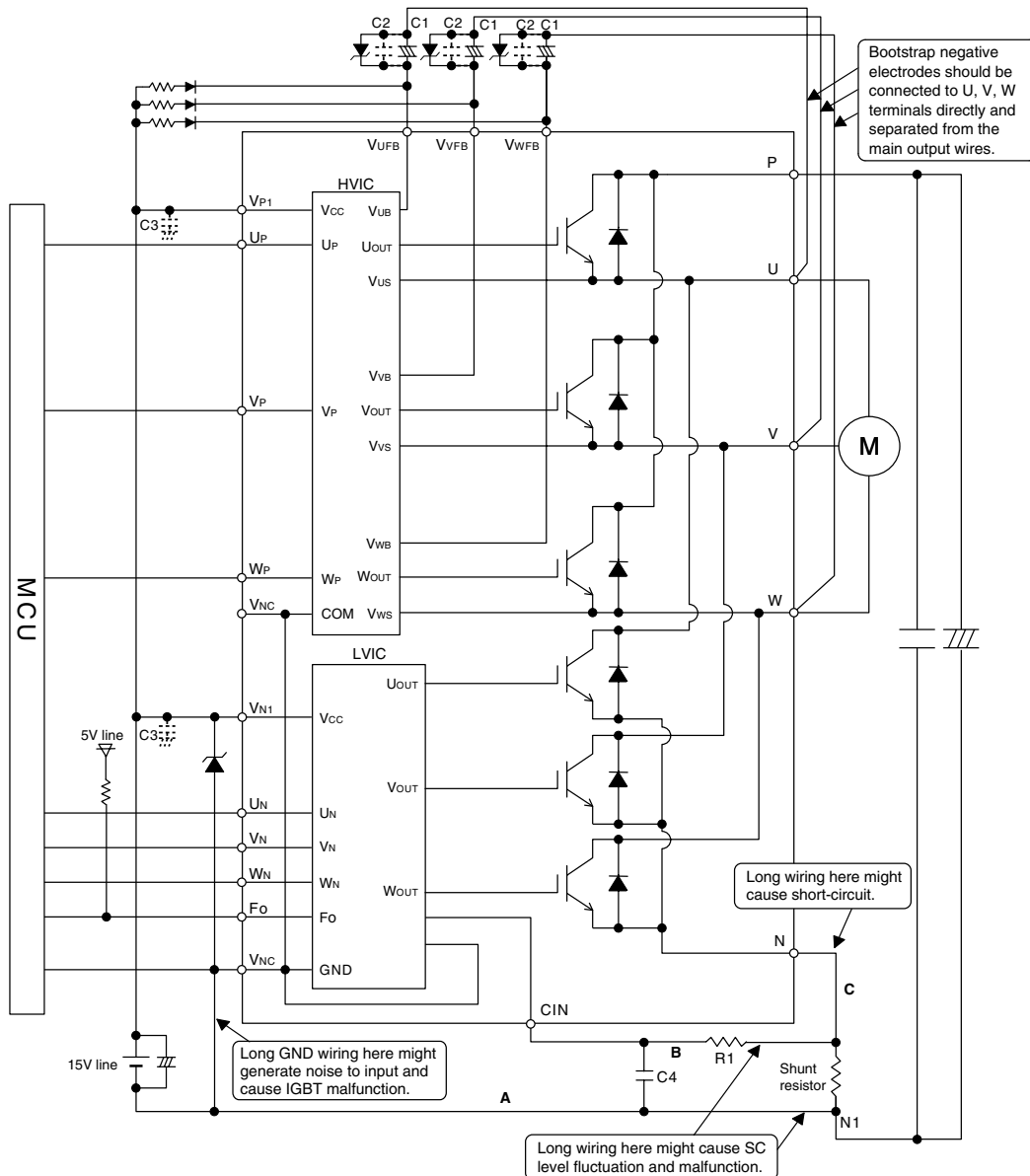
Fig. 10 WIRING CONNECTION OF SHUNT RESISTOR

MITSUBISHI ELECTRIC
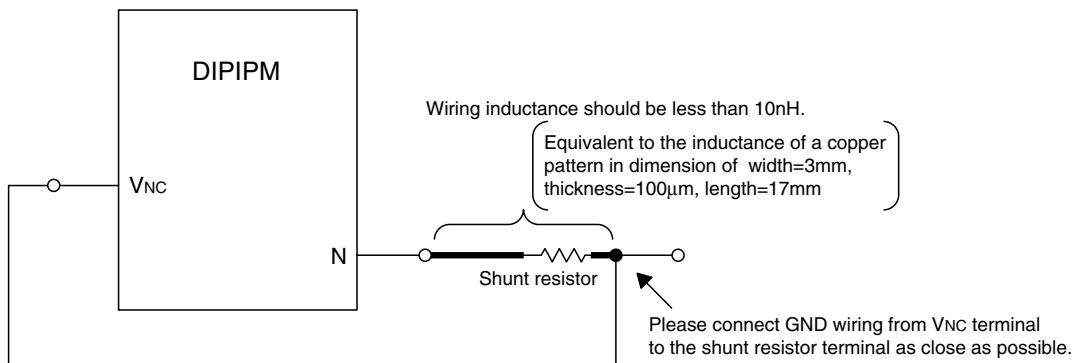
Fig. 11 AN EXAMPLE OF TYPICAL DIPIPM APPLICATION CIRCUIT

Note 1 : Input drive is High-active type. There is a 3.3kΩ (Min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

2 : Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

3 : Fo output is open drain type. It should be pulled up to the MCU or control power supply (e.g. 5V, 15V) by a resistor that makes I_{Fo} up to 1mA.

4 : To prevent erroneous protection, the wiring of A, B, C should be as short as possible.

5 : The time constant R1C4 of the protection circuit should be selected in the range of 1.5-2μs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C4

6 : All capacitors should be mounted as close to the terminals of DIPIPM as possible. (C1: good temperature, frequency characteristic electrolytic type, and C2, C3 (0.22~2μF) : good temperature, frequency and DC bias characteristic ceramic type are recommended.)

7 : To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber between the P-N1 terminals is recommended.

8 : Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND and leave the other open.

9 : It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.

10 : If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1.

11 : High voltage (V_{RRM} =600V or more) and fast recovery type (t_{rr}=100ns or less) diodes should be used in the bootstrap circuit.

Sep. 2008

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