CCD area image sensor
S7199-01

Front-illuminated FFT-CCDs for X-ray imaging

S7199-01 is a family of FFT-CCD image sensors specifically designed for X-ray imaging. A FOS (Fiber Optic plate with Scintillator) that converts X-ray into visible-light is mounted on the CCD chip, which enables S7199-01 to acquire the X-ray imaging. Two CCD chips of symmetric from side to side are mounted closely for realizing the possible minimum dead space in between. The effective photosensitive length of about 150 mm in total is realized; each chip has 1536 × 128 pixels and the pixel size is 48 × 48 µm. Even a X-ray image of moving object can be taken by taking a unique operation method of TDI, which can also be useful for a non-destructive inspection where the object moves on a belt conveyer.
The each chip of S7199-01 has an effective pixel size of 48 × 48 µm and is available in active area of 73.728 (H) × 6.144 (V) mm^2. FOP type is also available (S7199-01F).

Features

- 1536 (H) × 128 (V) pixel format
- Pixel size: 48 × 48 µm
- Buttable structure of 2 chips
- Coupled with FOS for X-ray imaging
- TDI (Time Delay Integration) operation
- 100 % fill factor
- Wide dynamic range
- Low dark signal
- Low readout noise
- MPP operation

Applications

- General X-ray imaging
- Non-destructive inspection
- Dental panorama

■ Selection guide

Type No.	Window	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm(V)]
S7199-01	FOS (fiber optic plate with scintillator)	Non-cooled	1536 × 128	1536 × 128	73.728 × 6.144
S7199-01F*	FOP (fiber optic plate)				

Note) As an input window, FOS is suited to S7199-01.
* When this product is used for X-ray detection applications, the user should assemble a scintillator or phosphor sheet.

■ General ratings

Parameter	S7199-01	S7199-01F
CCD structure	Full frame transfer or TDI	
Fill factor	100 %	
Number of active pixels	1536 (H) × 128 (V) *1	
Pixel size	48 (H) × 48 (V) µm	
CCD active area	73.728 (H) × 6.144 (V) mm *1	
X-ray sensitive area	146 × 6 mm	
Vertical clock phase	2 phase	
Horizontal clock phase	2 phase	
Output circuit	Two-stage MOSFET source follower with load resistance	
X-ray resolution	4 to 6 Lp/mm at 60 kVp, 20 µGy	-
Total dose irradiation	50 Gy max.	
Package	40 pin ceramic package	

*1: Number of active pixels per chip. Two chips are used.

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	-20	-	+70	°C
Operating temperature	Topr	0	-	+40	°C
OD voltage	V_{OD}	-0.5	-	+20	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
IGV voltage	V_{IGV}	-15	-	+15	V
IGH voltage	V_{IGH}	-15	-	+15	V
SG voltage	V_{SG}	-15	-	+15	V
OG voltage	V_{OG}	-15	-	+15	V
RG voltage	V_{RG}	-15	-	+15	V
TG voltage	V_{TG}	-15	-	+15	V
Vertical clock voltage	V_{P1AV}, V_{P2AV} V_{P1BV}, V_{P2BV}	-15	-	+15	V
Horizontal clock voltage	V_{P1AH}, V_{P2AH} V_{P1BH}, V_{P2BH}	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	12	15	-	V
Reset drain voltage			V_{RD}	12	13	14	V
Output gate voltage			V_{OG}	-0.5	2	5	V
Output transistor ground voltage			V_{SSA}	-	0	-	V
Substrate voltage			V_{SSD}	-5	0	-	V
Test point	Vertical input source		V_{ISV}	-	V_{RD}	-	V
	Vertical input gate		V_{IGV}	-8	0	-	
	Horizontal input gate		V_{IGH}	-8	0	-	
Vertical shift register clock voltage		High	V_{P1AVH}, V_{P2AVH} V_{P1BVH}, V_{P2BVH}	0	3	6	V
		Low	V_{P1AVL}, V_{P2AVL} V_{P1BVL}, V_{P2BVL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1AHH}, V_{P2AHH} V_{P1BHH}, V_{P2BHH}	0	3	6	V
		Low	V_{P1AHL}, V_{P2AHL} V_{P1BHL}, V_{P2BHL}	-9	-8	-7	
Summing gate voltage		High	V_{SGH}	0	3	6	V
		Low	V_{SGL}	-9	-8	-7	
Reset gate voltage		High	V_{RGH}	0	3	6	V
		Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage		High	V_{TGH}	0	3	6	V
		Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc		-	2	4	MHz
Reset clock frequency	frg		-	2	4	MHz
Vertical shift register capacitance	C_{P1AV}, C_{P2AV} C_{P1BV}, C_{P2BV}		-	15000	-	pF
Horizontal shift register capacitance	C_{P1AH}, C_{P2AH} C_{P1BH}, C_{P2BH}		-	500	-	pF
Summing gate capacitance	C_{SG}		-	15	-	pF
Reset gate capacitance	C_{RG}		-	10	-	pF
Transfer gate capacitance	C_{TG}		-	500	-	pF
Transfer efficiency	CTE	*2	0.99995	0.99999	-	
DC output level	Vout	*3	5	8	11	V
Output impedance	Zo	*3	-	500	-	Ω
Power dissipation	P	*3, *4	-	60	-	mW

*2: Measured at half of the full well capacity. CTE is defined per pixel.
*3: V_{OD}=15 V.
*4: Power dissipation of the on-chip amplifier (each chip).

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter			Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat		-	Fw × Sv	-	V
Full well capacity	Vertical		Fw		600	1200	-	ke⁻
	Horizontal				600	1200	-	
	Summing				600	1200	-	
CCD node sensitivity			Sv	*2	0.45	0.6	-	μV/e⁻
Dark current (MPP mode)			DS	*3	-	8	24	ke⁻/pixel/s
Readout noise	Ta=25 °C		Nr	*4	-	90	-	e⁻rms
	Ta=-40 °C				-	60	120	
Dynamic range			DR	*5	5000	20000	-	
X-ray response non-uniformity (S7199-01)			XRNU	*6	-	±10	±30	%
Photo response non-uniformity (S7199-01F)			PRNU	*7				
Blemish	Point defects *8	White spots	-		-	-	10	-
		Black spots			-	-	10	
	Cluster defects			*9	-	-	0	
	Column defects			*10	-	-	0	
X-ray resolution (S7199-01)			ΔR		4	6	-	Lp/mm

*2: V_{OD}=15 V.
*3: Dark current doubles for every 5 to 7 °C.
*4: Operating frequency is 2 MHz.
*5: Dynamic range = Full well capacity / Readout noise
*6: X-ray irradiation of 60kVp, measured at half of the full well capacity.

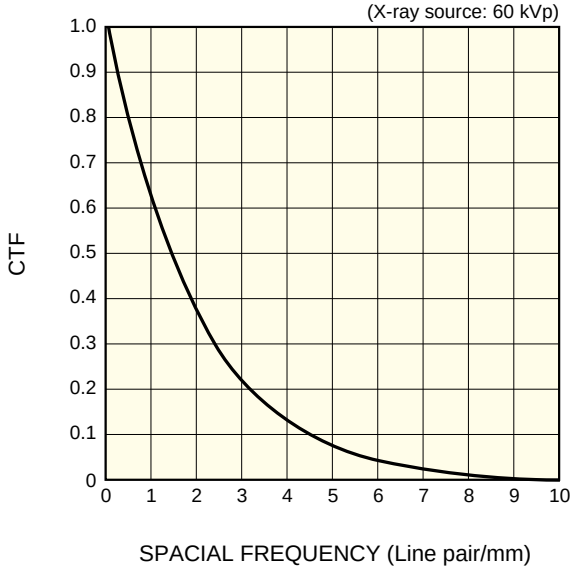
$$\text{XRNU (\%)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

Measuring region that is within 146.0 mm (H) × 6.0 mm (V) (refer to dimensional outline)
*7: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 565 nm)

$$\text{PRNU (\%)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*8: White spots > 20 times of typ. dark signal (8 ke⁻/pixel/s).
Black spots > 50 % reduction in response relative to adjacent pixels, measured at half of the full well capacity.
*9: continuous 2 to 9 point defects.
*10: continuous >10 point defects.

■ Resolution (S7199-01)



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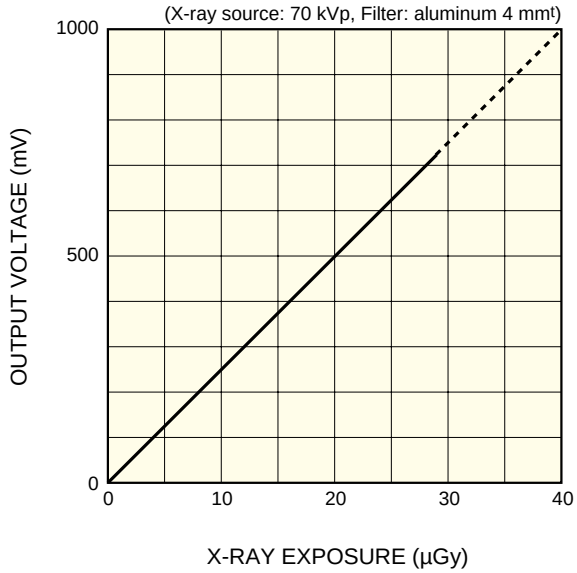
■ Response (S7199-01)



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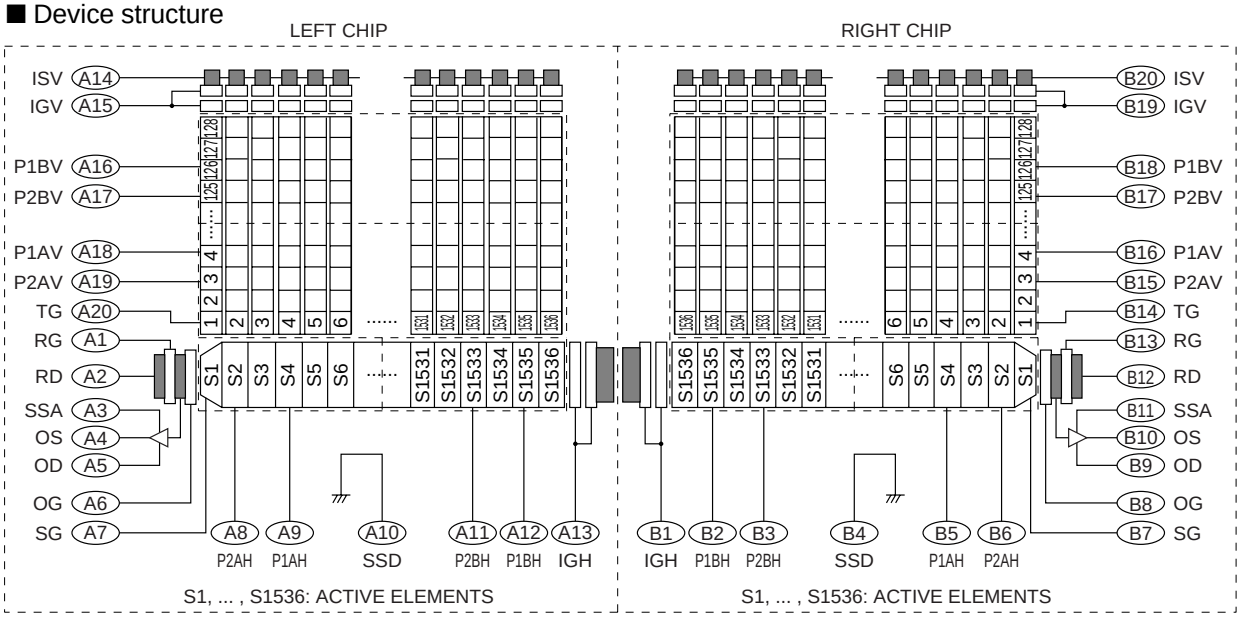
■ Device structure



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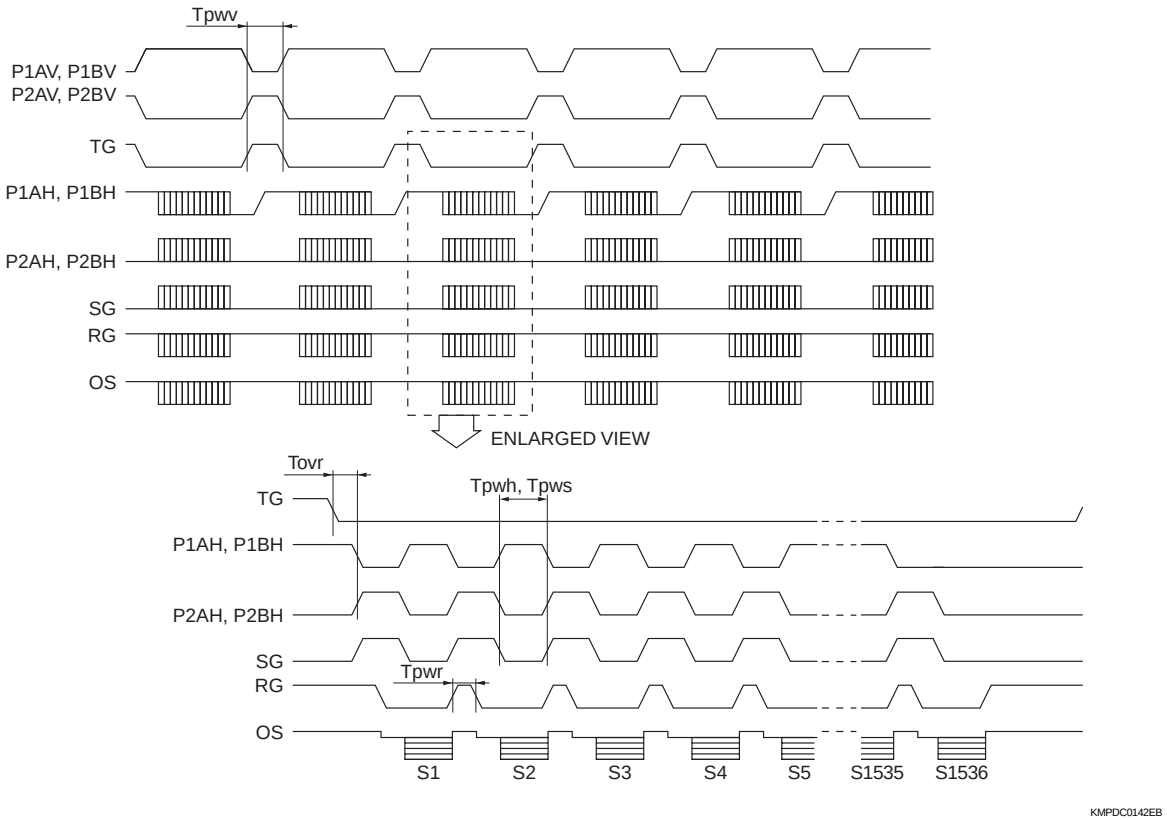
■ Pixel format

← Left Horizontal Direction → Right						
Blank	Optical black	Isolation	Effective	Isolation	Optical black	Blank
0	0	0	1536	0	0	0

Top ← Vertical direction → Bottom		
Isolation	Effective	Isolation
0	128	0

■ Timing chart (TDI operation)



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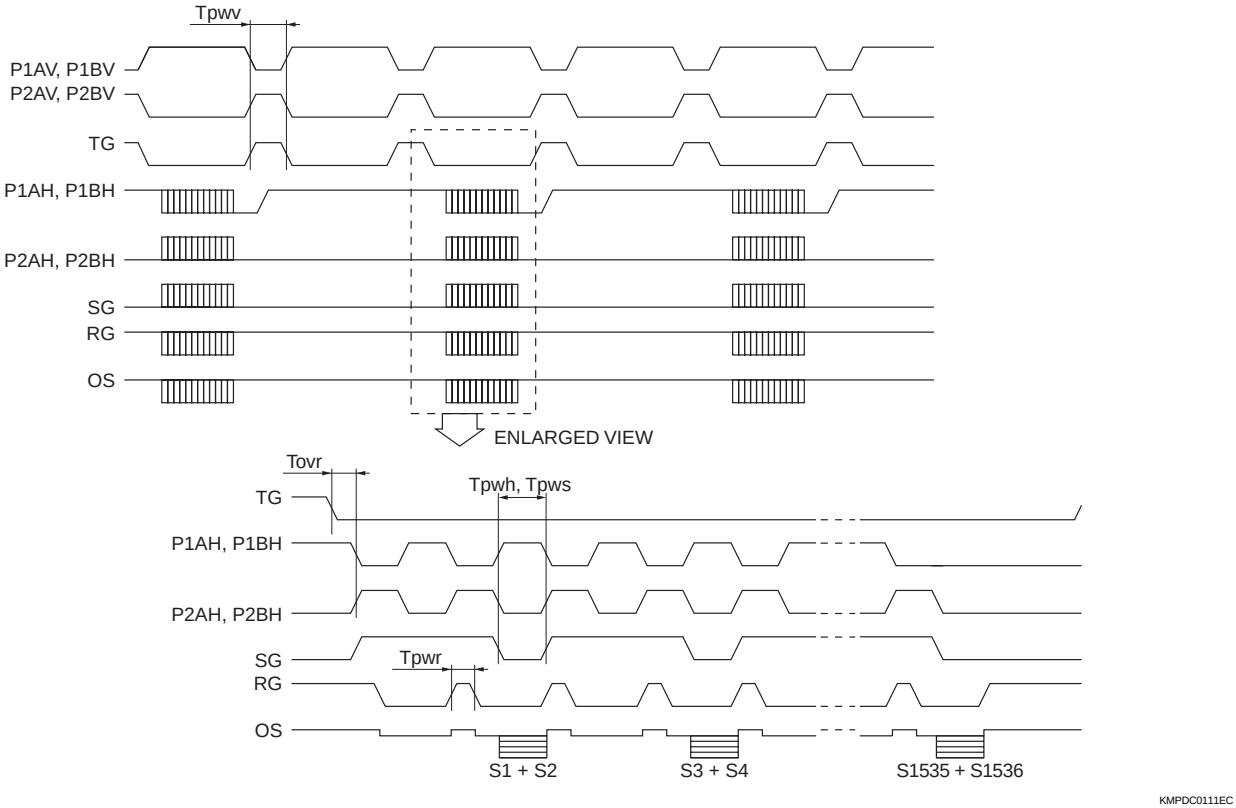
■ Timing chart (TDI operation, 2 × 2 pixel binning)

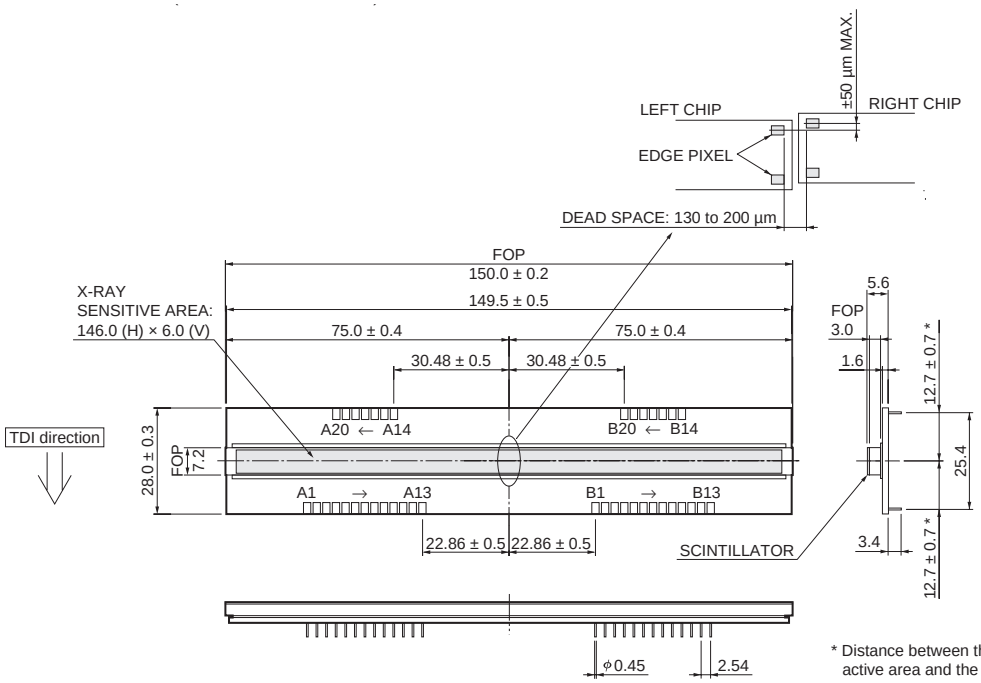


Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1AV, P1BV, P2AV, P2BV, TG	Pulse width	tpwv	*14, *15	30	60	-	µs
	Rise and fall time	tprv, tpfv		200	-	-	ns
P1AH, P1BH, P2AH, P2BH	Pulse width	tpwh	*15	125	250	-	ns
	Rise and fall time	tprh, tpfh		10	-	-	ns
	Duty ratio			-	50	-	%
SG	Pulse width	tpws		125	250	-	ns
	Rise and fall time	tprs, tpfs		10	-	-	ns
	Duty ratio			-	50	-	%
RG	Pulse width	tpwr		10	50	-	ns
	Rise and fall time	tprr, tpfr		5	-	-	ns
TG-P1AH, P1BH	Overlap time	tovr		10	20	-	µs

*14: TG terminal can be short-circuited to P2AV terminal.
*15: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■ Dimensional outline (unit: mm)

S7199-01



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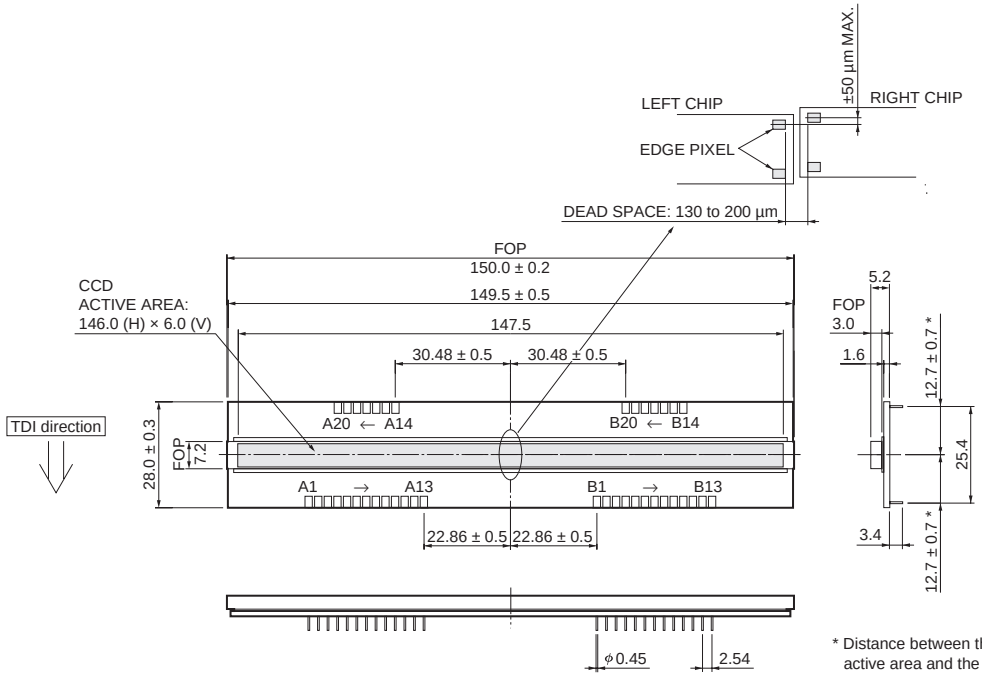
S7199-01F



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■ Pin connections

Pin No.	Symbol	Description	Remark
A1	RG	Reset gate	
A2	RD	Reset drain	
A3	SSA	Analog ground	
A4	OS	Output transistor source	
A5	OD	Output transistor drain	
A6	OG	Output gate	
A7	SG	Summing gate	
A8	P2AH	CCD horizontal register clock A-2	
A9	P1AH	CCD horizontal register clock A-1	
A10	SSD	Digital ground	
A11	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
A12	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
A13	IGH	Test point (Horizontal input gate)	
A14	ISV	Test point (Vertical input source)	Shorted to RD
A15	IGV	Test point (Vertical input gate)	
A16	P1BV	CCD vertical register clock B-1	Same timing as P1AV
A17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
A18	P1AV	CCD vertical register clock A-1	
A19	P2AV	CCD vertical register clock A-2	
A20	TG	Transfer gate	
B1	IGH	Test point (Horizontal input gate)	
B2	P1BH	CCD horizontal register clock B-1	Same timing as P1AH
B3	P2BH	CCD horizontal register clock B-2	Same timing as P2AH
B4	SSD	Digital ground	
B5	P1AH	CCD horizontal register clock A-1	
B6	P2AH	CCD horizontal register clock A-2	
B7	SG	Summing gate	
B8	OG	Output gate	
B9	OD	Output transistor drain	
B10	OS	Output transistor source	
B11	SSA	Analog ground	
B12	RD	Reset drain	
B13	RG	Reset gate	
B14	TG	Transfer gate	
B15	P2AV	CCD vertical register clock A-2	
B16	P1AV	CCD vertical register clock A-1	
B17	P2BV	CCD vertical register clock B-2	Same timing as P2AV
B18	P1BV	CCD vertical register clock B-1	Same timing as P1AV
B19	IGV	Test point (Vertical input gate)	
B20	ISV	Test Point (Vertical input source)	Shorted to RD

■ Precautions for use (Electrostatic countermeasures)

* Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
* Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
* Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
* Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

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Cat. No. KMPD1077E11
Apr. 2011 DN