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InGaAs area image sensor

G11097-0606S

Image sensor with 64 × 64 pixels developed for two-dimensional infrared imaging

The G11097-0606S has a hybrid structure consisting of a CMOS readout circuit (ROIC: readout integrated circuit) and back-illuminated InGaAs photodiodes. Each pixel is made up of an InGaAs photodiode and a ROIC electrically connected by an indium bump. A timing generator in the ROIC provides an analog video output and AD-TRIG output which are easily obtained by just supplying a master clock (MCLK) and master start pulse (MSP) from external digital inputs.
The G11097-0606S has 64×64 pixels arrayed at a 50 µm pitch and their signals are read out from a single video line. Light incident on the InGaAs photodiodes is converted into electrical signals which are then input to the ROIC through indium bumps. Electrical signals in the ROIC are converted into voltage signals by charge amplifiers and then sequentially output from the video line by the shift register. The G11097-0606S is hermetically sealed in a TO-8 package together with a one-stage thermoelectric cooler to deliver low-cost yet highly stable operation.

Features

- **Spectral response range: 0.95 to 1.7 µm**
- **Excellent linearity by offset compensation**
- **High sensitivity: 1600 nV/e⁻**
- **Simultaneous charge integration for all pixels (global shutter mode)**
- **Simple operation (built-in timing generator)**
- **One-stage TE-cooled**
- **Low cost**

Applications

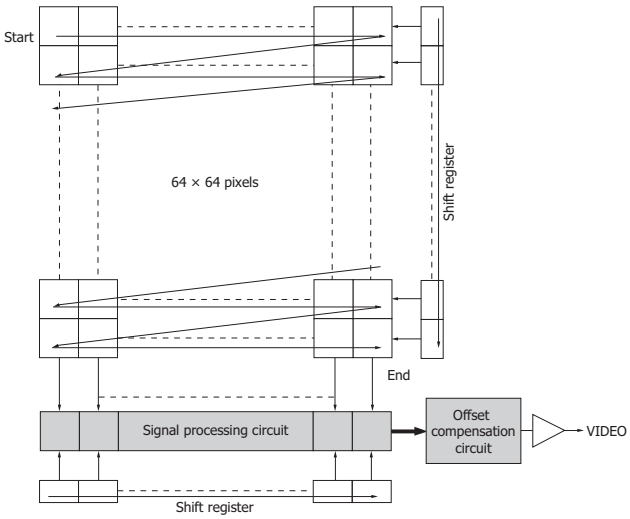
- **Thermal imaging monitor**
- **Laser beam profiler**
- **Near infrared image detection**
- **Foreign object detection**

Block diagram

A sequence of operation of the readout circuit is described below.
In the readout circuit, the charge amplifier output voltage is sampled and held simultaneously at all pixels during the integration time determined by the low period of the master start pulse (MSP) which is as a frame scan signal. Then the pixels are scanned and their video signals are output.
Pixel scanning starts from the starting point at the upper left in the right figure. The vertical shift register scans from top to bottom in the right figure while sequentially selecting each row.
For each pixel on the selected row, the following operations are performed:

① Transfers the sampled and held optical signal information to the signal processing circuit as a signal voltage.
② Resets the amplifier in each pixel after having transferred the signal voltage and transfers the reset voltage to the signal processing circuit.
③ The signal processing circuit samples and holds the signal voltage ① and reset voltage ②.
④ The horizontal shift register scans from left to right in the right figure, and the voltage difference between ① and ② is calculated in the offset compensation circuit. This eliminates the amplifier offset voltage in each pixel. The voltage difference between ① and ② is output as the output signal in the form of serial data.

The vertical shift register then selects the next row and repeats the operations from ① to ④. After the vertical shift register advances to the 64th row, the MSP, which is a frame scan signal, goes low. After that, when the MSP goes high and then low, the reset switches for all pixels are simultaneously released and the next frame integration begins.



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Element structure

Parameter	Specification	Unit
Image size	3.2 × 3.2	mm
Cooling	One-stage TE-cooled	-
Number of total pixels	4096 (64 × 64)	pixels
Number of effective pixels	4096 (64 × 64)	pixels
Pixel size	50 × 50	µm
Pixel pitch	50	µm
Package	TO-8 16-pin metal (refer to dimensional outline)	-
Window	Borosilicate glass with anti-reflective coating	-

Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage	Vdd	-0.3 to +5.5	V
Clock pulse voltage	V(MCLK)	Vdd + 0.5 max.	V
Operating temperature	Topr	-10 to +60	°C
Storage temperature	Tstg	-20 to +70	°C

Note: This product must be used within the range of the absolute maximum ratings. Product quality may suffer if any item of the absolute maximum ratings is exceeded even momentarily.

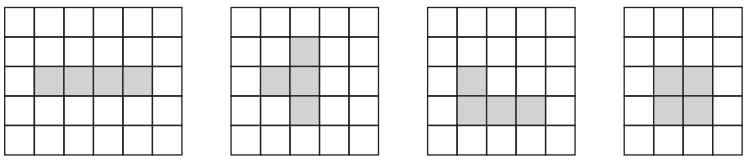
Electrical and optical characteristics (Element temperature=25 °C, Ta=25 °C, Vdd=5 V, PD_bias=4.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Spectral response range	λ		-	0.95 to 1.7	-	µm
Peak sensitivity wavelength	λp		-	1.55	-	µm
Photo sensitivity	S	λ=λp	0.7	0.8	-	A/W
Conversion efficiency	CE	Cf=0.1 pF	-	1600	-	nV/e^-
Saturation charge	Qsat		-	1.25	-	Me$^-$
Saturation output voltage	Vsat		-	2	-	V
Photo response non-uniformity*1	PRNU	After subtracting dark current, Integration time 5 ms	-	±10	±20	%
Dark voltage	VD		-	20	100	V/s
Dark current	ID		-	2	10	pA
Dark signal non-uniformity	DSNU		-	20	50	V/s
Readout noise	Nr	Integration time 10 ms	-	600	1200	µV rms
Dynamic range	DR		1600	3300	-	-
Defective pixel*2	-		-	-	1	%

*1: Measured at one-half of the saturation, excluding first and last pixels

*2: Pixels with photo response non-uniformity (integration time 5 ms), readout noise, or dark current higher than the maximum value
One or less cluster of four or more contiguous defective pixels

<Examples of four contiguous defective pixels>



Normal pixel

Defective pixel

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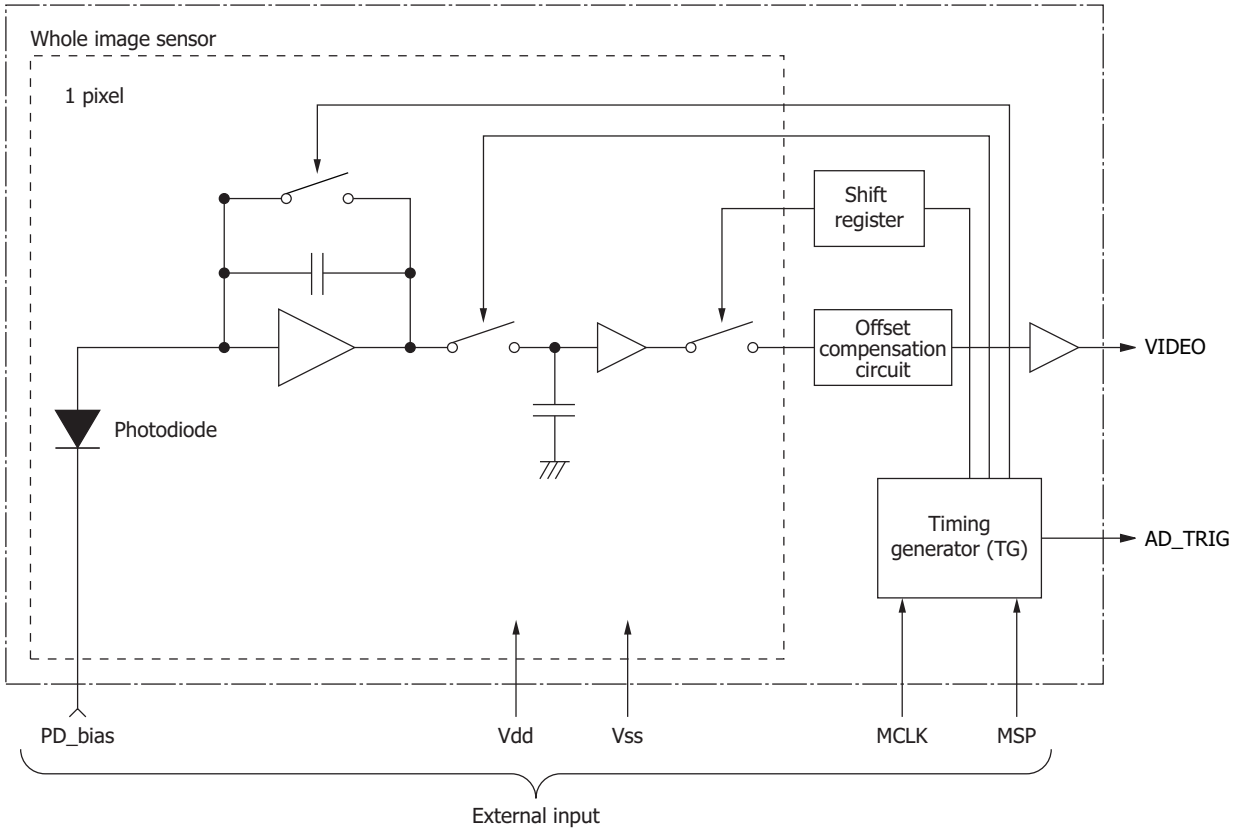
Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit.
Supply voltage		Vdd	4.9	5	5.1	V
Supply current		I(Vdd)	-	30	60	mA
Ground		Vss	-	0	-	V
Element bias		PD_bias	4.4	4.5	4.6	V
Element bias current		I(PD_bias)	-	-	1	mA
Clock frequency		f	-	-	40	MHz
Clock pulse voltage	High	V(MCLK)	Vdd - 0.5	Vdd	Vdd + 0.5	V
	Low		0	0	0.5	V
Clock pulse rise/fall times		tr(MCLK)	0	10	12	ns
		tf(MCLK)				
Clock pulse width		tpw(MCLK)	10	-	-	ns
Start pulse voltage	High	V(MSP)	Vdd - 0.5	Vdd	Vdd + 0.5	V
	Low		0	0	0.5	V
Start pulse rise/fall times		tr(MSP)	0	10	12	ns
		tf(MSP)				
Start pulse width		tpw(MSP)	1000	-	-	ns
Start (rise) timing		t1	10	-	-	ns
Start (fall) timing		t2	10	-	-	ns
Output setting time		t3	-	-	50	ns
Video output voltage	High	VH	-	3.2	-	V
	Low	VL	-	1.2	-	
Video data rate		fV	-	f/8	-	MHz

Equivalent circuit



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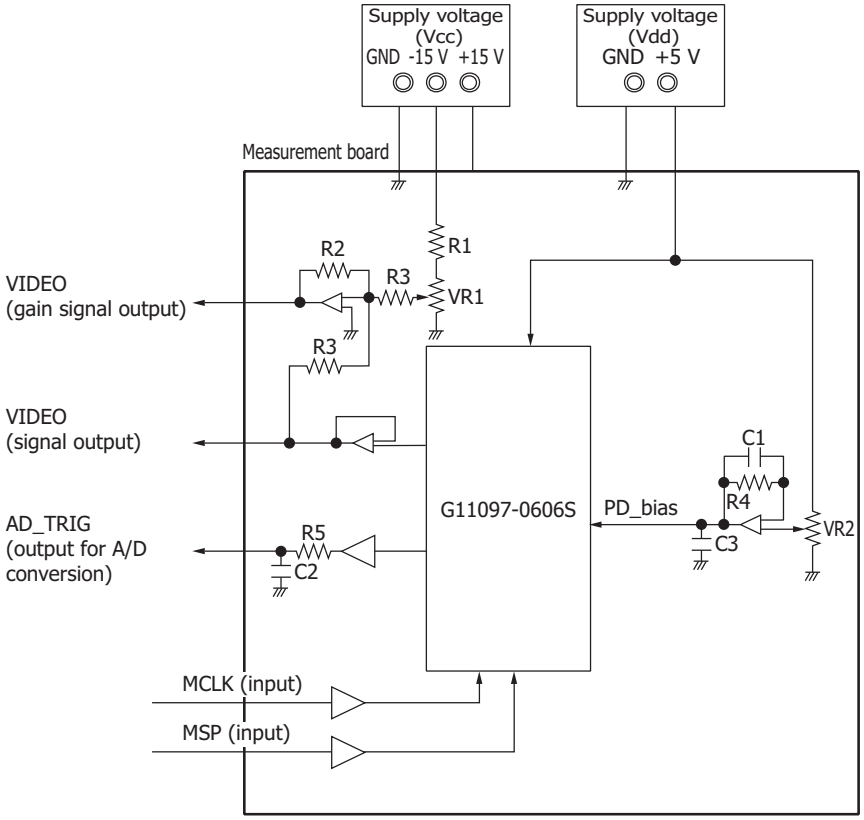
Connection example



(Reference) Parameter values

Symbol	Value
R1	2 kΩ
R2	5.1 kΩ
R3	1 kΩ
R4	10 kΩ
R5	10 Ω
VR1	10 kΩ
VR2	10 kΩ
C1	75 pF
C2	330 pF
C3	0.1 μF

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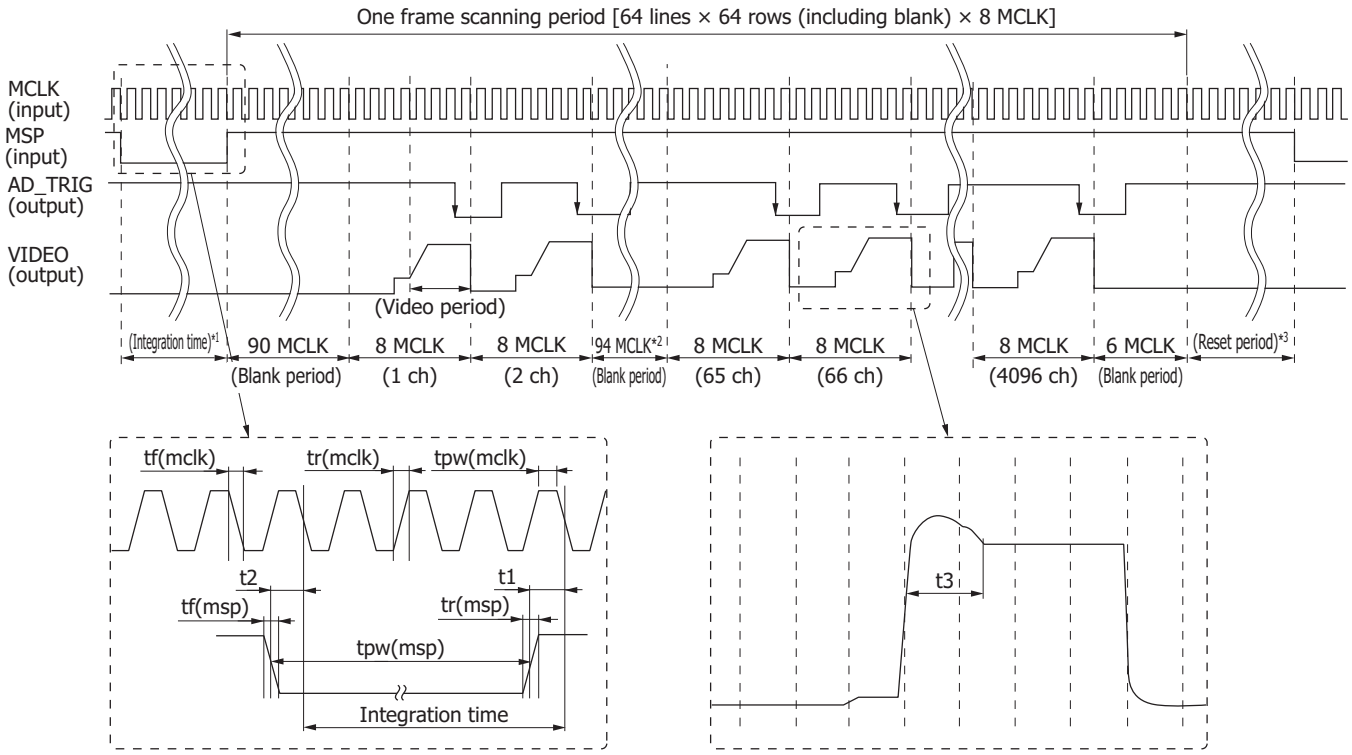
Timing chart

The video output from a single pixel is equal to 8 MCLK (master clock) pulses. The MSP (master start pulse) is a signal for setting the integration time, so making the low (0 V) period of the MSP longer will extend the integration time. The MSP also functions as a signal that triggers each control signal to perform frame scan. When the MSP goes from low (0 V) to high (5 V) , each control signal starts on the falling edge of the MCLK and frame scan is performed during the high period of the MSP.



*1 A minimum number of MCLK of integration time is 40 MCLK.
*2 There are blanks of 94 MCLK between each line.
*3 A minimum number of MCLK of reset period is 200 MCLK.

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Spectral response

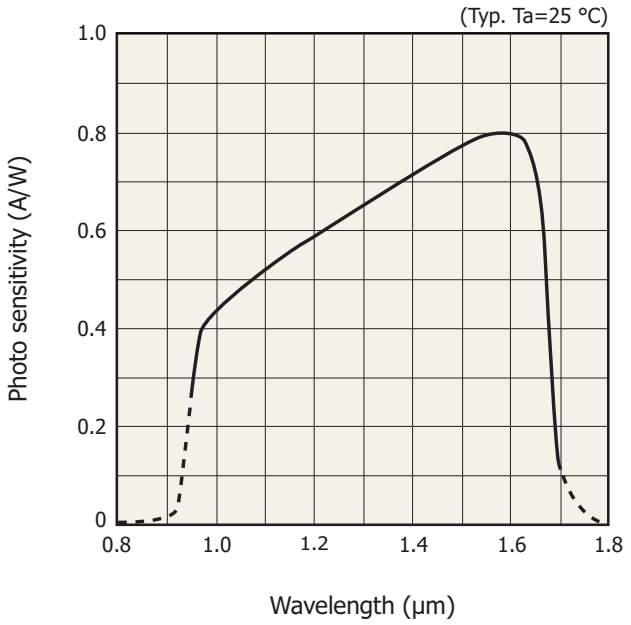
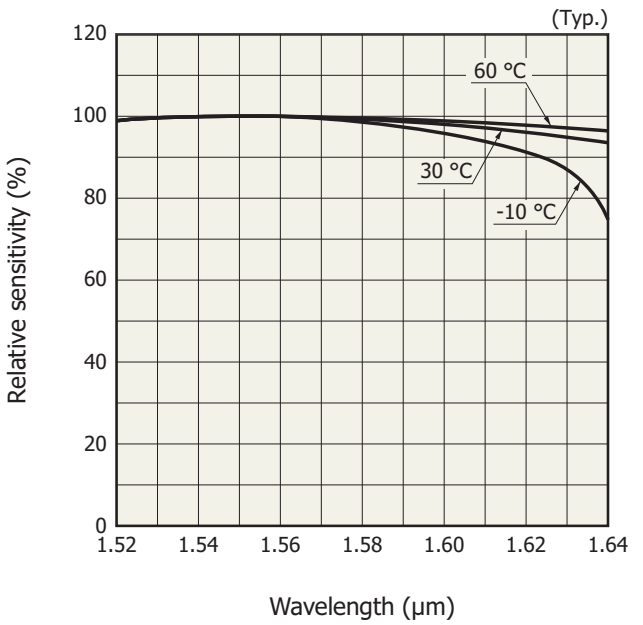


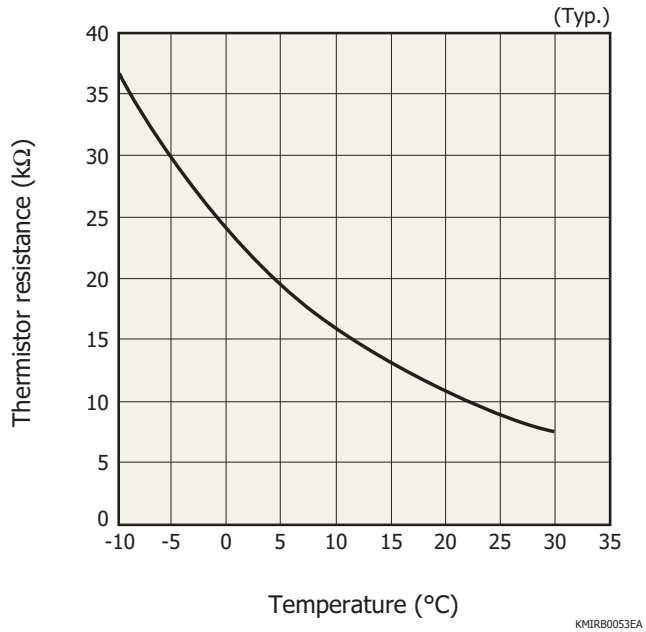
Photo sensitivity temperature characteristic



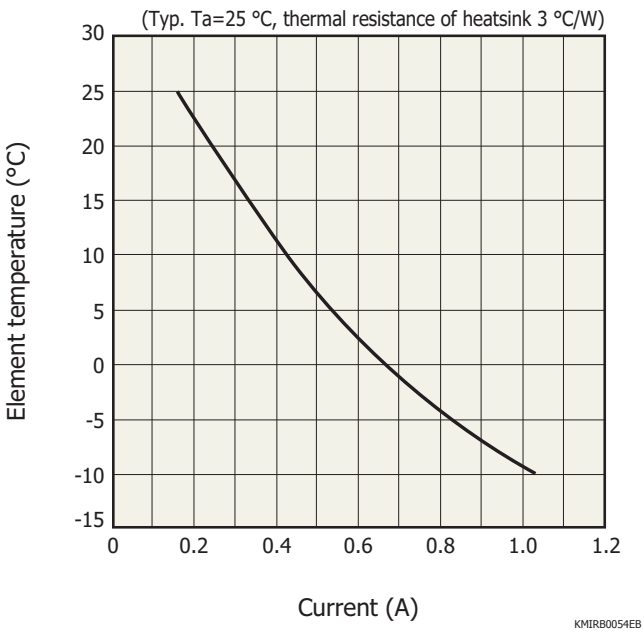
Specifications of one-stage TE-cooler (Ta=25 °C, Vdd=5 V, PD_bias=4.5 V)

Parameter	Symbol	Min	Typ	Max	Unit
TE-cooler allowable current	Ic	-	0.7	1.1	A
TE-cooler allowable voltage	Vc	-	1.0	1.5	V
Termistor resistance	Rth	8.8	9	9.2	kΩ
Termistor power dissipation	Pth	-	-	0.2	mW

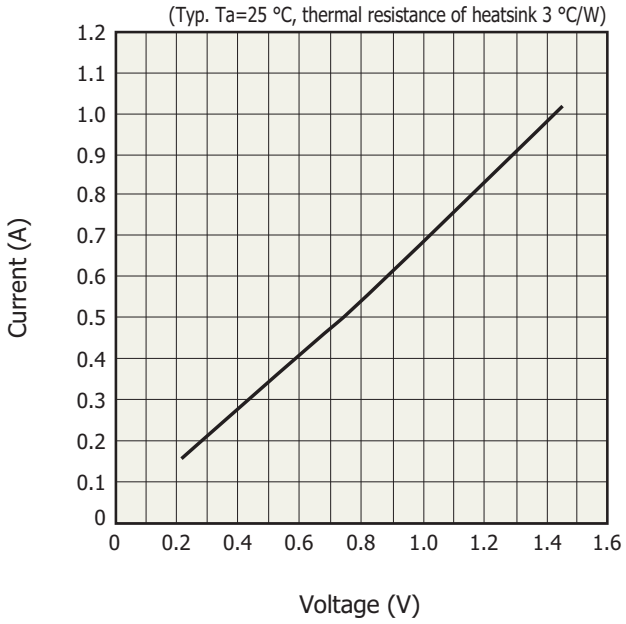
Thermistor temperature characteristic



Cooling characteristic of TE-cooler



Current vs. voltage (TE-cooler)



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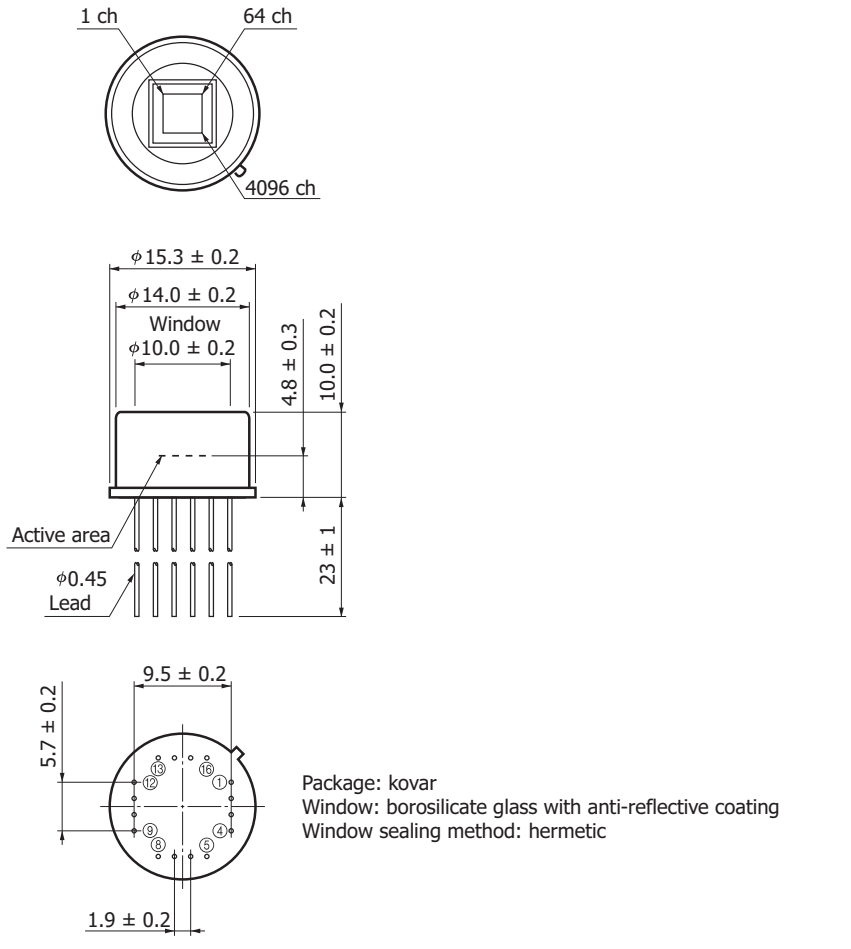
Dimensional outline (unit: mm)



Package: kovar
Window: borosilicate glass with anti-reflective coating
Window sealing method: hermetic

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Pin connections

Pin no.	Name	Input/Output	Function	Remark
1	Vss	Input	0 V ground	0 V
2	Vdd	Input	+5 V supply voltage	5 V
3	MCLK	Input	Clock pulse for timing generator	Falling synchronous pulse
4	AD_TRIG	Output	Signal for A/D sampling	Falling synchronous pulse
5	MSP	Input	Clock pulse for flame scan start	
6	NC	-	-	
7	NC	-	-	
8	Vdd	Input	+5 V supply voltage	5 V
9	PD_bias	Input	Photodiode bias voltage	4.5 V
10	NC	-	-	
11	NC	-	-	
12	VIDEO	Output	Video output	1.2 to 3.2 V
13	TE (-)	Input	TE-cooler (-)	
14	THERM	Output	Thermistor	
15	THERM	Output	Thermistor	
16	TE (+)	Input	TE-cooler (+)	

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