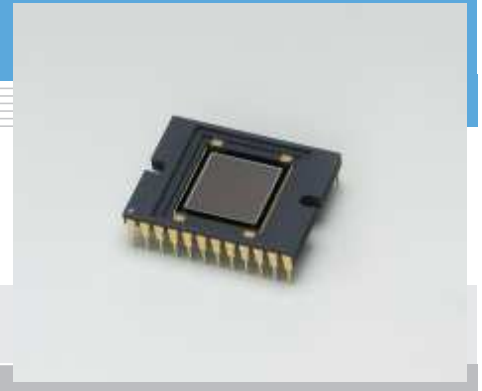


CCD area image sensor S9978

Front-illuminated FFT-CCDs, high IR sensitivity



S9978 is FFT-CCD area image sensor specifically designed for low-light-level detection in scientific applications. S9978 also features low noise and low dark current (MPP mode operation). These enable low-light-level detection and long integration time, thus achieving a wide dynamic range.

S9978 is pin compatible with S9736-01. (Operating conditions and characteristics are a little bit changed from S9736-01.)

Features

- High IR sensitivity
- 512 (H) × 512 (V) pixel format
- Pixel size: 24 × 24 μm
- 100 % fill factor
- Wide dynamic range
- Low dark current
- Low readout noise
- MPP operation

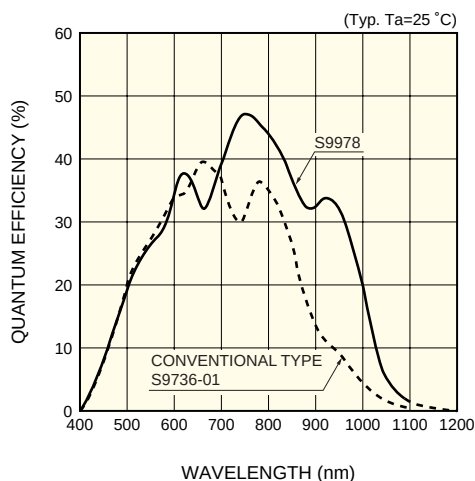
Applications

- Astronomy
- Scientific measuring instrument
- Fluorescence spectrometer
- Raman spectrophotometer
- Optical and spectrophotometric analyzer
- For low-light-level detection requiring

General ratings

Parameter	Rating
CCD structure	Full frame transfer
Fill factor	100 %
Number of active pixels	512 (H) × 512 (V)
Pixel size	24 (H) × 24 (V) μm
Active area	12.288 (H) × 12.288 (V) mm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	24-pin ceramic DIP
Window	None

Spectral response (without window)



■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	VOD	-0.5	-	+25	V
RD voltage	VRD	-0.5	-	+18	V
ISV voltage	VISV	-0.5	-	+18	V
ISH voltage	VISH	-0.5	-	+18	V
IGV voltage	VIG1V, VIG2V	-15	-	+15	V
IGH voltage	VIG1H, VIG2H	-15	-	+15	V
SG voltage	VSG	-15	-	+15	V
OG voltage	VOG	-15	-	+15	V
RG voltage	VRG	-15	-	+15	V
TG voltage	VTG	-15	-	+15	V
Vertical clock voltage	VP1V, VP2V	-15	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-15	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	18	20	22	V
Reset drain voltage		VRD	12	13	14	V
Output gate voltage		VOG	-0.5	0	2	V
Substrate voltage		VSS	-	0	-	V
Test point (vertical input source)		VISV	-	VRD	-	V
Test point (horizontal input source)		VISH	-	VRD	-	V
Test point (vertical input gate)		VIG1V, VIG2V	-8	0	-	V
Test point (horizontal input gate)		VIG1H, VIG2H	-8	0	-	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	0	4	6	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	0	4	6	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	0	4	6	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	0	4	6	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	0	4	6	V
	Low	VTGL	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	0.1	1	MHz
Vertical shift register capacitance	CP1V, CP2V	-	-	3500	-	pF
Horizontal shift register capacitance	CP1H, CP2H	-	-	60	-	pF
Summing gate capacitance	CSG	-	-	5	-	pF
Reset gate capacitance	CRG	-	-	5	-	pF
Transfer gate capacitance	CTG	-	-	70	-	pF
Transfer efficiency	CTE	*1	0.99995	0.99999	-	-
DC output level	Vout	*2	12	15	18	V
Output impedance	Zo	*2	-	3	-	kΩ
Power dissipation	P	*2, *3	-	15	-	mW

*1: Charge transfer efficiency per pixel, measured at half of the full well capacity.

*2: The values depend on the load resistance. (VOD=20 V, Load resistance=10 kΩ)

*3: Power dissipation of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	-	120	240	-	ke ⁻
	Horizontal			-	280	-	
CCD node sensitivity		Sv	*4	-	2.8	-	μV/e ⁻
Dark current (MPP mode)	+25 °C	DS	*5	-	1000	15000	e ⁻ /pixel/s
	0 °C			-	100	1500	
Readout noise		Nr	*6	-	4	18	e ⁻ rms
Dynamic range	Area scanning	-	*7	6667	60000	-	-
Spectral response range		λ	-	-	400 to 1100	-	nm
Photo response non-uniformity		PRNU	*8	-	-	±10	%
Blemish	Point defects	-	*9	-	-	0	-
	Cluster defects		*10	-	-	0	
	Column defects		*11	-	-	0	

*4: V_{OD}=20 V , Load resistance=10 kΩ

*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.

*6: -40 °C, operating frequency is 80 kHz.

*7: DR = Fw / Nr

*8: Measured at half of the full well capacity. PRNU = noise / signal × 100 [%], noise: fixed pattern noise (peak to peak)

*9: White spots > 3 % of full well at 0 °C after Ts=1 s

Black spots

Pixels whose sensitivity is lower than one-half of the average pixel output. (Measured with uniform light producing one-half of the saturation charge)

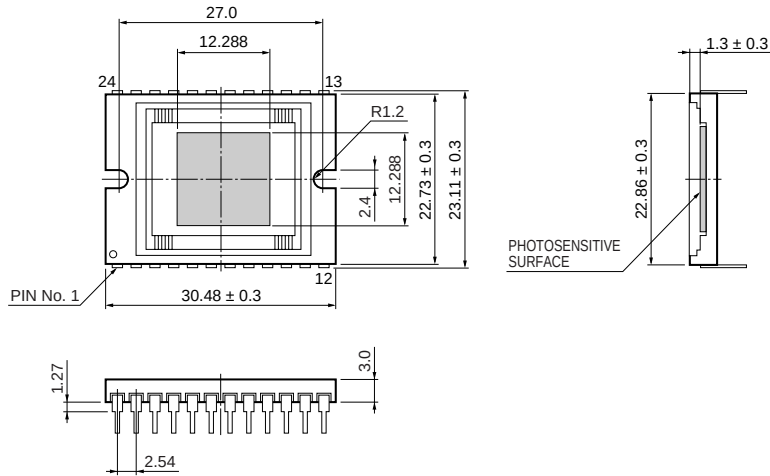
*10: 2 to 9 contiguous defective pixels

*11: 10 or more contiguous defective pixels

■ Pin connections

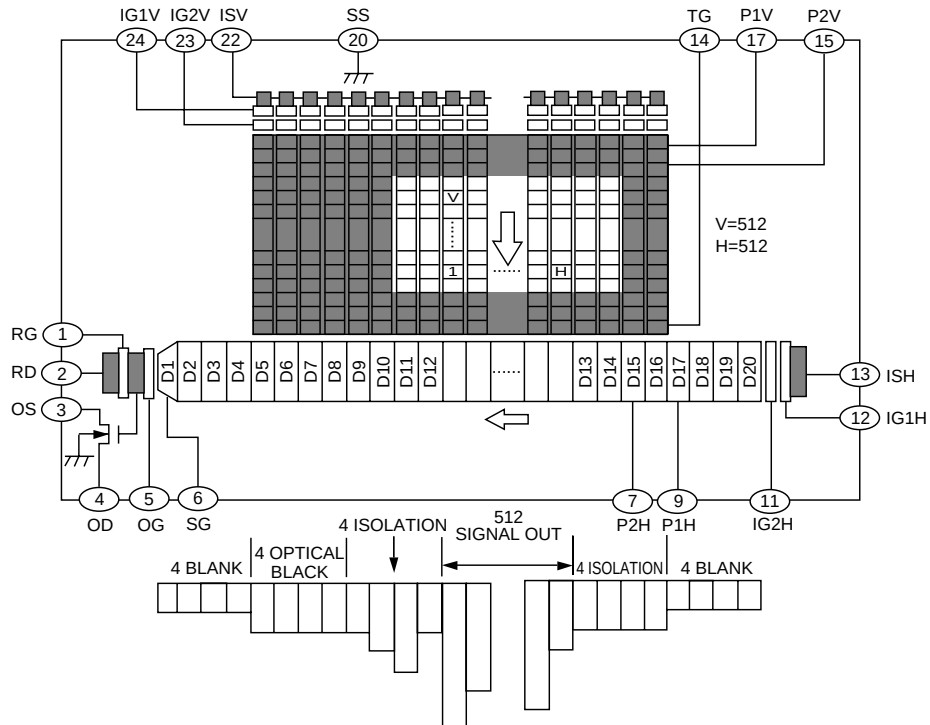
Pin No.	Symbol	Description	Remark
1	RG	Reset gate	-
2	RD	Reset drain	-
3	OS	Output source	-
4	OD	Output transistor drain	-
5	OG	Output gate	-
6	SG	Summing gate	-
7	P2H	CCD horizontal register clock-2	-
8	NC	No connection	-
9	P1H	CCD horizontal register clock-1	-
10	NC	No connection	-
11	IG2H	Test point (horizontal input gate-2)	Shorted to ground
12	IG1H	Test point (horizontal input gate-1)	Shorted to ground
13	ISH	Test point (horizontal input source)	Shorted to RD
14	TG	Transfer gate	-
15	P2V	CCD vertical register clock-2	-
16	NC	No connection	-
17	P1V	CCD vertical register clock-1	-
18	NC	No connection	-
19	NC	No connection	-
20	SS	Substrate (GND)	-
21	NC	No connection	-
22	ISV	Test point (vertical input source)	Shorted to RD
23	IG2V	Test point (vertical input gate-2)	Shorted to ground
24	IG1V	Test point (vertical input gate-1)	Shorted to ground

■ Dimensional outline (unit: mm)



KMPDA0140EB

■ Device structure, line output format



KMPDC0207EA

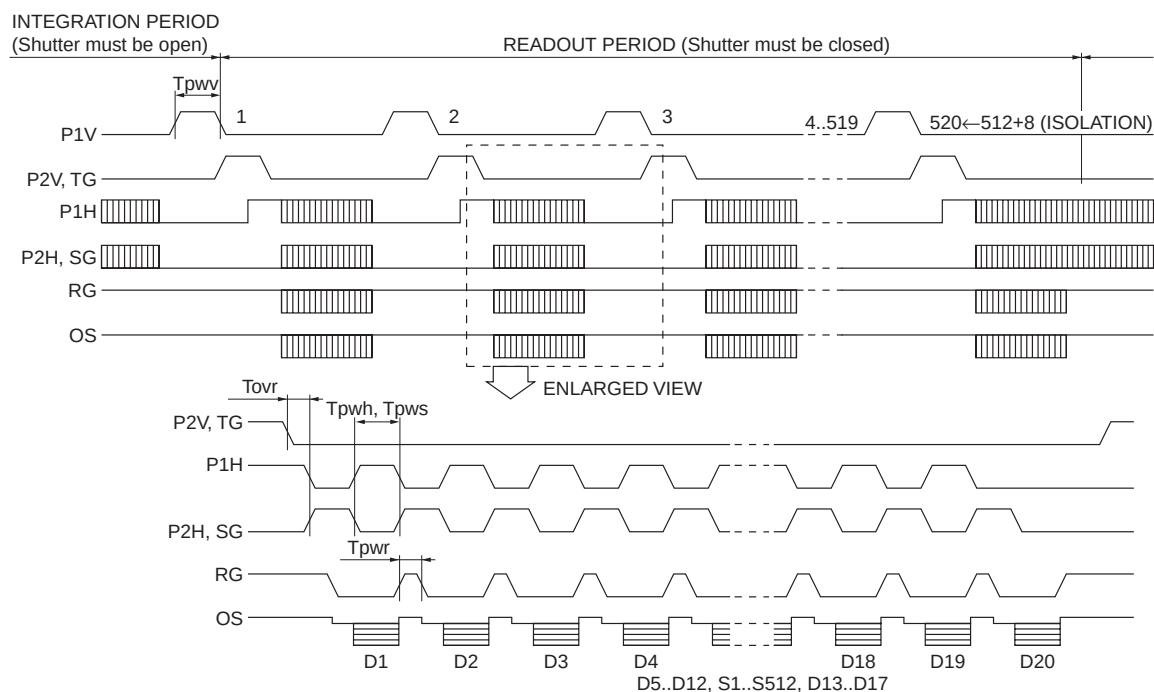
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	4	512	4	-	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
4	512	4

■ Timing chart

● Area scanning 1 (low dark current mode)

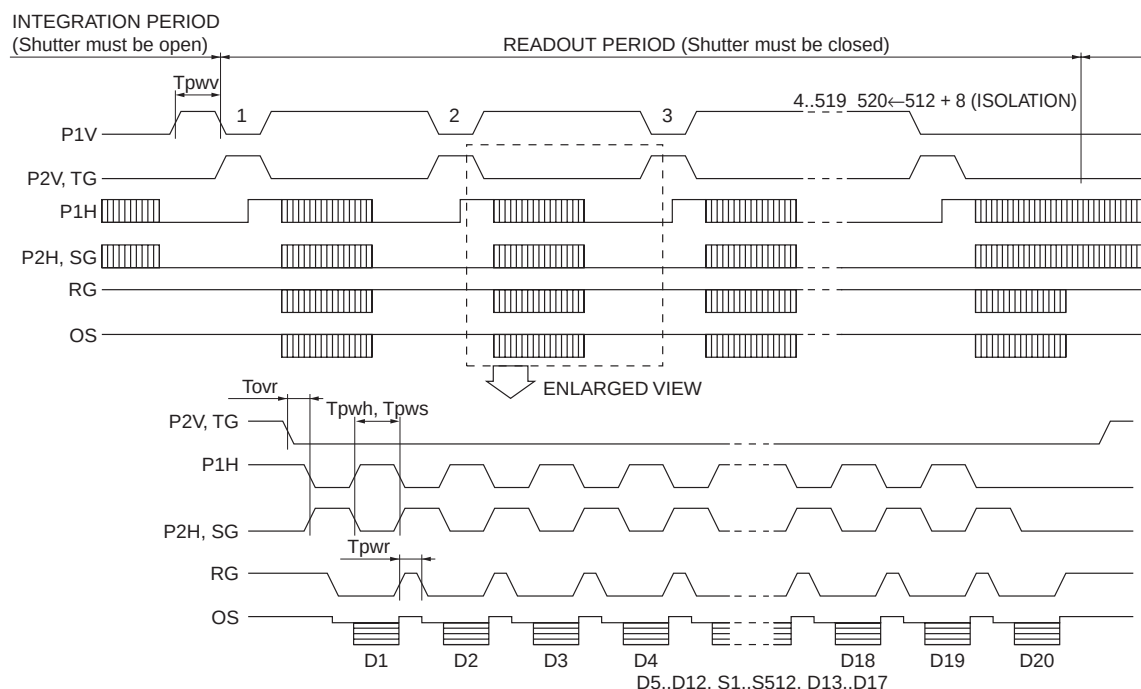


KMPDC0208EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V	Pulse width	Tpwv	*12	6	18	-	μs
P2V, TG	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*12	500	5000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	5000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	500	-	ns
	Rise and fall time	Tpr, Tprf		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	6	-	μs

*12: The clock pulses should be overlapped at 50 % of clock pulse amplitude.

● Area scanning 2 (large full well mode)



KMPDC0209EA

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V	Pulse width	Tpww	*13	6	18	-	μs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*13	500	5000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	5000	-	ns
	Rise and fall time	Tprs, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	500	-	ns
	Rise and fall time	Tpr, Tpfh		5	-	-	ns
TG – P1H		Tovr	-	3	6	-	μs

*13: The clock pulses should be overlapped at 50 % of clock pulse amplitude.

■ Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist strap, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

When cooling the CCD by an externally attached cooler, set the cooler operation so that the temperature gradient (rate of temperature change) for cooling or allowing the CCD to warm back is less than 5 K/minute.

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