

**FM1110****Nonvolatile 5V Quad State Saver****Features****Nonvolatile State Saver**

- Logic States Retained in Absence of Power
- Outputs Automatically Restored at Power-up
- Number of State Changes:  $10^{12}$
- Max  $t_{PD}$  50ns at 4.5V
- Max Frequency 1 MHz

**Low Power Operation**

- Supply voltage of 4.5V to 5.5V
- 30  $\mu$ A Standby Current

**Industry Standard Configuration**

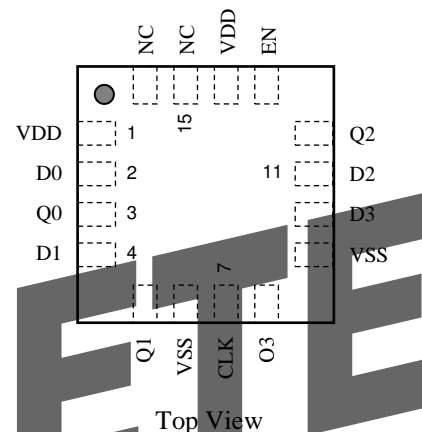
- Industrial Temperature  $-40^{\circ}$  C to  $+85^{\circ}$  C
- 16-pin “Green”/RoHS QFN Package

**Overview**

The FM1110 is an innovative FRAM-based device that stores inputs like conventional logic and retains the stored state in the absence of power. This product solves three basic problems in an elegant fashion. First, it provides continuous access to nonvolatile system settings without performing a memory read operation or using dedicated processor I/O pins. Second, it allows the storage of signals that may change frequently and possibly without notice. Third, it allows the nonvolatile storage of a system setting without the system overhead and extra pins of a serial memory.

Functionally, the inputs are stored and passed to the output on the rising edge of the clock CLK. This unique product serves a variety of applications. Here are a few applications:

- Control relays or valves with automatic setting on power-up without processor intervention
- Interface to soft/momentary front-panel switch and indicator lamp. Capture switch settings and drive LEDs without processor intervention
- Replaces jumpers & control signal routing
- Initialize state of I/O card signals
- Eliminate the overhead of serial memory for systems needing only a bit of data

**Pin Configuration**

Pin Names	Function
$D_N$	Data In
$Q_N$	Data Out
EN	Enable
CLK	Clock
VDD	Supply Voltage
VSS	Ground

**Ordering Information**

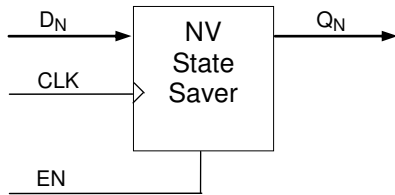
FM1110-QG	Quad State Saver, 16-pin “Green”/RoHS QFN
FM1110-QGTR	Quad State Saver, 16-pin “Green”/RoHS QFN, Tape and Reel

This is a product in the pre-production phase of development. Device characterization is complete and Ramtron does not expect to change the specifications. Ramtron will issue a Product Change Notice if any specification changes are made.

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Block Diagram and Truth Table



INPUTS			OUTPUT Q <sub>N</sub>
EN	CLK	D <sub>N</sub>	
H	↑	L	L
H	↑	H	H
H	H or L	X	Q <sub>0</sub>
L	X	X	Hi-Z

L Low voltage level  
 H High voltage level  
 X Don't Care  
 ↑ CLK rising edge  
 Q<sub>0</sub> Previous output state before CLK ↑

Pin Descriptions

Pin Name	I/O	Description
D(3:0)	I	Data inputs
Q(3:0)	O	Data outputs
CLK	I	Clock: On a rising edge of CLK, the D <sub>N</sub> inputs are transferred to the Q <sub>N</sub> outputs. While CLK is high or low, the Q <sub>N</sub> outputs do not change regardless of the state of the data inputs. See truth table.
EN	I	Enable. This active-high input enables the device. When low, inputs are ignored and updates to the nonvolatile cells are prevented. When high, the device operates normally.
VDD	Supply	Power Supply (4.5V to 5.5V)
VSS	Supply	Ground

## Description

Nonvolatile storage applied to logic is a revolutionary concept. The FM1110 simplifies the design of system control functions. This product is unique because it remembers the stored output values in the absence of power. Any change in the latched state is automatically written to a nonvolatile ferroelectric latch. This function is possible due to the fast write time and extremely high write endurance of the underlying ferroelectric memory technology.

## Use of Enable Pin

The FM1110 has an enable pin that is intended to be used in conjunction with a system reset. An active-low reset may be tied directly to the EN pin. At power-up, /RESET will be held low for some time during which the data input and CLK pins will be ignored. Once the system comes out of reset and EN goes high, the outputs  $Q_N$  drive to the state that were previously latched and the device operates normally. When the EN pin is low, the outputs  $Q_N$  are tri-stated.

The enable pin may be tied to  $V_{DD}$  since the device integrates a power management circuit that monitors the  $V_{DD}$  level during power cycles.

**OBSOLETE**

## Electrical Specifications

### Absolute Maximum Ratings

Symbol	Description	Ratings
V <sub>DD</sub>	Power Supply Voltage with respect to V <sub>SS</sub>	-1.0V to +7.0V
V <sub>IN</sub>	Voltage on any signal pin with respect to V <sub>SS</sub>	-1.0V to +7.0V and V <sub>IN</sub> < V <sub>DD</sub> +1.0V
T <sub>STG</sub>	Storage temperature	-55°C to +125°C
T <sub>LEAD</sub>	Lead temperature (Soldering, 10 seconds)	300° C
V <sub>ESD</sub>	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A) - Machine Model (JEDEC Std JESD22-A115-A)	4kV 1kV 200V
	Package Moisture Sensitivity Level	MSL-1

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

### DC Operating Conditions (T<sub>A</sub> = -40° C to +85° C, V<sub>DD</sub> = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V	
I <sub>SB</sub>	Standby Current		-	30	μA	1
C <sub>PD</sub>	Power Dissipation Capacitance		-	330	pF	2
I <sub>LI</sub>	Input Leakage Current			±1	μA	3
I <sub>LO</sub>	Output Leakage Current			±1	μA	3
V <sub>IL</sub>	Input Low Voltage	-0.3		0.3 V <sub>DD</sub>	V	
V <sub>IH</sub>	Input High Voltage	0.7 V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V	
V <sub>OH</sub>	Output High Voltage @ I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 0.5		-	V	
V <sub>OL</sub>	Output Low Voltage @ I <sub>OL</sub> = 1 mA (V <sub>DD</sub> =4.5V) @ I <sub>OL</sub> = 10 mA (V <sub>DD</sub> =4.5V)	-		0.4 0.8	V V	
V <sub>HYS</sub>	Input Hysteresis (CLK, EN)	150			mV	4

#### Notes

1. CLK = V<sub>SS</sub>, all other inputs at V<sub>DD</sub> or V<sub>SS</sub>.
2. To calculate device power dissipation, P<sub>D</sub> = C<sub>PD</sub>\*V<sub>DD</sub><sup>2</sup>\*f<sub>i</sub> + C<sub>L</sub>\*V<sub>DD</sub><sup>2</sup>\*f<sub>o</sub>, where f<sub>i</sub> is the input clk freq, f<sub>o</sub> is the output freq, and C<sub>L</sub> is the output load capacitance. Active current I<sub>DD</sub> may be calculated as I<sub>DD</sub> = C<sub>PD</sub>\*V<sub>DD</sub>\*f<sub>i</sub>, assuming outputs are floating.
3. V<sub>IN</sub> or V<sub>OUT</sub> = V<sub>SS</sub> to V<sub>DD</sub>.
4. This parameter is characterized but not tested.

**AC Parameters** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$ ,  $C_L = 30\text{pF}$  unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
$f_{MAX}$	Maximum Clock Frequency		1	MHz	
$t_{LOW}$	CLK Low Period	0.3		$\mu\text{s}$	
$t_{HIGH}$	CLK High Period	0.3		$\mu\text{s}$	
$t_{PD}$	Propagation delay CLK to $Q_N$		50	ns	
$t_{HZ}$	EN Low to $Q_N$ Hi-Z		25	ns	1
$t_R$	Input Rise Time		100	ns	1
$t_F$	Input Fall Time		100	ns	1
$t_{DS}$	Data ( $D_N$ ) Setup Time to CLK $\uparrow$	5		ns	
$t_{DH}$	Data ( $D_N$ ) Hold Time after CLK $\uparrow$	10		ns	
$t_{EHD}$	EN Hold Time (EN High after CLK $\uparrow$ )	50	-	ns	
$t_{EH}$	EN High Time	5		$\mu\text{s}$	
$t_{EL}$	EN Low Time	2		$\mu\text{s}$	

**Notes**

1. This parameter is characterized but not tested.

**Power Cycling and Data Retention** ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$ , unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
	Nonvolatile Data Retention Time	45	-	years	
$t_{VDR}$	$V_{DD}$ Rise Time	25	-	$\mu\text{s}/\text{V}$	1
$t_{VDF}$	$V_{DD}$ Fall Time	50	-	$\mu\text{s}/\text{V}$	1
$t_{RES}$	EN High to $Q_N$ Restore Time	-	0.5	$\mu\text{s}$	2
$t_{PDS}$	EN Low to Power Down Time	1	-	$\mu\text{s}$	
$t_{EHFC}$	EN High to First Clock (CLK $\uparrow$ ) after Power Up	4	-	$\mu\text{s}$	3

**Notes**

1. Slope measured at any point on  $V_{DD}$  waveform.
2. After power up, when EN goes high the nonvolatile latches are read and the values restored to the outputs  $Q_N$ .
3. After power up, this is the minimum time required before a state change operation may occur. EN and  $V_{DD}$  may be coincident at power up, and in this case  $t_{EHFC}$  time is referenced to  $V_{DD}$  (min) and CLK  $\uparrow$ .

**Capacitance** ( $T_A = 25^\circ\text{C}$ ,  $f=1.0\text{MHz}$ ,  $V_{DD} = 5.0\text{V}$ )

Symbol	Parameter	Min	Max	Units	Notes
$C_I$	Input Capacitance	-	14	pF	1

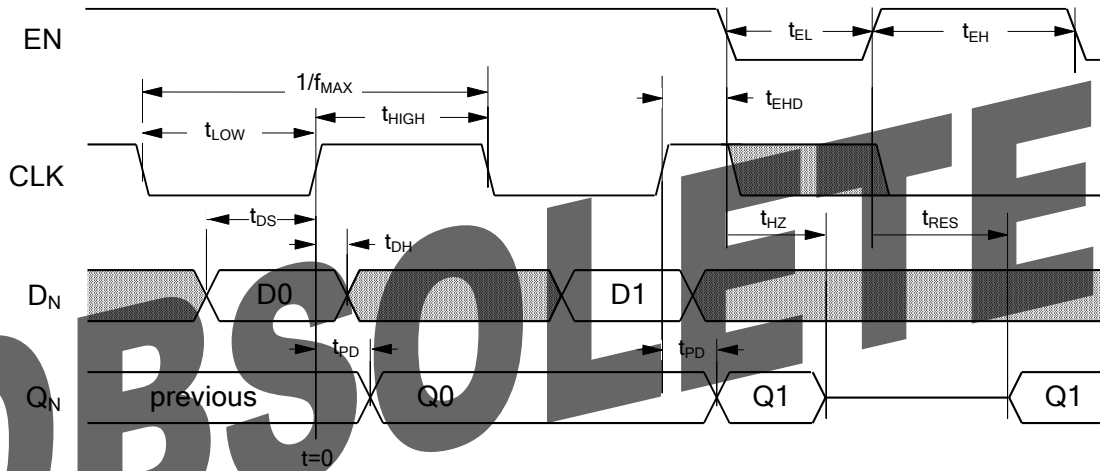
**Notes**

1. This parameter is characterized but not tested.

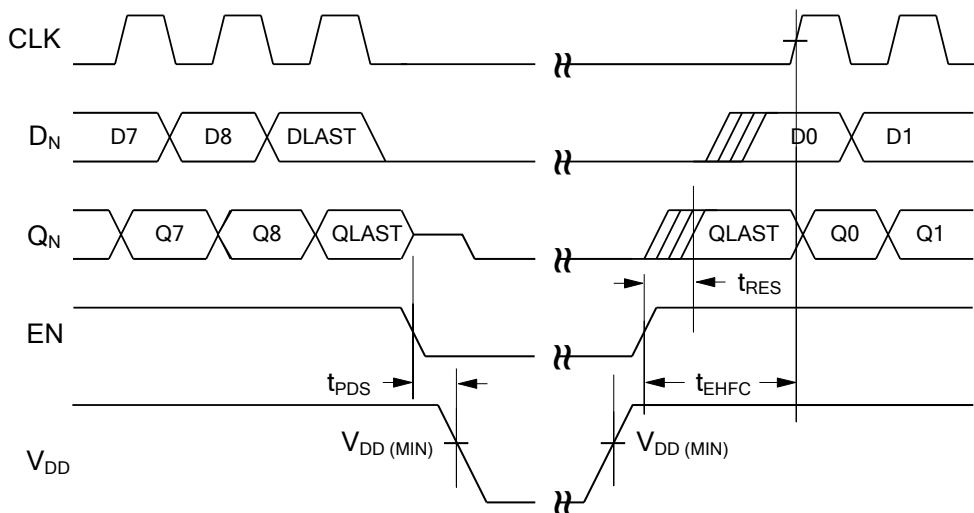
AC Test Conditions

Input Pulse Levels	0.1 V <sub>DD</sub> to 0.9 V <sub>DD</sub>
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.5 V <sub>DD</sub>
Output Load Capacitance	30pF

FM1110 Signal Timing



Power Cycle Timing





**Revision History**

Revision	Date	Summary
1.0	8/8/2007	Initial Release.
2.0	2/20/2008	Changed to Pre-Production status. Changed $V_{HYS}$ and $t_{EHD}$ (min.) limits.
2.1	5/4/2010	Added PCB footprint to mechanical drawing. Added ESD and MSL ratings.
4.0	4 <sup>th</sup> Oct 2012	Added obsolete text

**OBSOLETE**