

AM42-0007-DIE

GaAs MMIC Power Amplifier, 2.0 W
14.0 - 14.5 GHz

Rev. V6

Features

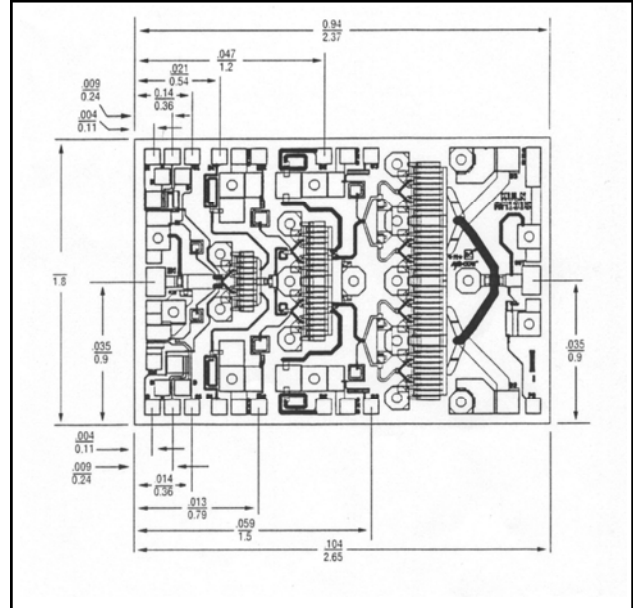
- High Linear Gain: 22 dB Typical.
- High Saturated Output Power: +33 dBm Typical
- High Power Added Efficiency: 22% Typical
- High P1dB: +32 dBm Typical
- 50 Ω Input / Output Broadband Matched
- Integrated Output Power Detector
- High Performance Ceramic Bolt Down Package

Description

The AM42-0007-DIE is a three stage MMIC linear power amplifier fabricated on a mature 0.5 micron MBE based GaAs process. The AM42-0007-DIE employs a fully matched chip with integral bias networks and output power detector.

This GaAs MMIC power amplifier is ideally suited for used as an output stage or driver in applications for VSAT applications.

Functional Schematic



Ordering Information

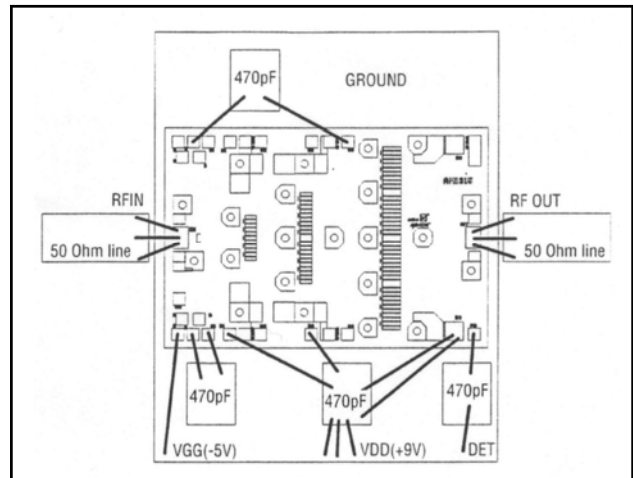
Part Number	Package
AM42-0007-DIE	DIE

Absolute Maximum Ratings^{1,2}

Parameter	Absolute Maximum
V _{DD}	+12 Volts
V _{GG}	-10 Volts
Power Dissipation	17.9 W
RF Input Power	+23 dBm
Channel Temperature	+150 °C
Storage Temperature	-65 °C to +150 °C

1. Exceeding any one or combination of these limits may cause permanent damage to this device.
2. Back of die temperature (T_B) = +25°C.

Typical Bias Configuration^{3,4}



3. Nominal bias is obtained by first connecting -5 volts to pin V_{GG} (resistor network used) followed by connecting +9 volts to pin V_{DD}. Note sequence.
4. It is recommended that the die be mounted with Au/Sn eutectic performs for good RF ground and thermal interface.

Electrical Specifications⁵: $T_B = +25^\circ\text{C}$, $V_{DD} = +9\text{ V}$, $V_{GG} = -1.2\text{V}$, $Z_0 = 50\ \Omega$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Linear Gain	$P_{IN} < 0\text{ dBm}$	dB	—	22	—
Input VSWR	—	Ratio	—	2.5:1	—
Output VSWR	—	Ratio	—	2.7:1	—
Saturated Output Power	$P_{IN} < +14\text{ dBm}$	dBm	—	+33	—
Output Power @ 1 dB Compression	—	dBm	31	+32	—
Output IP_3	—	dBm	—	41	—
Power Added Efficiency (PAE)	$P_{IN} < +14\text{ dBm}$	%	—	22	—
Bias Current	I_{DSQ} (No RF) I_{GG} (No RF)	mA mA	—	850 0.1	—
Thermal Resistance	θ_{CB2} ⁶	$^\circ\text{C/W}$	—	7	—
Detector Output Voltage (V_{DET})	$P_{in} = +3\text{ dBm}$, $I_{ds} = 750\text{ mA Typ.}$	V	—	+3.5	—

5. 100% on wafer tested (50 μs pulse width, 20% duty factor) without resistor network on gates.

6. Channel to die backside.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

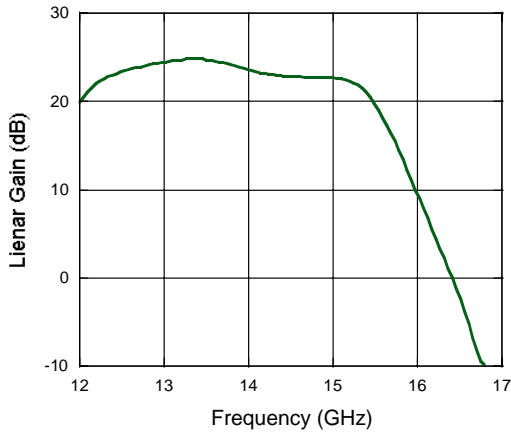
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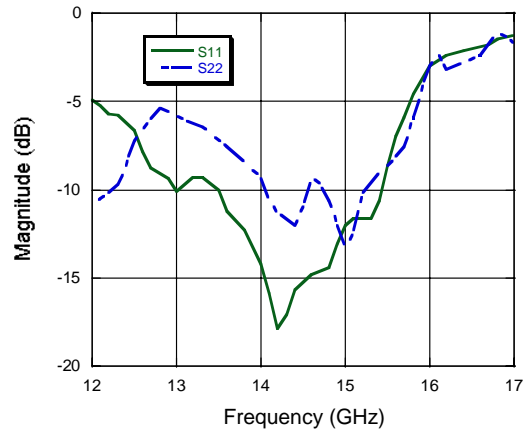
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Typical Performance @ 25°C

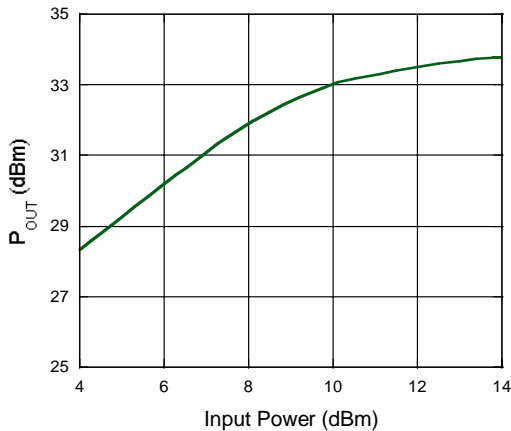
Linear Gain vs. Frequency



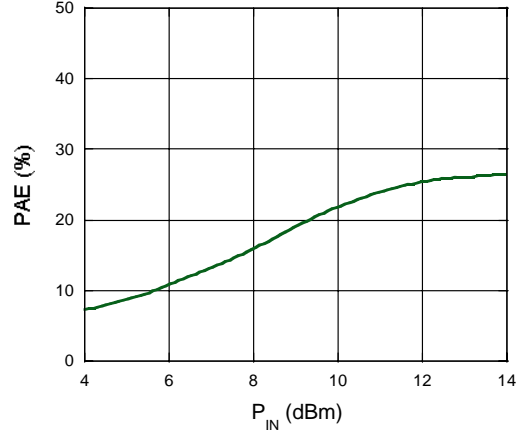
Input & Output Return Loss vs. Frequency



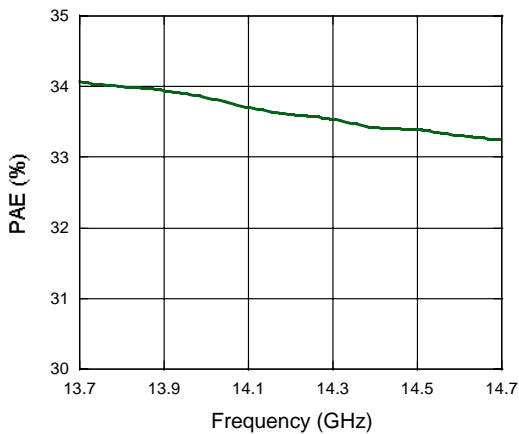
Output Power vs. Input Power @ 14 GHz



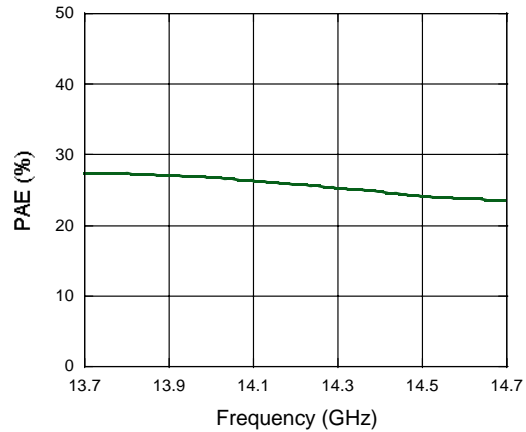
Power Added Efficiency vs. Input Power @ 14 GHz



Output Power vs. Frequency @ P_{IN} = +14 dBm



PAE vs. Frequency @ P_{IN} = +14 dBm



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