XU1010-QH

Up Converter
17.0-34.0 GHz

Rev. V2

Mimix Broadband

Features

- Integrated Balanced Mixer, LO Buffer and LO Doubler
- +23.0 dBm Input Third Order Intercept (IIP3)
- +2.0 dBm LO Drive Level
- 4x4mm QFN Package
- 100% RF and DC Testing
- RoHS* Compliant and 260°C Reflow Compatible

Description

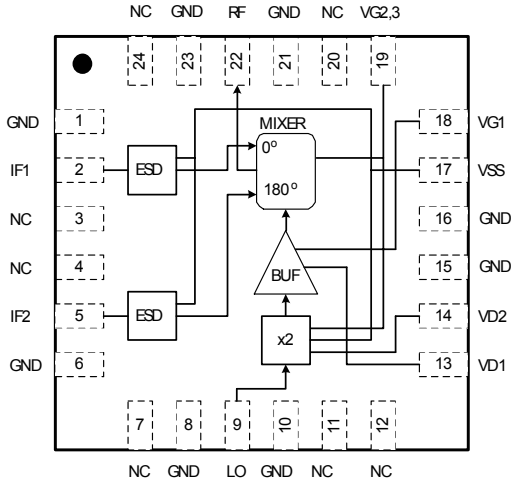
M/A-COM Tech's 17.0-34.0 GHz GaAs packaged up-converter has an input third order intercept point of +23.0 dBm and 10.0 dB of conversion loss. The device consists of a balanced resistive pHEMT mixer, LO buffer amplifier and LO doubler packaged in an industry standard, fully molded 4x4mm QFN package. IF and *IF mixer inputs are provided and an external 180 degree hybrid is required. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part. This device is well suited for Millimeter-wave Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Absolute Maximum Ratings[1]

Parameter	Absolute Max.
Drain Voltage Supply (Vdd)	+4.3 V
Drain Current (Ids)	350 mA
Input Power (Pin) IF	+5 dBm
Input Power (Pin) LO	+10 dBm
Storage Temperature (Tstg)	-65 °C to +165 °C
Operating Temperature (Tb)	-55 °C to +85 °C
ESD Min. - Machine Model (MM)	Class A
ESD Min. - Human Body Model (HBM)	Class 0
MSL Level	MSL3

(1) Operation of this device above any one of these parameters may cause permanent damage.

Functional Block Diagram



Pin Configuration

Pin No.	Function	Pin No.	Function
1	Ground	14	LO Doubler Drain
2	IF1 Input	15-16	Ground
3-4	Not Connected	17	Doubler/ESD Bias
5	IF2 Input	18	LO Buffer Gate
6-8	Ground	19	LO Doubler/ Mixer Gate
7	Not Connected	20	Not Connected
8	Ground	21	Ground
9	LO Input	22	RF Input
10	Ground	23	Ground
11-12	Not Connected	24	Not Connected
13	LO Buffer Drain		

Ordering Information

Part Number	Package
XU1010-QH-0G00	bulk quantity
XU1010-QH-0G0T	tape and reel
XU1010-QH-EV1	evaluation module

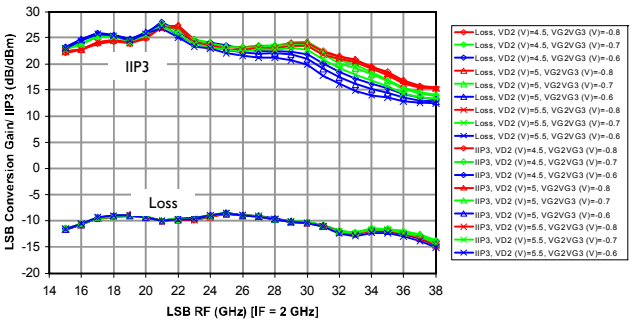
• **North America** Tel: 800.366.2266 • **Europe** Tel: +353.21.244.6400
• **India** Tel: +91.80.43537383 • **China** Tel: +86.21.2407.1588
Visit www.macomtech.com for additional data sheets and product information.

Electrical Specifications: 17-34 GHz (RF) (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (RF)	GHz	17		34
Frequency Range (LO)	GHz	8		20
Frequency Range (IF)	GHz	DC		3.5
Conversion Loss (CL)	dB		10	
Input Third Order Intercept (IIP3)	dBm		23	
LO Input Drive	dBm		2	
RF Input Return Loss	dB		15	
LO Input Return Loss	dB		15	
IF Input Return Loss	dB		15	
2xLO Leakage at RF	dBm		-20	
1xLO Leakage at RF	dBm		-30	
Drain Bias Voltage (Vd1,2)	VDC		4.0	
Gate Bias Voltage (Vg1)	VDC		~ -0.2	
Gate Bias Voltage (Vg2,3)	VDC		-0.8	
Gate Bias Voltage (Vss)	VDC		-4.0	
Supply Current (Id1)	mA		130	
Supply Current (Id2)	mA		~ 60	
Supply Current (Iss)	mA		45	

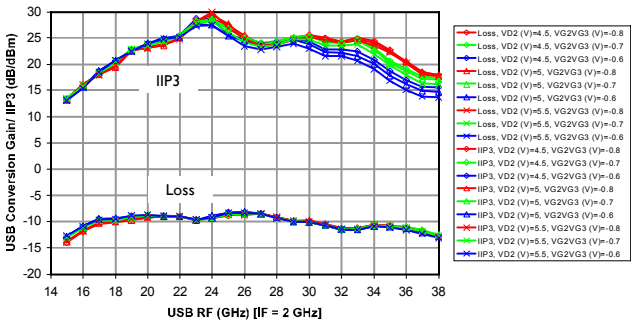
Typical Performance Curves

XU1010-QH, Glob Top, R10C2: LSB Conversion Loss & IIP3 vs. RF, PLO = 2 dBm, PIFscl = 0 dBm, IF1 - IF2 = 10 MHz, Doubler and Mixer bias swept



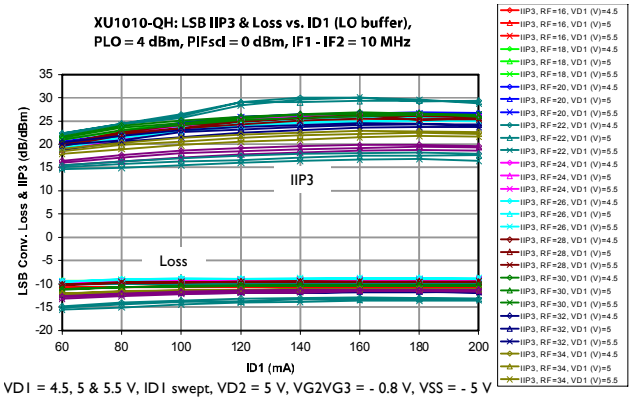
VD1 = 5 V, ID1 = 140 mA, VD2 = 5 V, VG2VG3 = - 0.8 V, VSS = - 5 V

XU1010-QH, Glob Top, R10C2: USB Conversion Loss & IIP3 vs. RF, PLO = 2 dBm, PIFscl = 0 dBm, IF1 - IF2 = 10 MHz, Doubler and Mixer bias swept



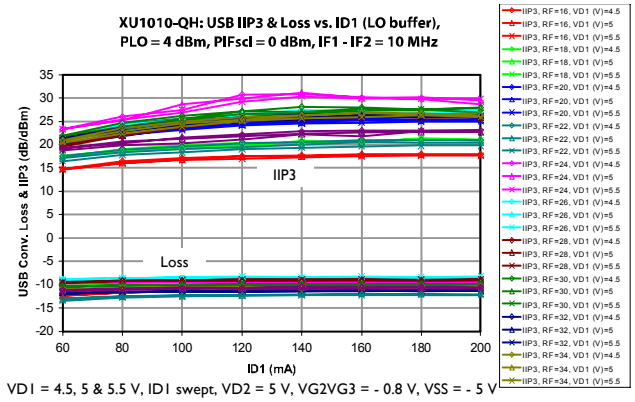
VD1 = 5 V, ID1 = 140 mA, VD2 = 5 V, VG2VG3 = - 0.8 V, VSS = - 5 V

XU1010-QH: LSB IIP3 & Loss vs. ID1 (LO buffer), PLO = 4 dBm, PIFscl = 0 dBm, IF1 - IF2 = 10 MHz



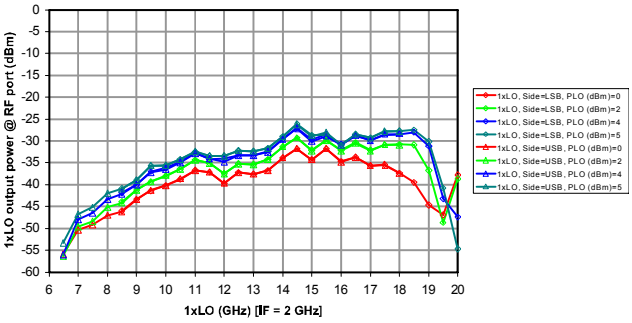
VD1 = 4.5, 5 & 5.5 V, ID1 swept, VD2 = 5 V, VG2VG3 = - 0.8 V, VSS = - 5 V

XU1010-QH: USB IIP3 & Loss vs. ID1 (LO buffer), PLO = 4 dBm, PIFscl = 0 dBm, IF1 - IF2 = 10 MHz



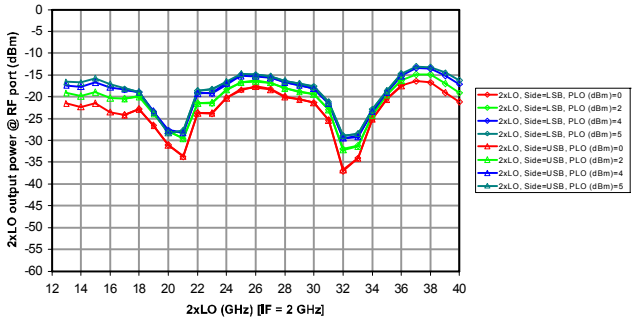
VD1 = 4.5, 5 & 5.5 V, ID1 swept, VD2 = 5 V, VG2VG3 = - 0.8 V, VSS = - 5 V

XU1010-QH, Glob Top, R10C2: 1xLO output power @ RF port, PLOswp, PIFscl = 0 dBm, IF1 - IF2 = 10 MHz



VD1 = 5 V, ID1 = 140 mA, VD2 = 5 V, VG2VG3 = - 0.8 V, VSS = - 5 V

XU1010-QH, Glob Top, R10C2: 2xLO output power @ RF port, PLOswp, PIFscl = 0 dBm, IF1 - IF2 = 10 MHz



VD1 = 5 V, ID1 = 140 mA, VD2 = 5 V, VG2VG3 = - 0.8 V, VSS = - 5 V

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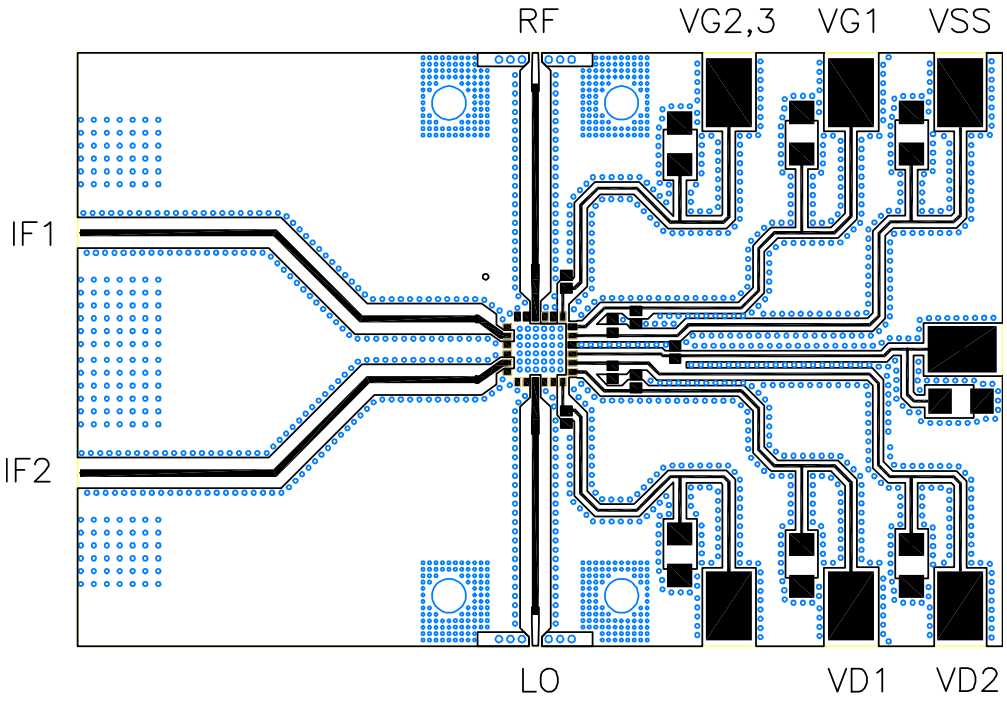
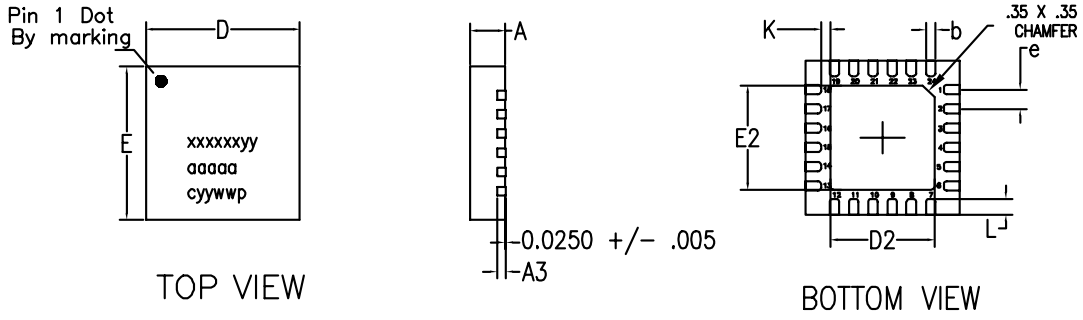
App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing VD1 and VD2 at 4.0 V with 130 mA and approximately 60 mA respectively. VG2,3 and VSS require fixed voltage biasing with VSS biased at -4.0 V and 45 mA. It is recommended to use active bias on VG1 to keep the current in VD1 constant in order to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.2 V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Board Layout - As shown in the board layout, it is recommended to provide 100pF decoupling caps as close to the bias pins as possible, with additional 10µF decoupling caps.

Recommended Board Layout

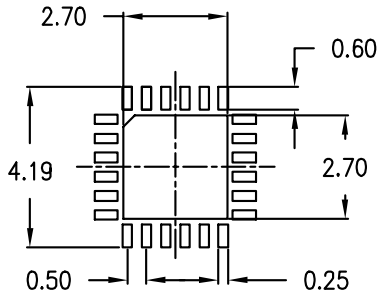


Lead-Free Package Dimensions/Layout



MARKINGS:
PIN 1/BOM REV/Pb FREE SYM
MIMIX PART/MODEL NO.
WAFER LOT NUMBER
DATE CODE

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTES:
1. DIMENSIONS ARE IN MM.

	MIN	TYP	MAX
A	0.80	0.90	1.00
A3		0.20 REF	
b	0.20	0.25	0.30
K	0.20	–	–
D		4.00 BSC	
E		4.00 BSC	
e		0.50	
D2	2.45	2.60	2.75
E2	2.45	2.60	2.75
L	0.20	0.30	0.40

1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.