
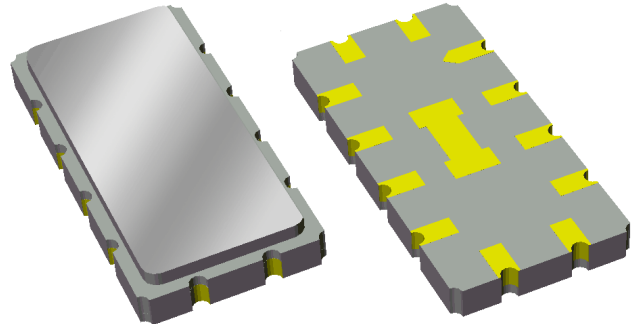


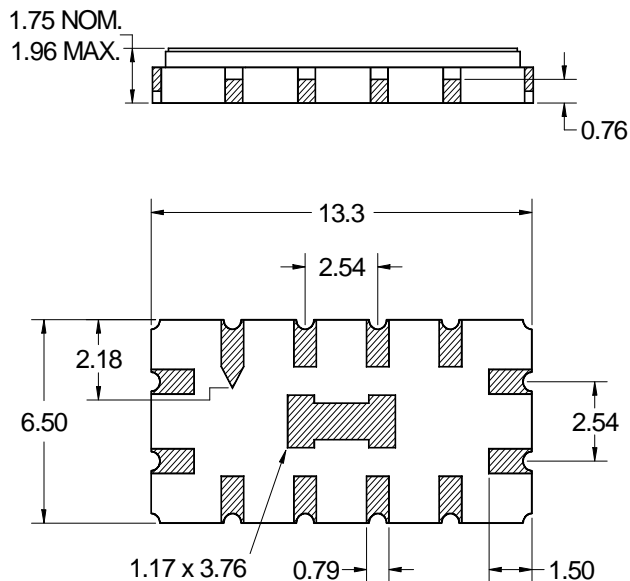
## Features

- For TD-SCDMA applications
- Usable bandwidth 15 MHz
- Low Loss
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



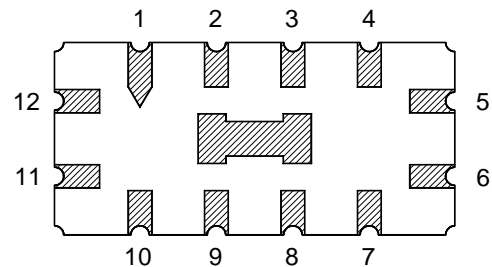
## Package

Surface Mount 13.30 x 6.50 x 1.75 mm  
SMP-53A



## Pin Configuration

Bottom View



### Single-ended Configuration

Pin No.	Description
11	Input
5	Output
1,4,6,7,10,12	Ground
2,3,8,9	Case Ground

Dimensions shown are nominal in millimeters  
All tolerances are  $\pm 0.15$ mm except overall  
length and width  $\pm 0.10$ mm

Body:  $Al_2O_3$  ceramic  
Lid: Kovar, Ni plated  
Terminations: Au plating 0.5 - 1.0 $\mu$ m,  
over a 2 - 6 $\mu$ m Ni plating

**Target Electrical Specifications <sup>(1)</sup>**

Operating Temperature Range: <sup>(2)</sup> -40 to +85 °C

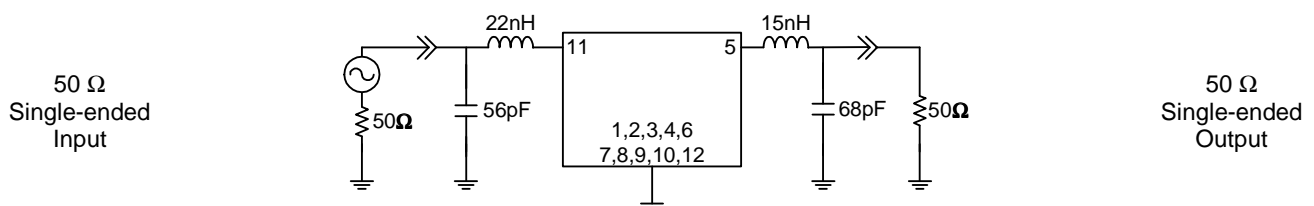
Parameter <sup>(3)</sup>	Minimum	Typical <sup>(4)</sup>	Maximum	Unit
Center Frequency	-	153.6	-	MHz
Insertion Loss at Center Frequency	-	10	12	dB
1 dB Bandwidth <sup>(5)</sup>	15	17.2	-	MHz
3 dB Bandwidth <sup>(5)</sup>	16	18.3	-	MHz
40 dB Bandwidth <sup>(5)</sup>	-	22.3	25	MHz
Lower 1 dB Band Edge <sup>(5)</sup>	-	144.9	146.1	MHz
Upper 1 dB Band Edge <sup>(5)</sup>	161.1	162.1	-	MHz
Lower 3 dB Band Edge <sup>(5)</sup>	-	144.5	145.6	MHz
Upper 3 dB Band Edge <sup>(5)</sup>	161.6	162.8	-	MHz
Amplitude Variation 146.1 – 161.1 MHz	-	0.4	1.0	dB p-p
Group Delay at 153.6	-	1.04	1.3	µs
Group Delay Variation 146.1 – 161.1 MHz	-	55	140	ns p-p
Phase Ripple 146.1 – 161.1 MHz	-	10	-	deg
Relative Attenuation <sup>(5)</sup> 10 – 50 MHz	50	62	-	dB
50 – 141.1 MHz	40	51	-	dB
166.1 – 170.1 MHz	40	43.7	-	dB
170.1 – 300 MHz	40	58	-	dB
300 – 500 MHz	45	70	-	dB
Input/Output Return Loss 146.1 – 161.1 MHz	8	10	-	dB
Source Impedance (single-ended) <sup>(6)</sup>	-	50	-	Ω
Load Impedance (single-ended) <sup>(6)</sup>	-	50	-	Ω

**Notes:**

1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. Relative to loss at center frequency
6. This is the optimum impedance in order to achieve the performance shown

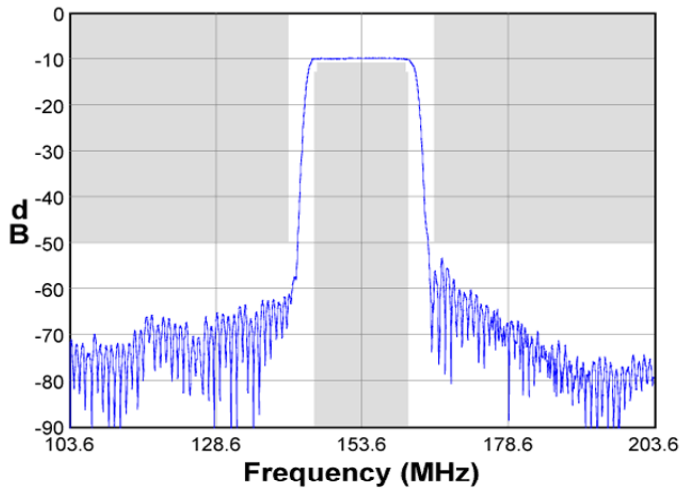
**Test Circuit:**

Actual matching values may vary due to PCB layout and parasitics

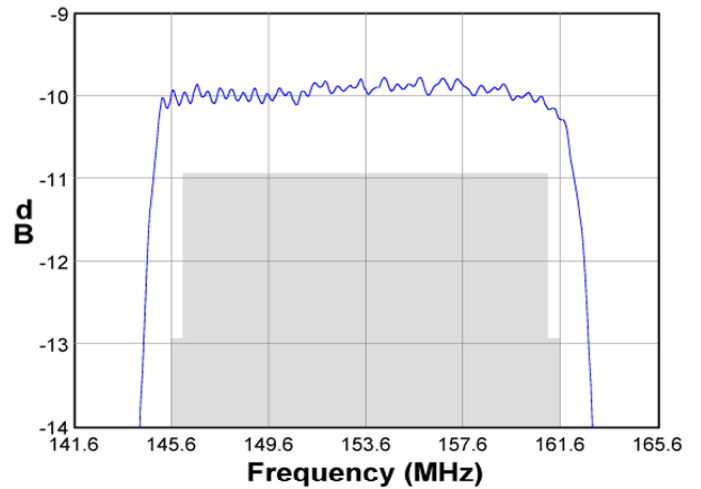


**Typical Performance (at room temperature)**

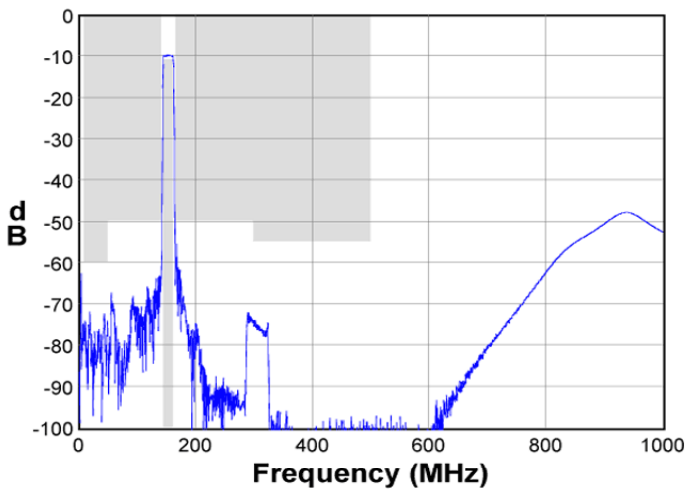
**Frequency Response**



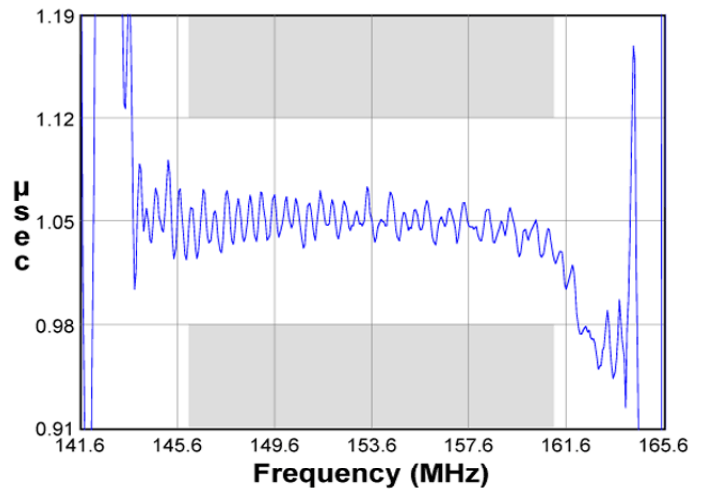
**Passband Response**



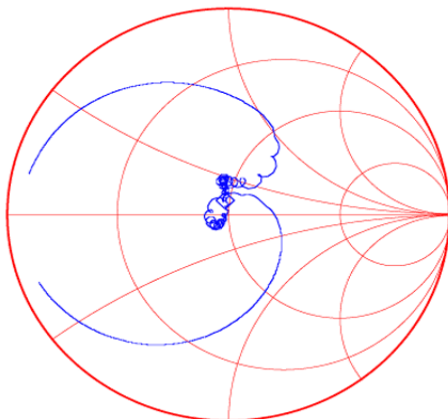
**Wideband Response**



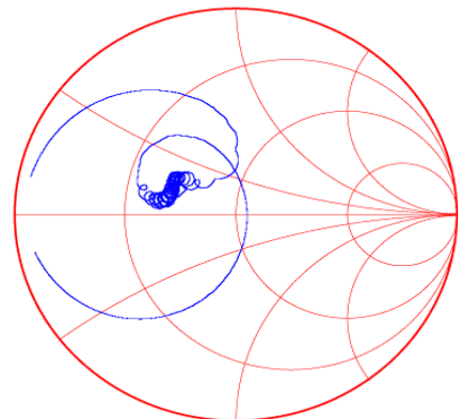
**Group Delay Response**



**Input Smith Chart**

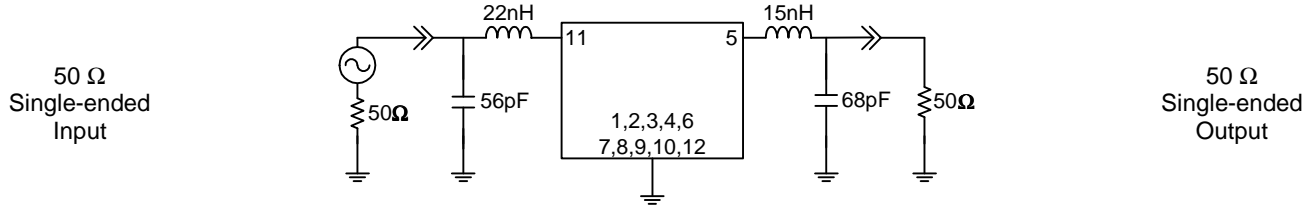


**Output Smith Chart**



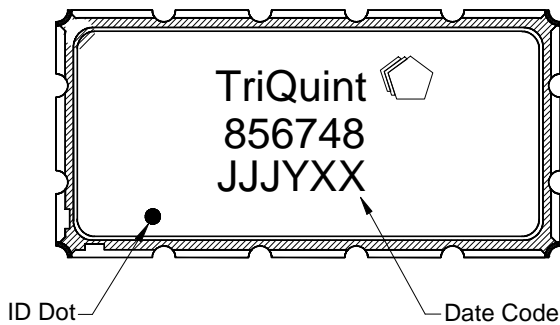
**Matching Schematics**

Actual matching values may vary due to PCB layout and parasitics

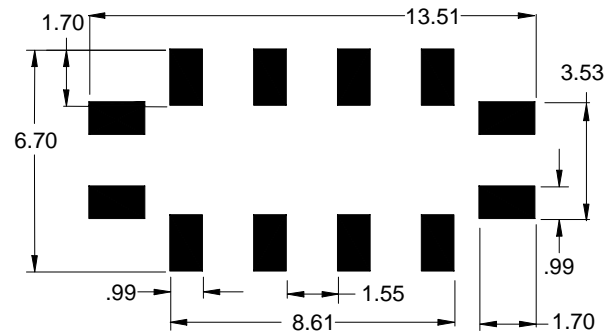


**Marking**

**PCB Footprint**

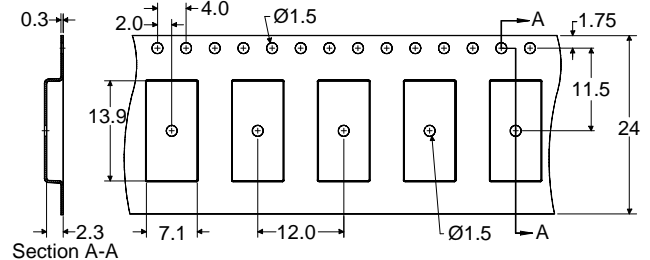
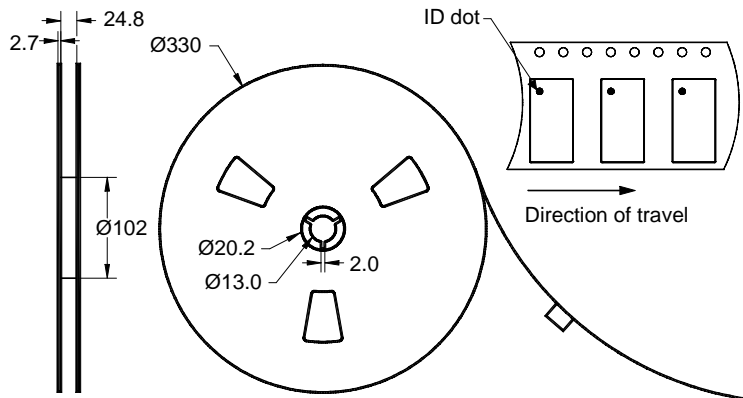


The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)



This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**




Dimensions shown are nominal in millimeters  
Packaging quantity: 2000 units/reel

### Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-40	+85	°C
Storage Temperature Range	T <sub>stg</sub>	-40	+85	°C

### Important Notes

#### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

#### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

#### Solderability

- Compatible with JESD22-B102, Pb-free process, 260C peak reflow temperature ([see soldering profile](#))

### Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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