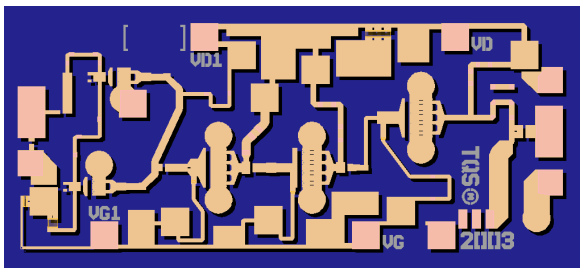
TGA4036

19 - 38 GHz Medium Power Amplifier



Key Features

- Frequency Range: 19 - 38 GHz
- 20 dB Nominal Gain
- 22 dBm Nominal Psat
- 30 dBm Nominal TOI
- Bias: 5 V, 160 mA (210mA @ P1dB)
- 0.25 um 3MI pHEMT Technology
- Chip Dimensions 1.69 x 0.75 x 0.10 mm (0.066 x 0.030 x 0.004 in)

Product Description

The TriQuint TGA4036 is a compact Medium Power Amplifier MMIC for Wide-band applications. The part is designed using TriQuint's proven standard 0.25 um power pHEMT production process.

The TGA4036 provides a nominal 20 dB Gain from 19-36 GHz, with Saturated Output Power of 22 dBm.

The part is ideally suited for low cost emerging markets such as Point-to-Point Radio, Point-to-Multi Point Communications, and Instrumentation.

The TGA4036 is 100% DC and RF tested on-wafer to ensure performance compliance.

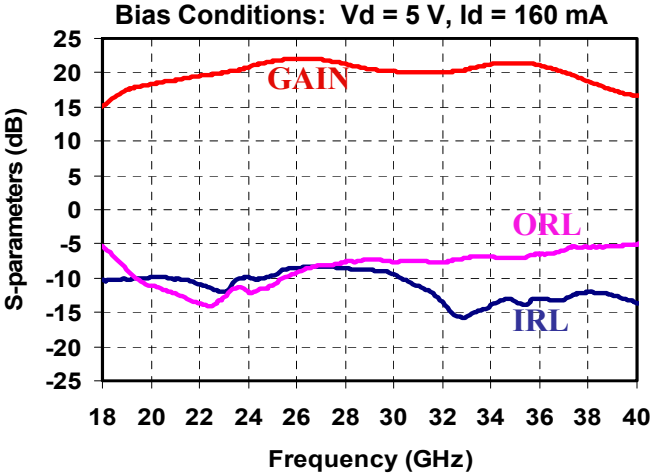
Evaluation boards are available.

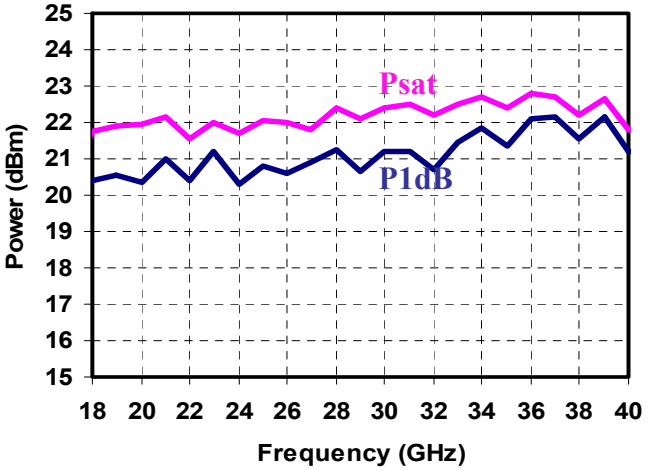
Primary Applications

- Point-to-Point Radio
- Point-to-Multipoint Communications
- Instrumentation

Measured Fixtured Data

Bias Conditions: Vd = 5 V, Id = 160 mA





Datasheet subject to change without notice

TriQuint Semiconductor: www. triquint.com (972)994-8465 Fax (972)994-8504 Info-mmw@tqs.com

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
Vd	Drain Voltage	7 V	2/
Vg	Gate Voltage Range	-1 TO +0.5 V	
Id	Drain Current	400 mA	2/ 3/
|Ig|	Gate Current	7 mA	3/
P_{IN}	Input Continuous Wave Power	20 dBm	
P_D	Power Dissipation	2.5 W	2/ 4/
T_{CH}	Operating Channel Temperature	200°C	5/ 6/
	Mounting Temperature (30 Seconds)	320 °C	
T_{STG}	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ Total current for the entire MMIC.

4/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is 2.3E4 hrs.

5/ Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings apply to each individual FET.

TABLE II
DC PROBE TEST
(TA = 25 °C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
Idss (Q1A)	Saturated Drain Current	15	94	mA
Gm (Q1A)	Transconductance	33	106	mS
Vp (Q1)	Pinch-off Voltage	-1.5	-0.5	V
BVGS (Q1A)	Breakdown Voltage Gate-Source	-30	-8	V
BVGD (Q1A,Q1B)	Breakdown Voltage Gate-Drain	-30	-10	V

Q1A and Q1B are 150um Input FETs

TABLE III

ELECTRICAL CHARACTERISTICS

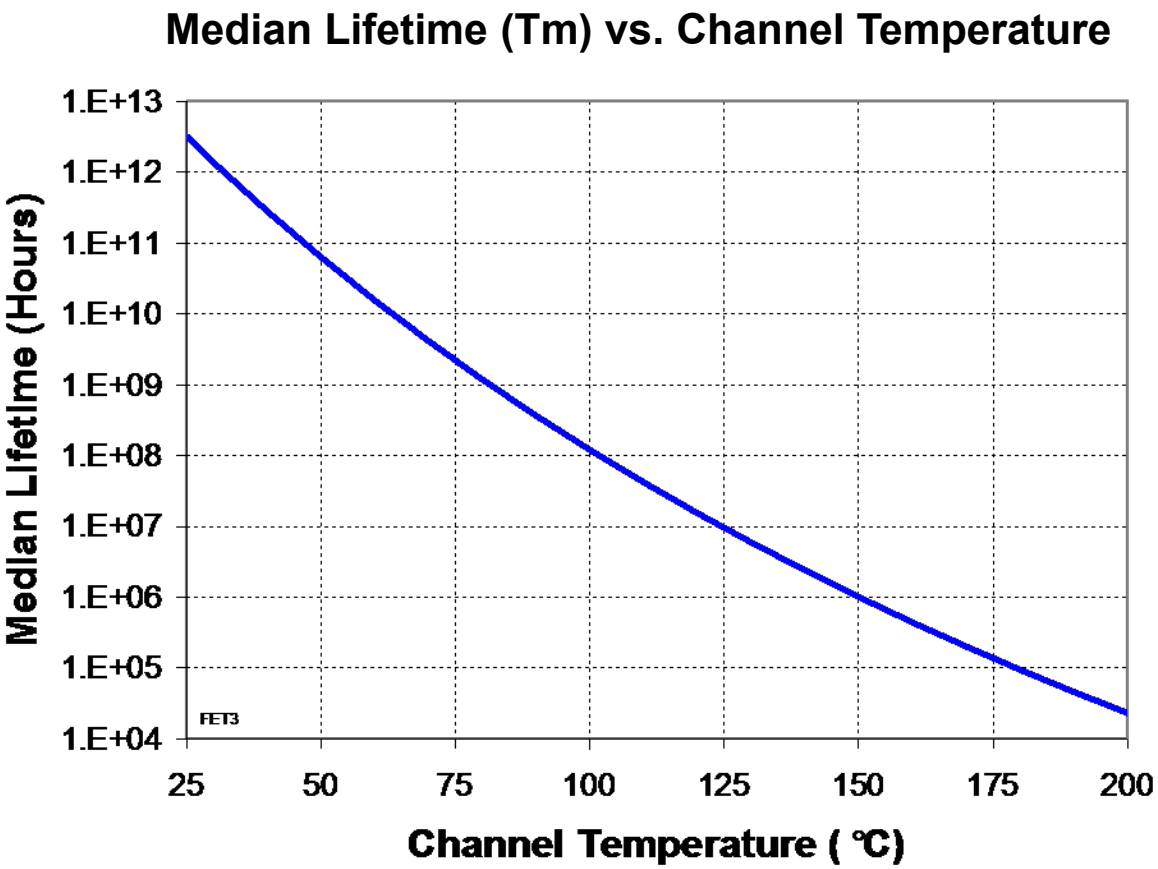
(Ta = 25 ^{0}C Nominal)

PARAMETER	TYPICAL	UNITS
Frequency Range	19 - 38	GHz
Drain Voltage, Vd	5.0	V
Drain Current, Id	160	mA
Gate Voltage, Vg	-0.6	V
Small Signal Gain, S21	20	dB
Input Return Loss, S11	11	dB
Output Return Loss, S22	8	dB
Output Power @ 1dB Gain compression, P1dB	21	dBm
Saturated Output Power, Psat	22	dBm
Output TOI @ Pin/tone = -10dBm	30	dBm
Temperature Coefficient	0.038	dB/^{0}C

TABLE IV
THERMAL INFORMATION

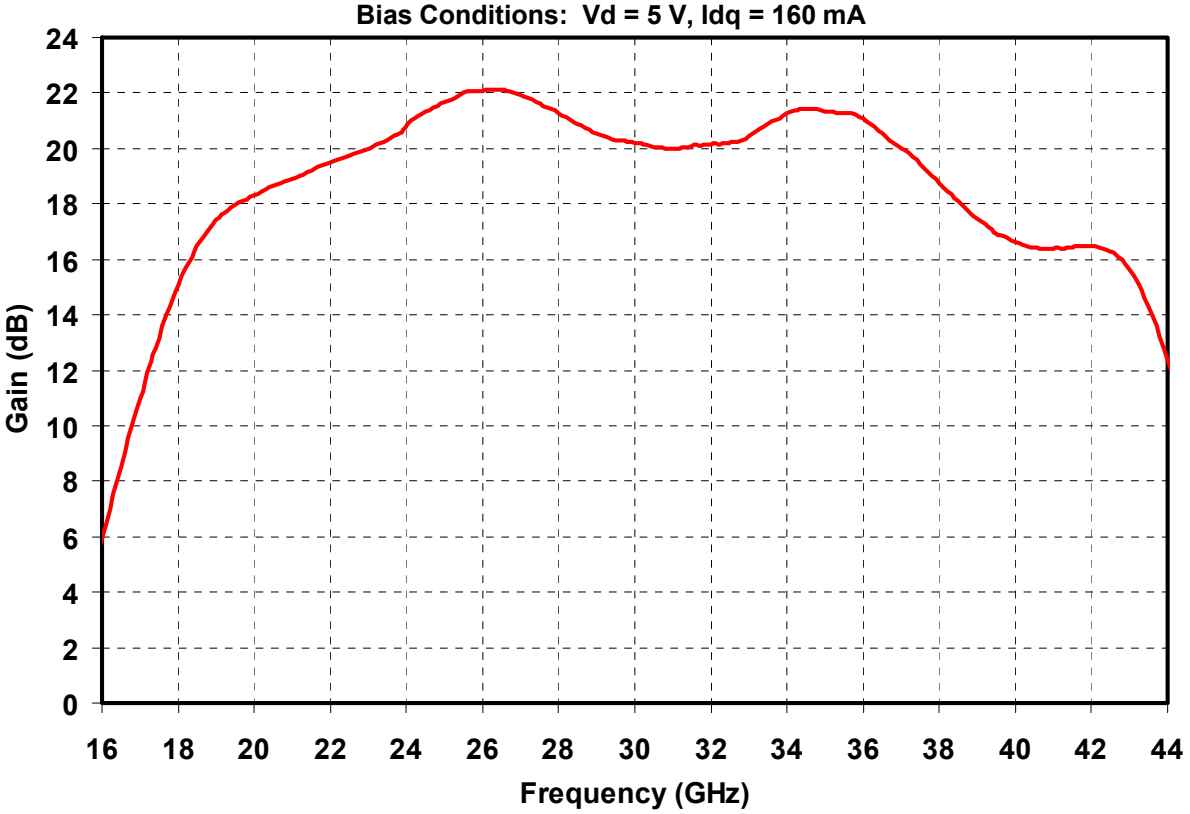
PARAMETER	TEST CONDITIONS	T_{CH} (°C)	θ_{JC} (°C/W)	Tm (HRS)
θ_{JC} Thermal Resistance (channel to Case)	Vd = 5 V Id = 160 mA Pdiss = 0.80 W	112	51.9	3.4E+7

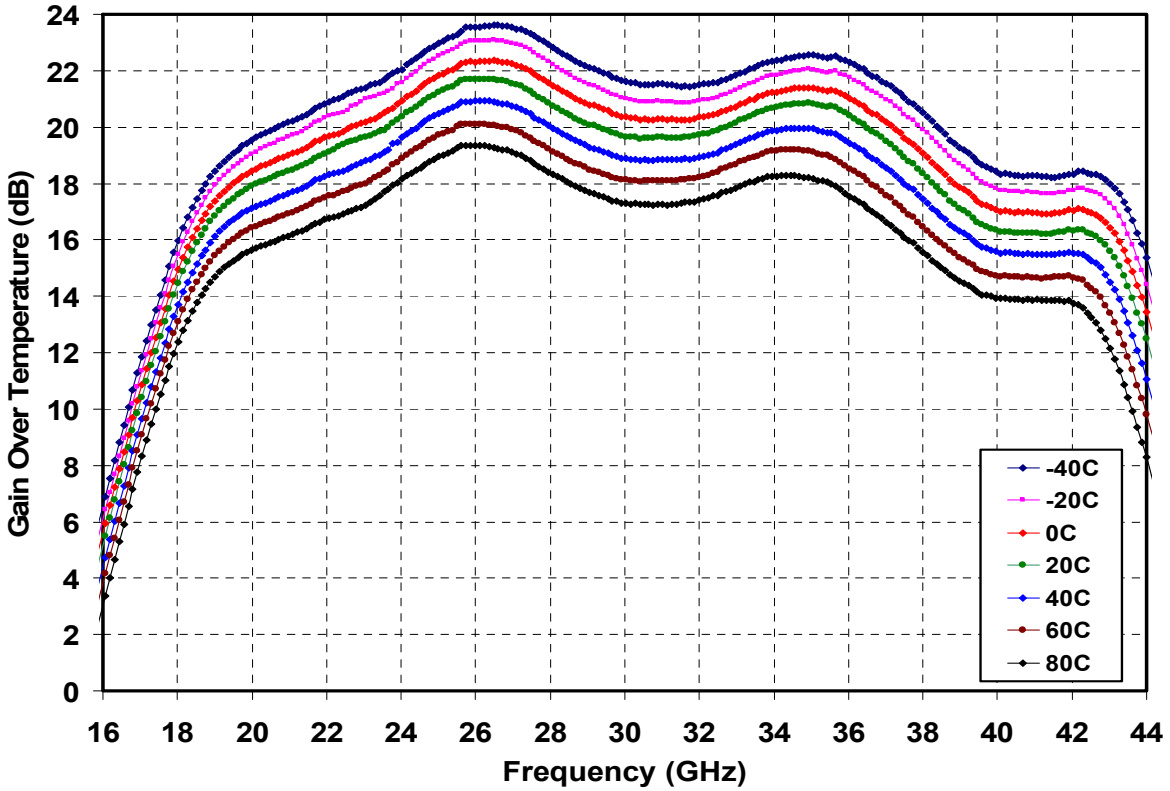
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70 °C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.



Preliminary Measured Data

Bias Conditions: Vd = 5 V, Idq = 160 mA





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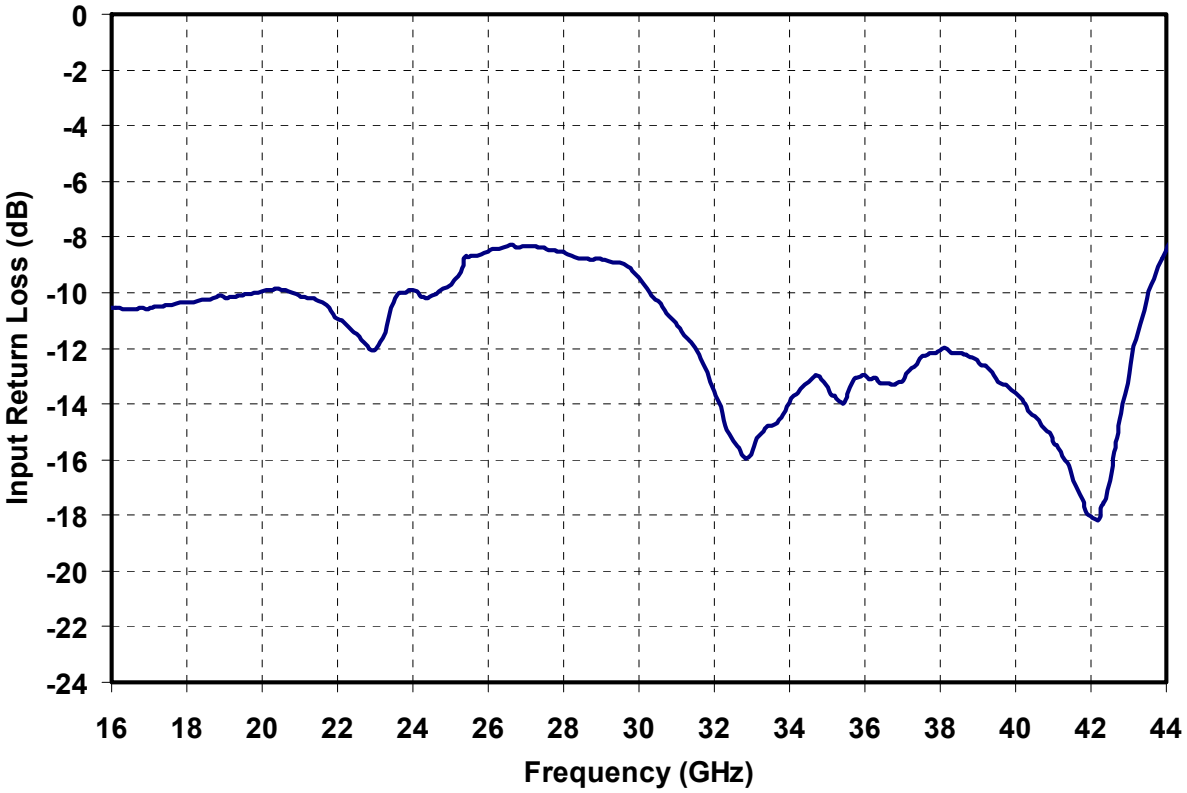

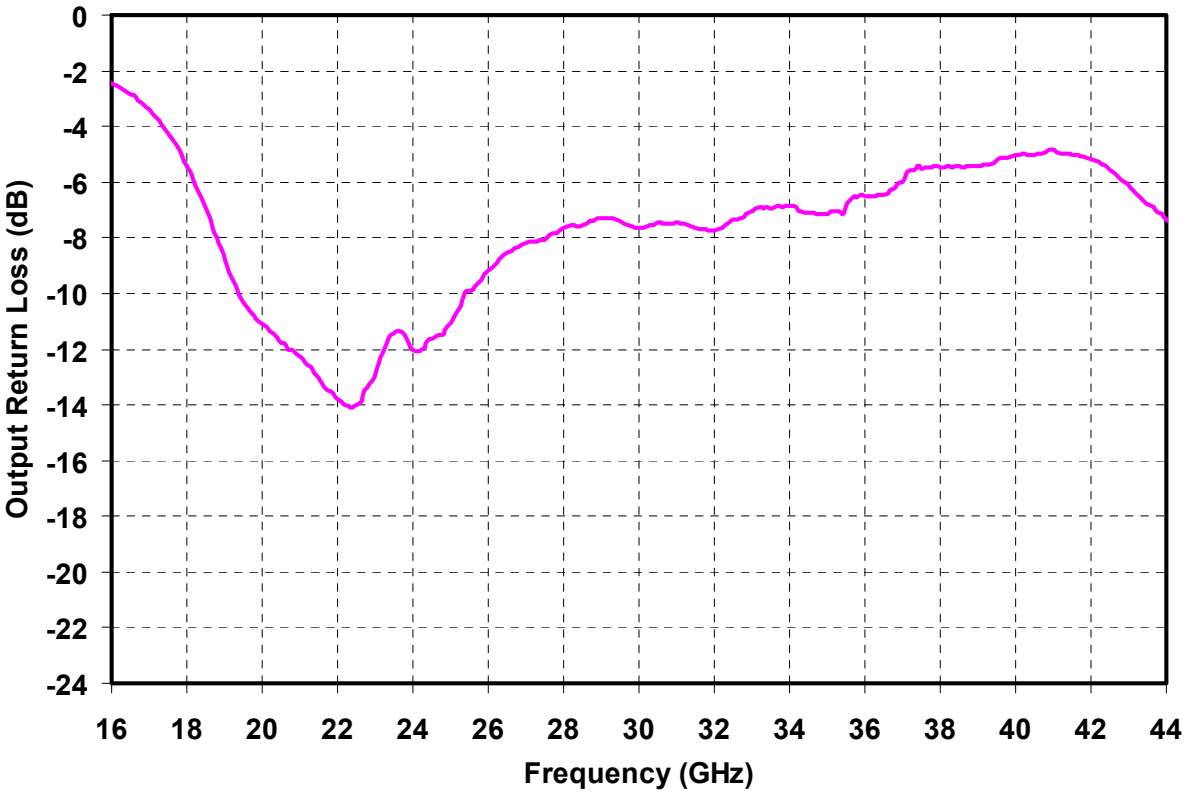

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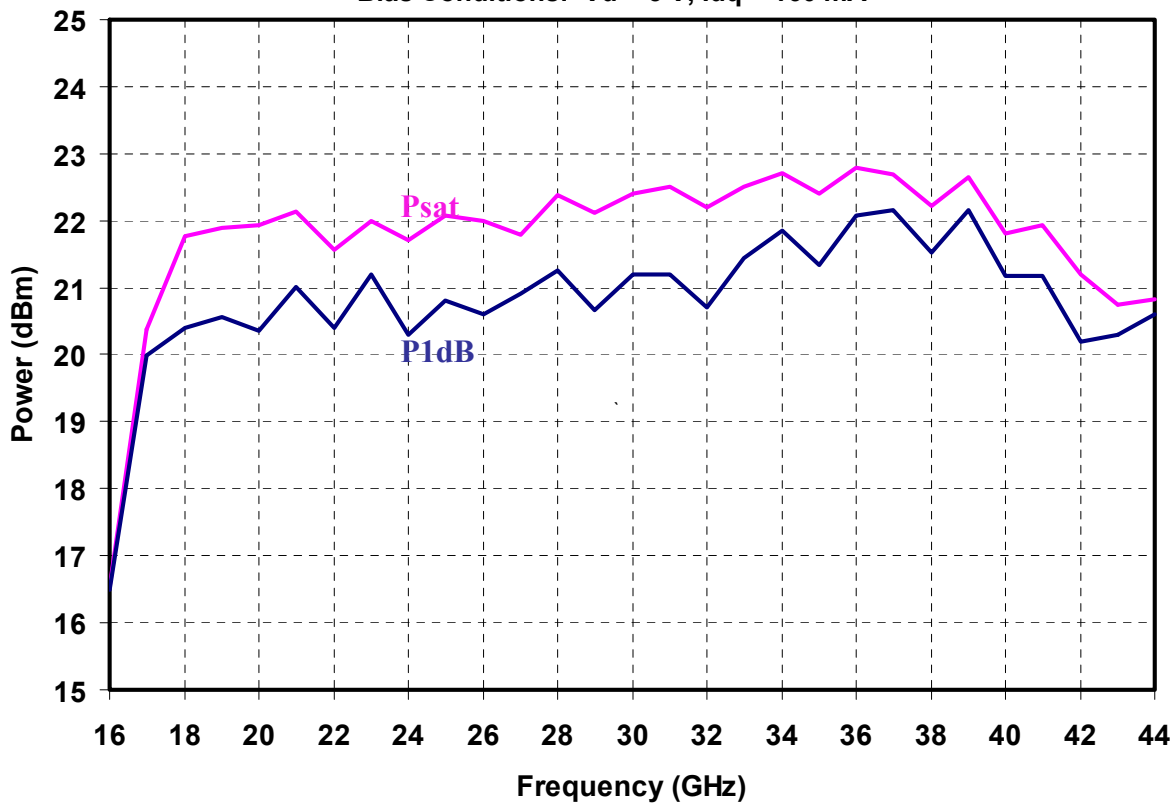

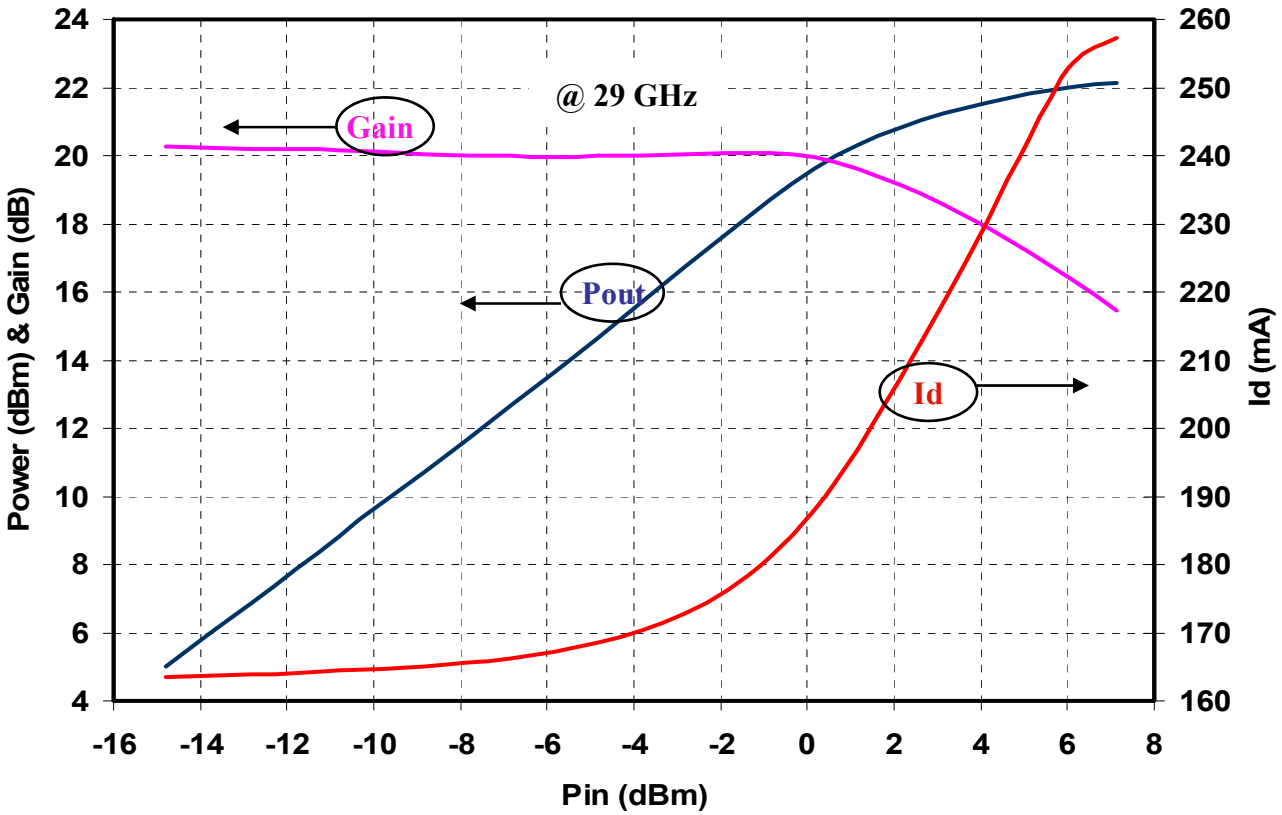

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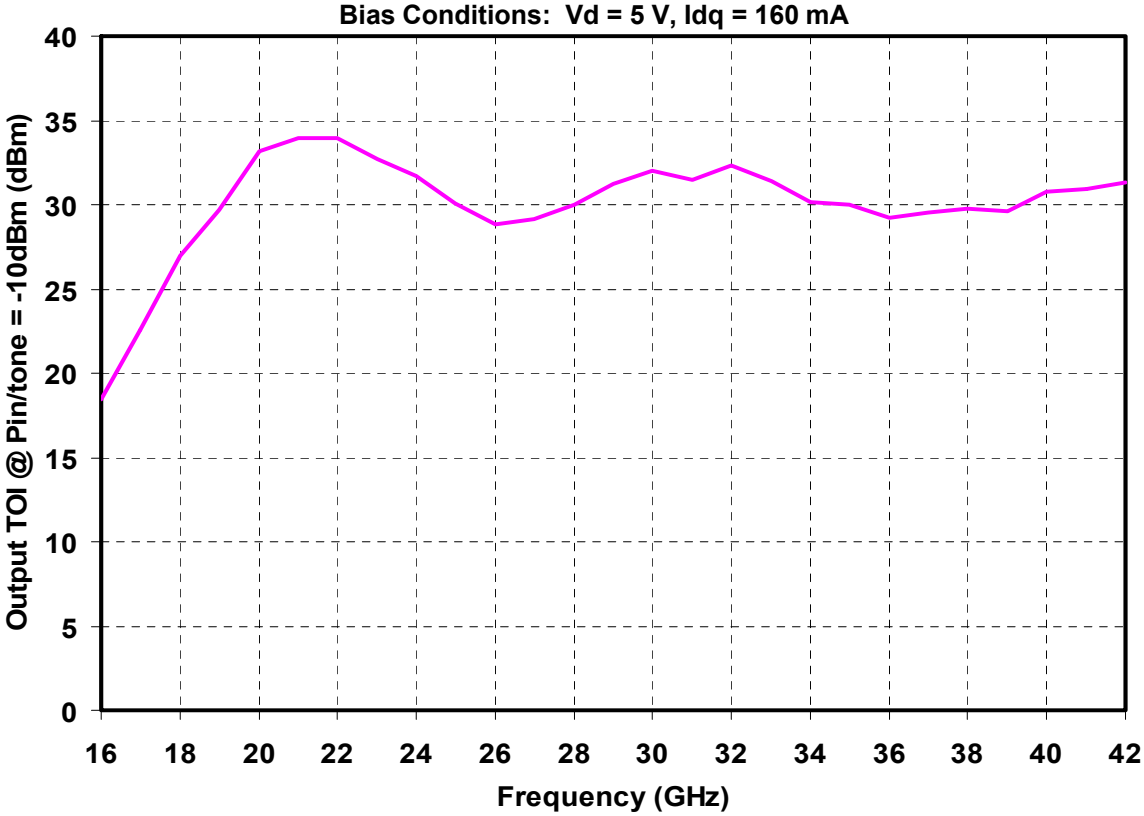
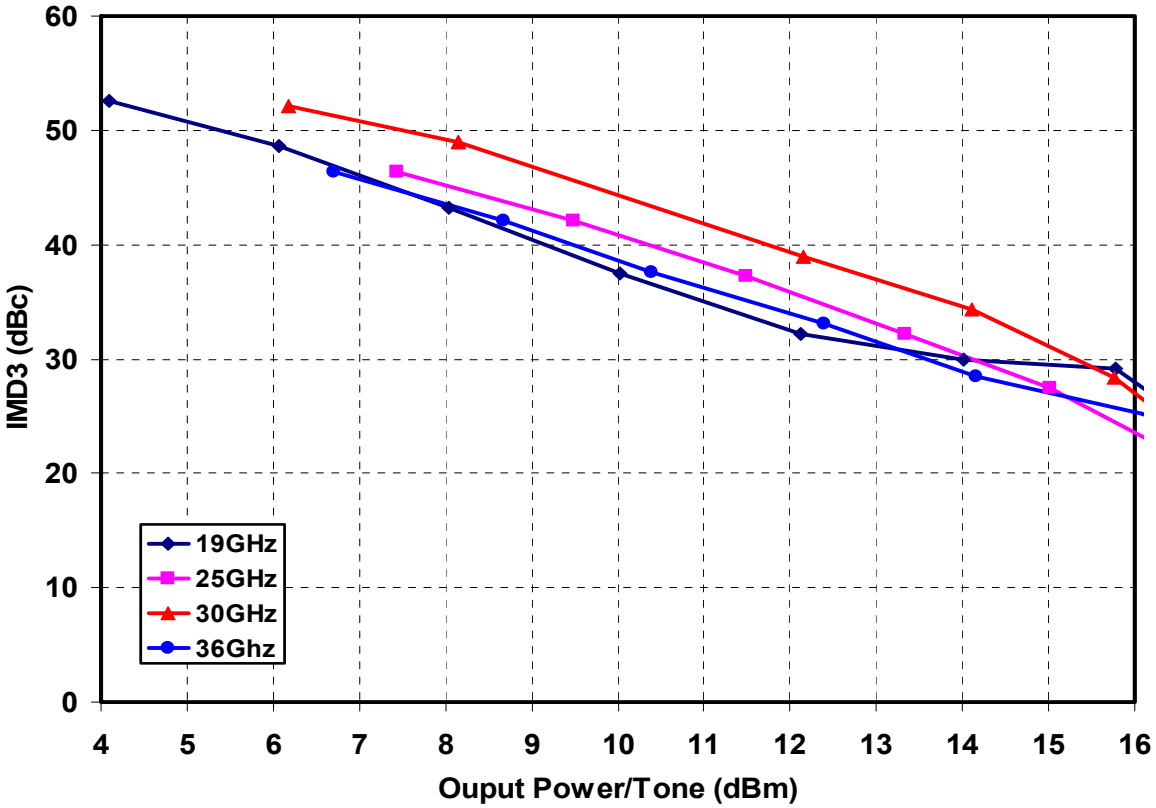
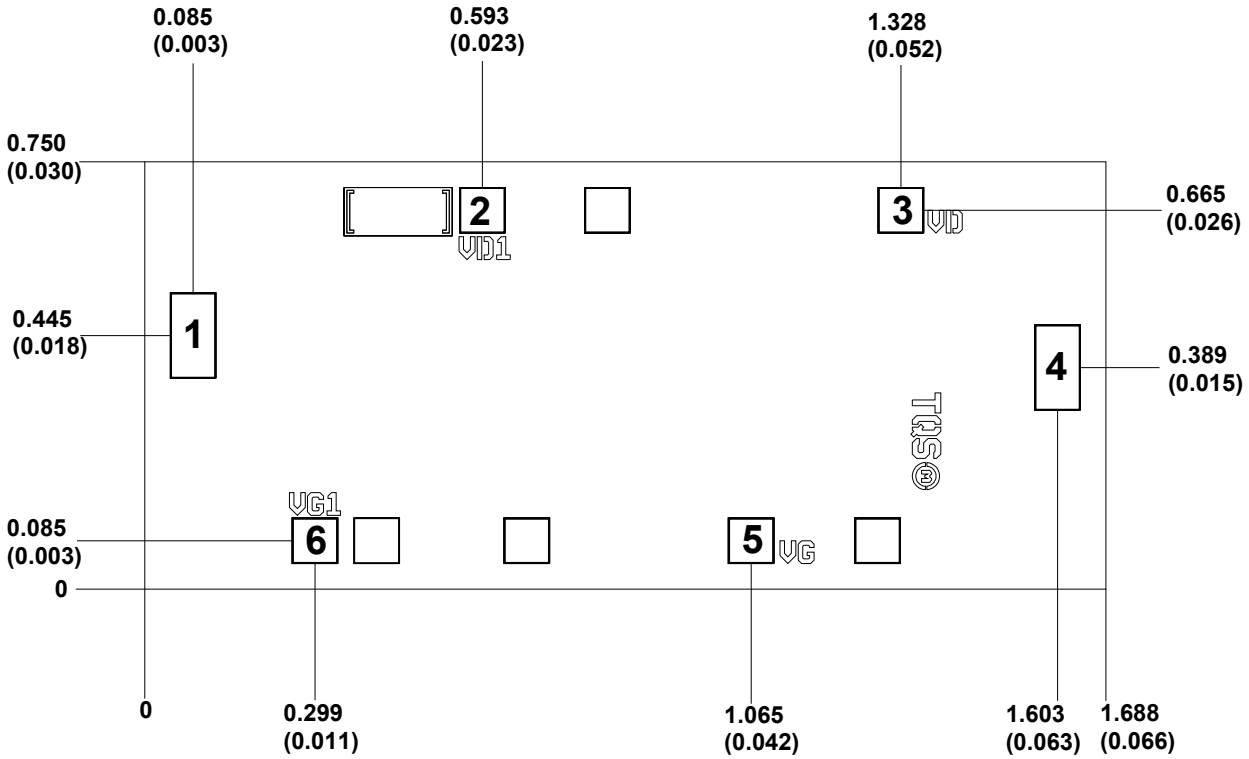




Mechanical Drawing

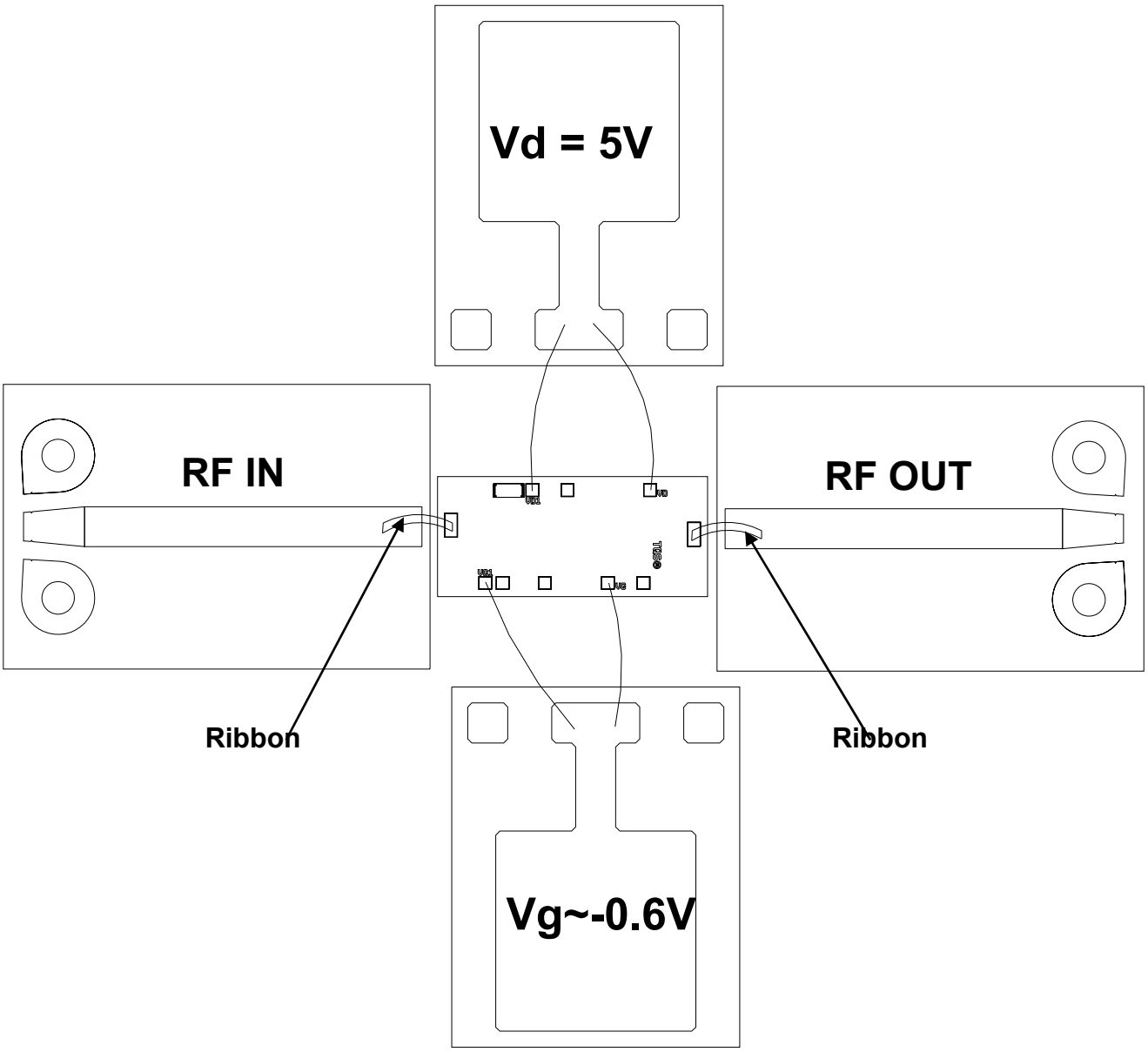


Units: Millimeters (inches)
Thickness: 0.100 (0.004) (Reference Only)
Cip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)
RF Ground is backside of MMIC

Bond pad #1:	**(RF In)**	**0.080 x 0.150 (0.003 x 0.006)**
Bond pad #2, #3:	**(Vd)**	**0.080 x 0.080 (0.003 x 0.003)**
Bond pad #4:	**(RF Out)**	**0.080 x 0.150 (0.003 x 0.006)**
Bond pad #5, #6:	**(Vg)**	**0.080 x 0.080 (0.003 x 0.003)**

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Chip Assembly Diagram



Adjust Vg to get Id = 160mA

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300^{0}C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200^{0}C.

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