Step-Down Switching Regulator with Current-Mode Control

Features and Benefits

- Current-mode control system employed
- Excellent line regulation (60 mV maximum)
- 165 mΩ maximum on-resistance of built-in MOSFET
- Output current 3.5 A
- Wide range of input voltages (4.75 to 28 V), supports 24 V direct drive
- Output voltage 0.5 to 24 V, compatible with various IC power supply voltages, through low V_{REF} of 0.5 V.
- High efficiency, 94% maximum at V_{IN} = 8 V, V_O = 5 V, and I_O = 0.5 A
- Operating frequency 350 kHz, supports downsizing of smoothing choke coil
- Soft start and output on/off functions built-in
- Built-in protection:
  - Drooping overcurrent protection
  - Overtemperature protection
  - Undervoltage lockout (UVLO)

Package: 8-pin DIP

Not to scale

Description

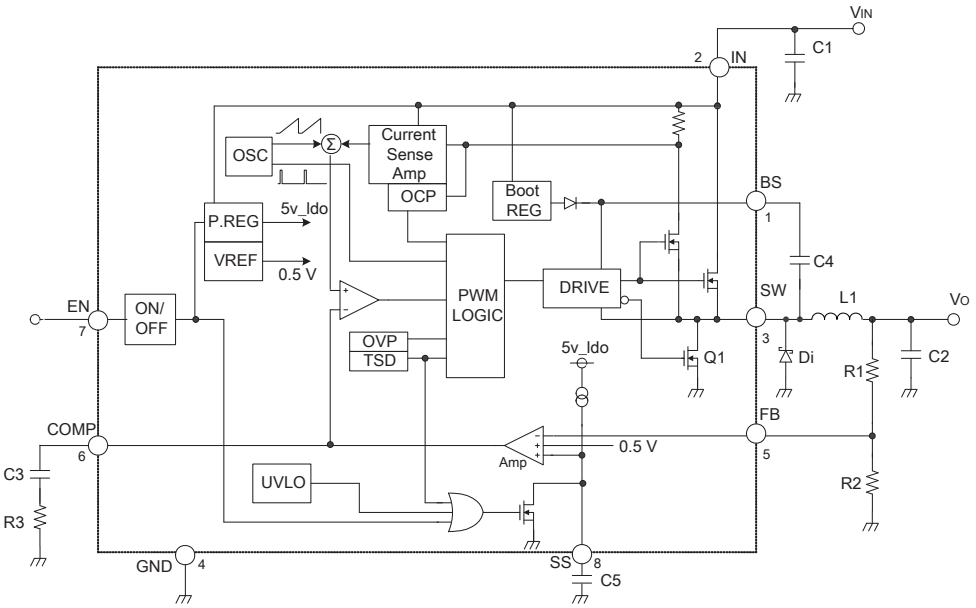
The SI-8105QL is a step-down switching regulator IC, designed as an output voltage regulator at the secondary stage of switch mode power supplies. The current-mode control system permits small ceramic capacitors to be used as output capacitors. Together with the compact DIP8 package, this allows reduction of regulator circuitry area on the PCB by approximately 50% in comparison with conventional topologies.

Designed to save power, losses in the SI-8105QL are reduced by controlling the maximum on-resistance of a built-in output MOSFET to as low as 165 mΩ. Furthermore, die miniaturization has been accomplished through a proprietary BCD process.

The SI-8105QL supplies an output current of 3.5 A and an output voltage that is variable from 0.5 to 24 V, which is easily set to a voltage compatible with the diverse reduced power supply voltages required by signal processing ICs. Accepting a wide input voltage range, from 4.75 to 28 V, the SI-8105QL can be driven directly by a 24 V power supply.

Applications include power supplies for signal processing ICs for memories and microcomputers used in plasma display panel (PDP) TVs, liquid crystal display (LCD) TVs, computer hard drives, and DVD recorders.

Functional Block Diagram



SANKEN ELECTRIC CO., LTD.
http://www.sanken-ele.co.jp/en/

Selection Guide

Part Number	Packing
SI8105QL-TL	1000 pieces per reel

Absolute Maximum Ratings

Characteristic	Symbol	Remarks	Rating	Unit
DC Input Voltage	V_{IN}		30	V
DC Input Voltage	V_{EN}		6	V
Allowable Power Dissipation	P_D	Limited by internal thermal shutdown, mounted on a 70 mm × 60 mm glass epoxy PCB with 1310 mm^2 exposed copper area	1.50	W
Junction Temperature	T_J	Internal thermal shutdown activates at approximately 140°C	–30 to 150	°C
Storage Temperature	T_{stg}		–40 to 150	°C
Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on a 70 mm × 60 mm glass epoxy PCB with 1310 mm^2 exposed copper area	67	°C/W
Thermal Resistance (Junction to Case)	$R_{\theta JC}$		25	°C/W

Recommended Operating Conditions*

Characteristic	Symbol	Remarks	Min.	Typ.	Max.	Units
DC Input Voltage Range	V_{IN}	V_{IN}(min) is the greater of either 4.75 V or V_O+3 V; except if $V_O + 2 \le V_{IN} \le V_O + 3$ V, then V_{IN}(min) is set such that $I_O \le 2$ A	See remarks	–	28	V
DC Output Current Range	I_O	Using the circuit defined in the Typical Application diagram and within P_D limits	0	–	3.5	A
Operating Junction Temperature Range	T_{JOP}		–30	–	125	°C
Operating Temperature Range	T_{OP}	Operation within P_D limits	–30	–	85	°C

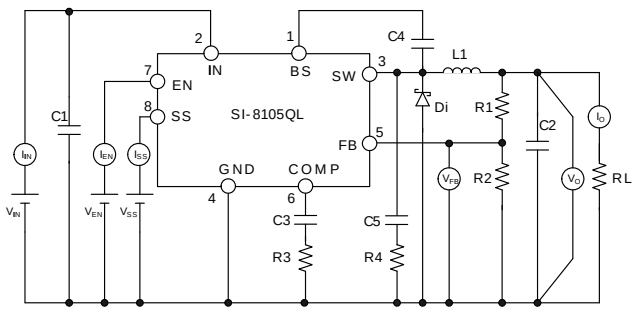
*Recommended operating range indicates conditions which are required for maintaining normal circuit functions shown in the Electrical Characteristics table.

ELECTRICAL CHARACTERISTICS[1], valid at T_A=25°C, unless otherwise noted

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Reference Voltage	V_{REF}	V_{IN} = 12 V, I_O = 1.0 A	0.485	0.500	0.515	V
Output Voltage Temperature Coefficient	$\Delta V_{REF}/\Delta T$	V_{IN} = 12 V, I_O = 1.0 A, T_A = –25°C to 100°C	–	±0.05	–	mV/°C
Efficiency[2]	η	V_{IN} = 12 V, V_O = 5 V, I_O = 1 A	–	90	–	%
Operating Frequency	f_O	V_{IN} = 16 V, V_O = 5 V, I_O = 1 A	315	350	385	kHz
Line Regulation	V_{LINE}	V_{IN} = 8 to 28 V, V_O = 5 V, I_O = 1 A	–	20	50	mV
Load Regulation	V_{LOAD}	V_{IN} = 12 V, V_O = 5 V, I_O = 0.1 to 3.5 A	–	20	50	mV
Overcurrent Protection Threshold	I_S	V_{IN} = 12 V, V_O = 5 V	3.6	–	6.0	A
Quiescent Current 1	I_{IN}	V_{IN} = 12 V, V_O = 5 V, I_O = 0 A, V_{EN} = open	–	18	–	mA
Quiescent Current 2	$I_{IN(off)}$	V_{IN} = 12 V, V_O = 5 V, I_O = 0 A,V_{EN} = 0 V	–	–	20	µA
SS Terminal Leakage Current[3]	I_{SSL}	V_{SSL} = 0 V, V_{IN} = 12 V	–	5	–	µA
EN Terminal High Level Voltage	V_{CEH}	V_{IN} = 12 V	2.8	–	–	V
EN Terminal Low Level Voltage	V_{CEL}	V_{IN} = 12 V	–	–	2.0	V
EN Terminal Leakage Current	I_{CEH}	V_{EN} = 0 V	–	1	–	µA
Error Amplifier Voltage Gain	A_{EA}		–	1000	–	V/V
Error Amplifier Transconductance	G_{EA}		–	800	–	µA/V
Current Sense To COMP Transimpedance	$1/G_{CS}$		–	0.35	–	V/A
Maximum Duty Cycle (On)	DC_{MAX}		–	92	–	%
Minimum On-Time	t_{MIN}		–	100	–	ns

[1]Using circuit shown in Measurement Circuit diagram.
[2]Efficiency is calculated as: $\eta(\%) = ([V_O \times I_O] / [V_{IN} \times I_{IN}]) \times 100$.
[3]SS terminal enables soft start when a an external capacitor is connected to it. Because a pull-up resistor is provided inside the IC, no external voltage can be applied to this terminal.

Measurement Circuit Diagram

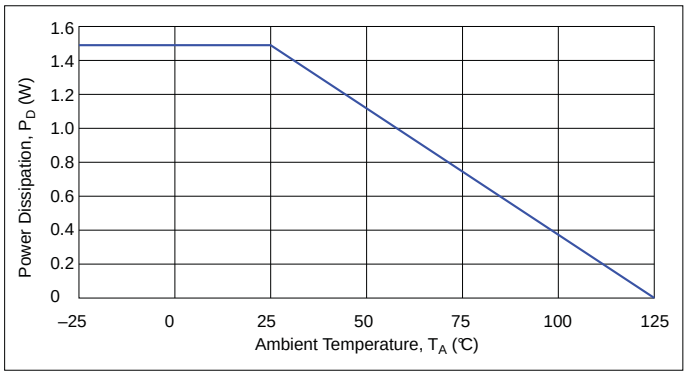


Component	Rating
C1	10 µF / 50 V
C2	47 µF / 25 V
C3	1200 pF / 10 V
C4	10 nF / 25 V
C5	1000 pF
Di	SPB-G56S
L1	22 µH
R1	46 kΩ
R2	5.1 kΩ
R3	20 kΩ
R4	10 Ω

All performance characteristics given are typical values for circuit or system baseline design only and are at the nominal operating voltage and an ambient temperature, T_A, of 25°C, unless otherwise stated.

Maximum Allowable Package Power Dissipation

Mounted on a 70 mm × 60 mm glass epoxy PCB with 1310 mm^2 exposed copper area



Results calculated as:

$$P_D = V_O \times I_O \left(\frac{100}{\eta x} - 1 \right) - V_F \times I_O \left(1 - \frac{V_O}{V_{IN}} \right)$$

where:

V_O is the output voltage,

V_{IN} is the Input voltage (0.4 V for these results),

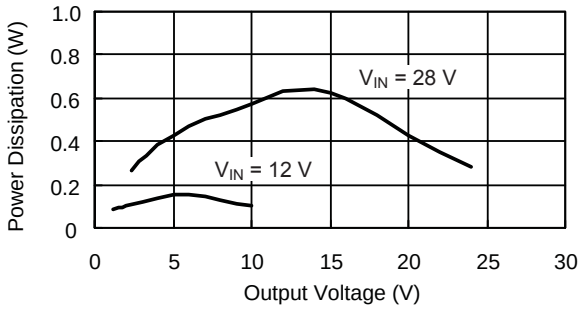
I_O is the Output current (0.3 A for these results),

ηx is the efficiency (%), which varies with V_{IN} and I_O (derived from the Efficiency curves in the Characteristic Performance section), and

V_F is the diode forward voltage for D1, determination of the value for D1 should be made based on testing with the actual application (Sanken diode SFPB-54 was used for these results).

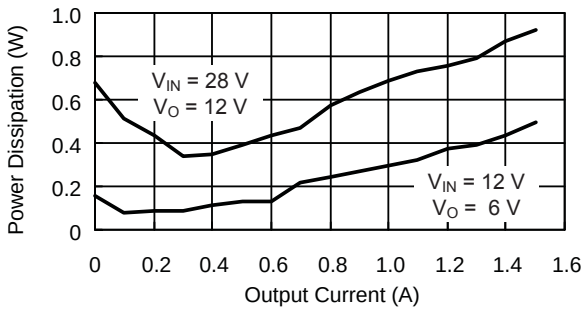
Package Power Dissipation with No Load

I_O = 0 A, L = 22 µH, T_A = 25°C



Package Power Dissipation with Load

L = 22 µH, T_A = 25°C

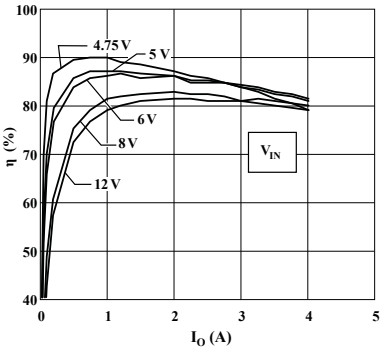


Note: When the SI-8105QL is operating in Discontinuous Conduction mode, the SI-8105QL has internal losses because the SI-8105QL must dissipate the energy from the charged Output capacitor (C2 in the Functional Block diagram) through the low-side switch MOSFET (Q1) on the SW circuit.

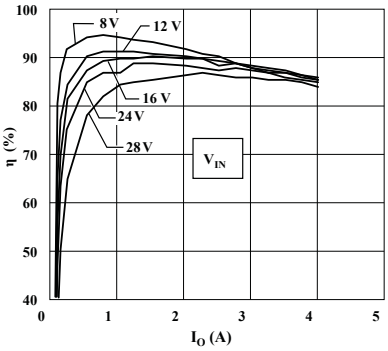
Performance Characteristics

at T_A = 25°C

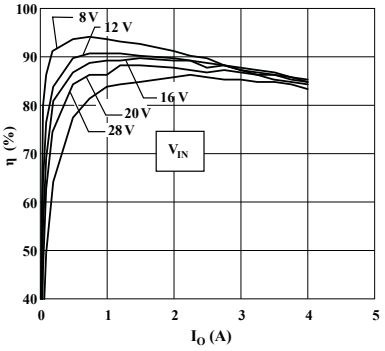
Efficiency versus Output Current
V_O = 1.2 V



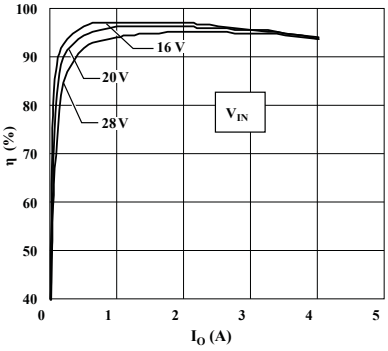
Efficiency versus Output Current
V_O = 3.3 V



Efficiency versus Output Current
V_O = 5 V



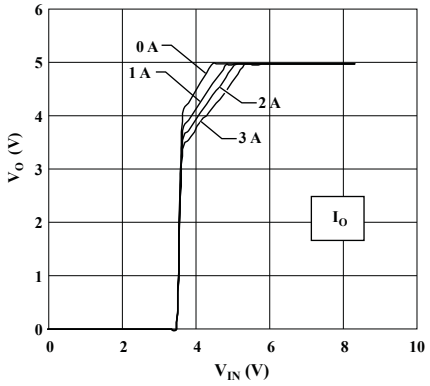
Efficiency versus Output Current
V_O = 12 V



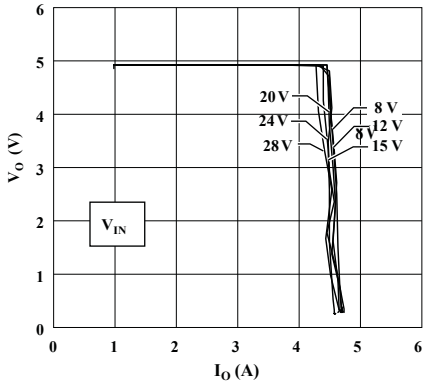
Performance Characteristics

at T_A = 25°C

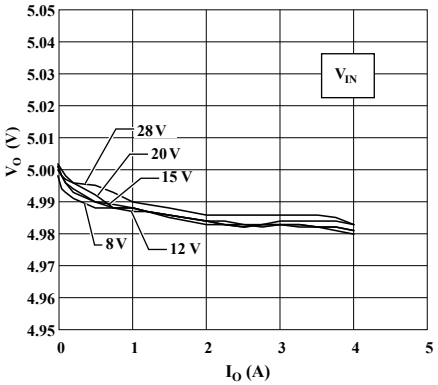
Overcurrent Protection
Load = CR



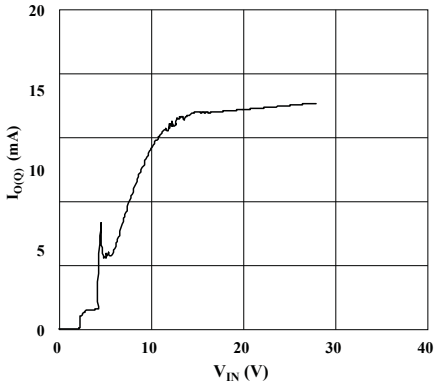
Overcurrent Protection



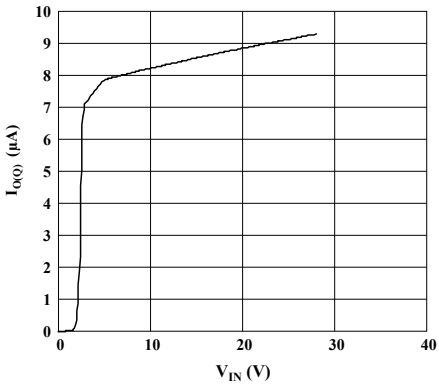
Load Regulation



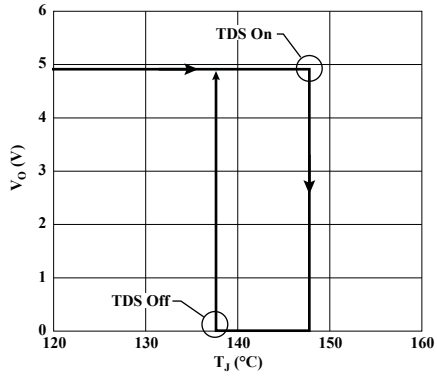
Quiescent Current versus Input Voltage
I_O = 0 A



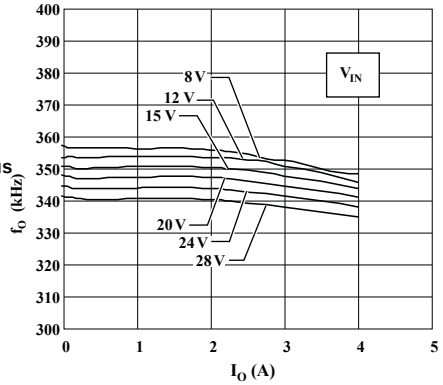
Quiescent Current versus Input Voltage
V_{EN} = 0 V



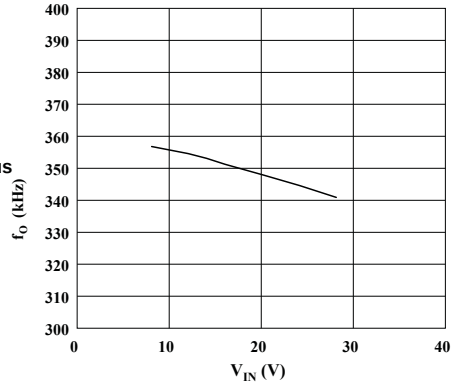
Overvoltage Protection
V_{IN} = 12 V
I_O = 0 A



Operating Frequency versus Output Current



Operating Frequency versus Input Voltage
I_O = 0 A



Diode Di A Schottky-barrier diode must be used for Di. If other diode types, such as fast recovery diodes, are used, the IC may be destroyed because of reverse voltages applied by the recovery voltage or turn-on voltage.

Choke Coil L1 If the winding resistance of the choke coil is too high, IC efficiency may go down to the extent that the resistance is beyond the rating. Because the overcurrent protection threshold current is approximately 4 A, attention must be paid to the heating of the choke coil by magnetic saturation due to overload or short-circulated load.

Capacitors C1, C2, C3 and C7 Because large ripple currents for SMPS flow across C1 and C2, capacitors with high frequency and low impedance must be used. Especially when the impedance of C2 is high, the switching waveform may not be normal at low temperatures.

C3 is used to enable soft start. If the soft start function is not used, leave the SS terminal open.

C7 is for ringing noise suppression

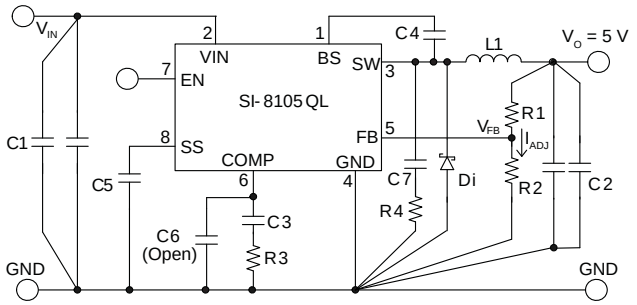
Resistors R1, R2 and R4 R1 and R2 set the output voltage, V_O. Select the resistor values to set I_{ADJ} to 0.1 mA. R_1 and R_2 are calculated by the following expression:

$$R_1 = \frac{(V_O - V_{FB})}{I_{ADJ}} = \frac{(V_O - 0.5)}{1\times10^{-3}} (\Omega) \text{ , and } R_2 = \frac{V_{FB}}{I_{ADJ}} = \frac{0.5}{1\times10^{-3}} \cong 5\,(\text{k}\Omega) \quad (1)$$

R4 is for ringing noise suppression.

For optimum performance, minimize the distance between components.

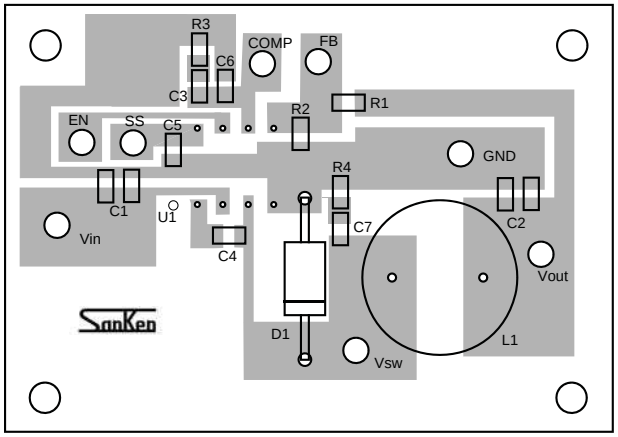
Typical Application Diagram



Note: If the value of output capacitor (C2) is large, or if it has a high ESR, or both, then C6 is required.

Component	Rating	Manufacturer
C1 (2 ea)	10 µF / 50 V	Murata, P/N GRM55DB31H106KA87
C2 (2 ea)	22 µF / 16 V	Murata, P/N GRM32ER71A226KE20
C3	1200 pF	Murata, P/N GRM18 series
C4, C5	10 nF	Murata, P/N GRM18 series
C7	1000 pF	Murata, P/N GRM18 series
Di		Sanken, P/N SPB-G56S or SJPB-L4
L1	22 µH	
R1	46 kΩ	
R2	5.1 kΩ	
R3	20 kΩ	
R4	10 Ω	

Recommended PCB Layout



All external components should be mounted as closely as possible to the SI-8105QL. The ground of all components should be connected at one point.

Phase Compensation Components C3, C6, and R3 The stability and response of the loop is controlled through the COMP pin. The COMP pin is the output of the internal transconductance amplifier. The combination of a series-connected capacitor and resistor sets the combination of a pole and zero frequency point that decide the characteristics of the control system. The DC gain of the voltage feedback loop is calculated by the following equation:

$$Adc = Rl \times Gcs \times A_{EA} \times \frac{V_{FB}}{Vout} \quad , \tag{2}$$

where

V_{FB} is the feedback voltage (0.5 V),

A_{EA} is the error amplifier voltage gain,

G_{CS} is the current sense transconductance, and

Rl is the load resistor value.

The system has two important poles. One is set by the phase compensation capacitor (C3) and the output resistor of the error amplifier. The other is set by the output capacitor and load resistor. These poles are calculated by the following equations:

$$fp1 = \frac{G_{EA}}{2\pi \times C3 \times A_{EA}} \quad , \tag{3}$$

$$fp2 = \frac{1}{2\pi \times C2 \times Rl} \quad , \tag{4}$$

where G_{EA} is the error amplifier transconductance.

The system has one important zero. This is set by the phase compensation capacitor (C3) and phase compensation resistor (R3). The zero is shown by the following equation:

$$fz1 = \frac{1}{2\pi \times C3 \times R3} \quad . \tag{5}$$

If the value of the output capacitor is the large or if it has a high ESR, the system may have another important zero. This zero would be set by the ESR and capacitance of the output capacitor. The zero is shown by the following equation:

$$fESR = \frac{1}{2\pi \times C2 \times RESR} \quad . \tag{6}$$

In this case a third pole, which is set by the phase compensation capacitor (C6) and phase compensation resistor (R3), is used to compensate the effect of the ESR zero on the loop gain.

The pole is shown by the following equation:

$$fp3 = \frac{1}{2\pi \times C6 \times R3} \quad . \tag{7}$$

The goal of phase compensation design is to shape the converter transfer function to get the required loop gain. The system crossover frequency, where the feedback loop has unity gain, is important. Lower crossover frequencies result in slower line and load transient responses. On the other hand, higher crossover frequencies cause system instability. A good standard is to adjust the crossover frequency to approximately one-tenth of the switching frequency.

The optimal selection of phase compensation components can be determined using the following procedure:

1. Choose the phase compensation resistor (R3) to adjust the required crossover frequency. R3 value is calculated by the following equation:

$$R3 = \frac{2\pi \times C2 \times fc}{GEA \times GCS} \times \frac{Vout}{VFB} < \frac{2\pi \times C2 \times 0.1 \times fs}{GEA \times GCS} \times \frac{Vout}{V_{FB}} \quad , \tag{8}$$

where f_c is the required crossover frequency. This is usually adjusted to less than one-tenth of the switching frequency.

2. Choose the phase compensation capacitor (C3) to get the required phase margin. For applications that have typical inductor values, adjusting the compensation zero to less than one-quarter of crossover frequency provides sufficient phase margin. The value of C3 is calculated by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times fc} \quad , \tag{9}$$

where R3 is the phase compensation resistor.

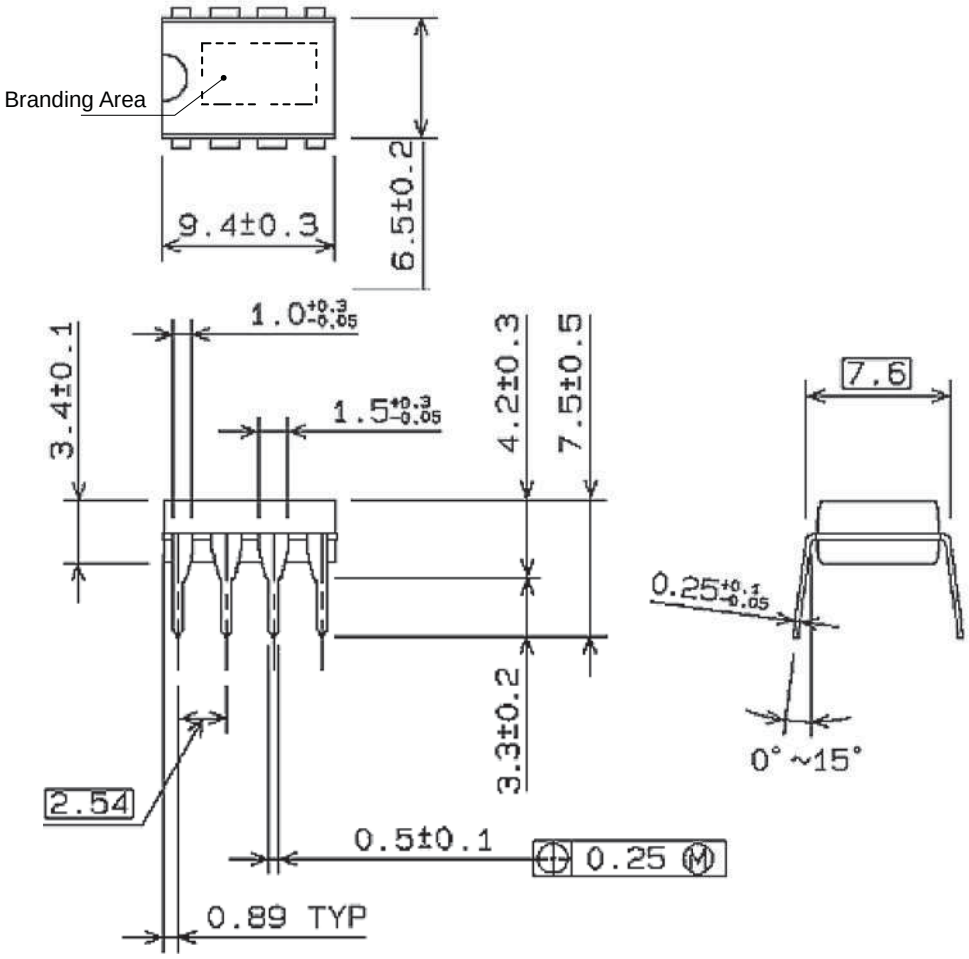
3. It is necessary to determine whether a second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is less than half of the switching frequency, expressed as follows:

$$\frac{1}{2\pi \times C2 \times RESR} < \frac{fs}{2} \quad . \tag{10}$$

If this is the case, add the second compensation capacitor (C6) and adjust ESR zero frequency (f_{p3}). C6 value is calculated by the following equation:

$$C6 = \frac{C2 \times RESR}{R3} \quad . \tag{11}$$

Package Outline Drawing



Dimensions in millimeters

Branding codes (exact appearance at manufacturer discretion):
1st line, type: 8105QL
2nd line, lot: YMW
Where: Y is the last digit of the year of manufacture
M is the month (1 to 9, O, N, D)
W is the week of the month (1 to 5)
3rd line, control number: NNNN

Leadframe plating Pb-free. Device composition complies with the RoHS directive.

Cautions

In general, the junction temperature level of surface mount package ICs is dependent upon the area and material of the PC board and its copper area. Therefore, please design the PCB to allow sufficient margin for heat dissipation.

Parallel Operation Parallel operation of multiple products to increase the current is not allowed.

Thermal Shutdown The SI-8000Q series has a thermal protection circuit. This circuit keeps the IC from the damage by overload. But this circuit cannot guarantee the long-term reliability against the continuous overload conditions.

ESD Susceptibility Take precautions against damage by static electricity.

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  In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.
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