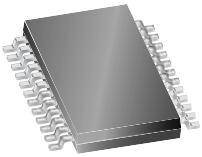
LED Backlight Driver for LCD Monitors and Televisions

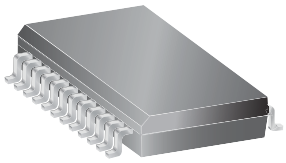
Features and Benefits

- Fixed frequency current mode control with integrated gate driver
- Each individual current sink is capable of 80 mA
- Adjustable overvoltage protection (OVP)
- Active current sharing between LED strings for ±0.6% accuracy and matching
- 250 kHz to 1 MHz adjustable switching frequency
- Open or shorted LED string protection
- Overtemperature, cycle-by-cycle current limit, and undervoltage protection
- No audible MLCC noise during PWM dimming
- No pull-up resistors required for LED modules that use ESD capacitors
- SOIC 24-pin package for easy single-side PCB manufacturing or TSSOP 24-pin package with exposed thermal pad for better thermal performance

Packages:



24-pin TSSOP
with exposed thermal pad
(Package LP)



24-pin SOICW
with internally fused pins
(LB package)

Not to scale

Description

The A8507 is a multi-output WLED/RGB driver for backlighting LCD monitors and televisions. The A8507 integrates a boost controller to drive external MOSFET and six internal current-sinks. The boost converter is constant frequency current mode converter.

PWM dimming allows LED currents to be controlled in 500:1 ratio. The LED sinks are capable of sinking up to 80 mA each, and can be paralleled together to achieve even higher currents.

The A8507 provides protection against overvoltage, open or shorted LED string, and overtemperature. A dual level cycle-by-cycle current limit function provides soft start and protects against overloads.

The device is provided in a 24-pin SOICW package (LB), with internally fused pins for enhanced thermal dissipation, and a 24-pin TSSOP package (LP), with an exposed thermal pad for enhanced thermal dissipation. Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

Functional Block Diagram

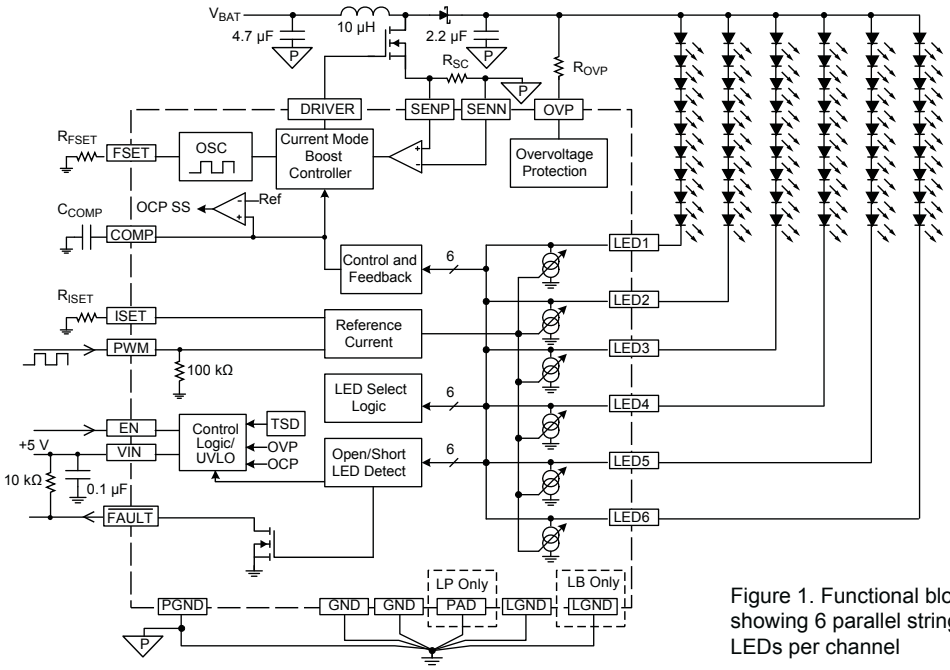


Figure 1. Functional block diagram showing 6 parallel strings with 9 series LEDs per channel

Selection Guide

Part Number	Packing	Package
A8507ELBTR-T	1000 pieces per 13-in. reel	24-pin SOICW, with internally fused pins for enhanced thermal dissipation
A8507ELPTR-T	4000 pieces per 13-in. reel	24-pin TSSOP, with exposed thermal pad for enhanced thermal dissipation

Absolute Maximum Ratings

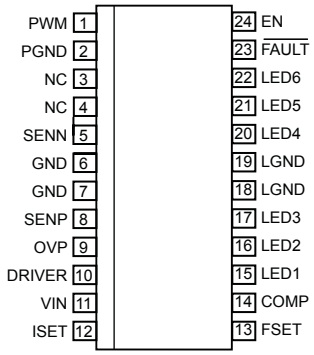
Characteristic	Symbol	Notes	Rating	Unit
LED Output Voltage	V_{LEDx}		–0.3 to 40	V
OVP Pin Input Voltage	V_{OVP}		–0.3 to 50	V
SENP and SENN Pin Input Voltage	V_{SENx}		–0.3 to 1	V
Remaining Pins Input Voltage	V_{IN}		–0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

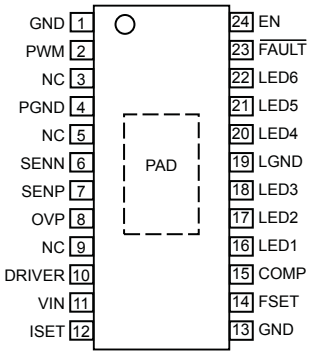
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LB, on 2-layer PCB, 1-in^2 2-oz copper exposed area	51	ºC/W
		Package LB, on 4-layer PCB, based on JEDEC standard	35	ºC/W
		Package LP, 4-layer PCB, based on JEDEC standard	28	ºC/W

*Additional thermal information available on the Allegro website

Pin-out Diagrams



Package LB



Package LP

Terminal List Table

Number		Name	Function
LB	LP		
1	2	PWM	PWM LED-current control; apply logic level PWM for dimming
2	4	PGND	Power ground for external FET gate driver; connect to common star ground and R_{SC} ground
3,4	3,5,9	NC	No internal electrical connection to these pins
5	6	SENN	Connect ground side of current sense resistor R_{SC}
6,7	1,13	GND	Connect to common star ground
8	7	SENP	Connect high side of current sense resistor R_{SC}
9	8	OVP	Connect this pin to output capacitor +ve node to enable overvoltage protection; typical OVP level is 36 V, and this level can be increased by connecting through an external resistor R_{OVP}
10	10	DRIVER	Gate driver terminal to drive external MOSFET
11	11	VIN	Input supply for the IC; decouple with a 0.1 µF ceramic capacitor
12	12	ISET	Sets 100% Current through LED strings; connect R_{ISET} from ISET to GND
13	14	FSET	Sets switching frequency; connect R_{FSET} from FSET to GND
14	15	COMP	Compensation pin; connect 1 µF capacitor to GND or common star ground
15,16,17	16,17,18	LEDx	LED sinks capable of 80 mA sink; connect unused LEDx pins to ground
18,19	19	LGND	Connect to common star ground
20,21,22	20,21,22	LEDx	LED sinks capable of 80 mA sink; connect unused LEDx pins to ground
23	23	$\overline{\text{FAULT}}$	During normal operation, this pin is high (high impedance); at a fault event, this pin pulls low
24	24	EN	Device enable
–	PAD	PAD	Exposed pad for enhanced thermal dissipation, connect to common star ground

ELECTRICAL CHARACTERISTICS Valid at V_{IN} = 5 V; T_A = 25°C, R_{FSET} = 52 kΩ, R_{ISET} = 12.4 kΩ, except • indicates specifications guaranteed over the full operating temperature range with $T_A = T_J$, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit
Input Voltage Range	V_{IN}		•	4.3	–	5.5	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} Falling	•	–	–	4.0	V
Undervoltage Lockout Hysteresis	$V_{UVLOHYS}$			–	0.1	–	V
Supply Current[2]	I_{VIN}	Switching at no load		–	7	–	mA
		Shutdown, EN = V_{IL}, T_A = 25°C		–	0.1	1	µA
		Standby, EN = V_{IH}, PWM = V_{IL}, soft start completed	•	–	1	2	mA
Boost Controller							
Switching Frequency	f_{SW}		•	0.8	1	1.25	MHz
Minimum Switch Off-Time	$t_{off(min)}$	Driver output		–	72	–	ns
Minimum Switch On-Time	$t_{on(min)}$	Driver output		–	72	–	ns
Logic Input Levels (EN and PWM pins)							
Input Voltage Level Low	V_{IL}		•	–	–	0.4	V
Input Voltage Level High	V_{IH}		•	1.5	–	–	V
Input Leakage Current[2]	I_{IN}	EN = PWM = 5 V		–	100	–	µA
Driver Section							
High Side Gate Drive On Resistance	$R_{DS(on)H}$	Measured at $V_{GATE} = V_{IN} / 2$		–	9	–	Ω
Low Side Gate Drive On Resistance	$R_{DS(on)L}$	Measured at $V_{GATE} = V_{IN} / 2$		–	10	–	Ω
Driver to GND Resistance During Shutdown	R_{SDOFF}			–	125	–	kΩ
Sense Overcurrent Threshold Voltage	V_{SEN}	$V_{SENP} – V_{SENN}$		80	95	110	mV
LED Current Sinks							
LEDx Pin Regulation Voltage	V_{LEDx}	I_{LED} = 80 mA		–	1	–	V
I_{SET} to I_{LEDx} Current Gain	A_{ISET}	I_{SET} = 100 µA		–	640	–	A/A
ISET Pin Voltage	V_{ISET}			–	1.235	–	V
I_{SET} Allowable Current Range[2]	I_{SET}		•	41	–	125	µA
LEDx Accuracy[3]	Err_{ILEDX}	LED1 through LED6 = 1 V, at 100% Current	•	–3	±0.6	3	%
LEDx Matching[4]	ΔI_{LEDX}	LED1 through LED6 = 1 V, I_{SET} = 100 µA	•	–3	±0.6	3	%
LEDx Switch Leakage Current[2]	I_{SL}	V_{LEDx} = 12 V, EN = 0		–	0.1	–	µA
Soft Start							
Soft Start Sense Threshold Voltage	V_{SENS}	Sense voltage for boost switch current sensing		–	28.5	–	mV
Soft Start LEDx Current Limit Relative to LED 100% Current	$I_{LED(SS)}$	Current through enabled LEDx pins during soft start		–	8	–	%

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued) Valid at V_{IN} = 5 V; T_A = 25°C, R_{FSET} = 52 kΩ, R_{ISET} = 12.4 kΩ, except • indicates specifications guaranteed over the full operating temperature range with $T_A = T_J$, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit
Protection Features							
Thermal Shutdown Threshold	T_{TSD}	T_J rising		–	165	–	°C
Short Circuit Detect Voltage	V_{SC}			–	18.7	–	V
Output Overvoltage Threshold	V_{OVP}	R_{OVP} = 0		–	36	–	V
OVP Pin Leakage Current[2]	I_{OVPLK}	V_{OVP} = 22 V, EN = V_{IL}		–	0.1	–	µA
Overvoltage Protection Sense Current[2]	I_{OVPH}			–	240	–	µA
$\overline{\text{FAULT}}$ Pin Output Leakage[2]	I_{FLT}	V = 5 V		–	–	1	µA
$\overline{\text{FAULT}}$ Pin Output Voltage	V_{OL}	I = 500 µA	•	–	–	0.4	V

[1]Typical specifications are at T_A = 25ºC.
[2]For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).
[3]LED accuracy is defined as (I_{SET} × 640 – I_{LED}(av)) / (I_{SET} × 640), I_{LED}(av) measured as the average of I_{LED1} through I_{LED6}.
[4]LED current matching is defined as (I_{LEDx} – I_{LED}(av)) / I_{LED}(av), with I_{LED}(av) as defined in footnote 3.

Characteristic Performance

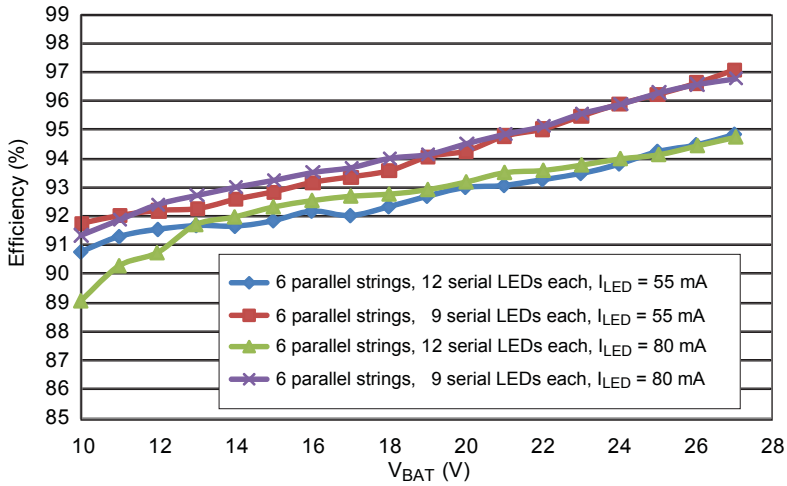


Figure 2. Efficiency versus Battery Voltage at various LED configurations, R_{FSET} = 105 kΩ (500 kHz), R_{ISET} = 14.3 kΩ (55 mA) or 10 kΩ (80 mA), Q1 = FQB17N08L, L1 = 10 µH

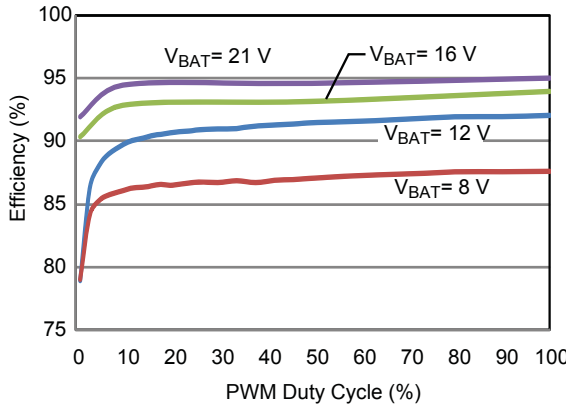


Figure 3. Efficiency versus PWM Duty Cycle at various V_{BAT} levels, 5 parallel strings with 9 series LEDs each, I_{LED} = 55 mA per channel

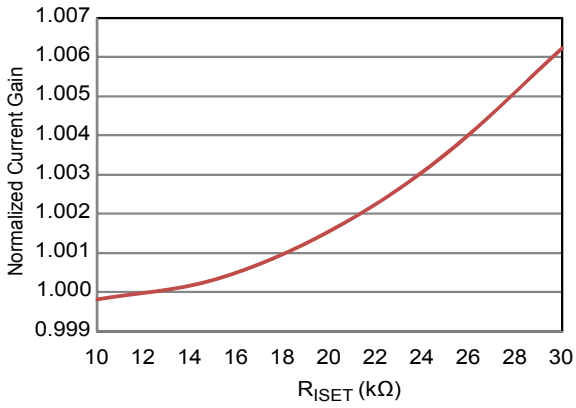


Figure 4. Normalized Current Gain versus R_{ISET} , normalized to 1 for R_{ISET} = 12.4 kΩ

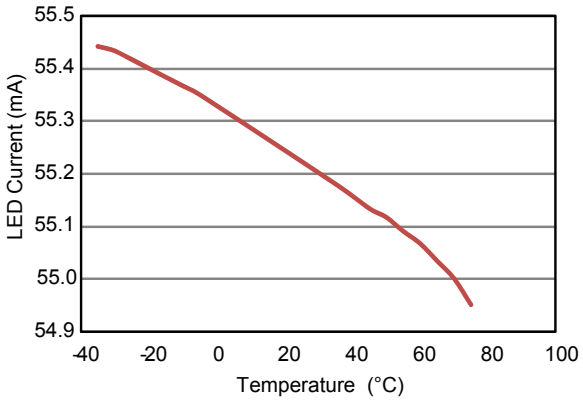


Figure 5. LED Current versus Ambient Temperature, R_{ISET} = 14.3 kΩ

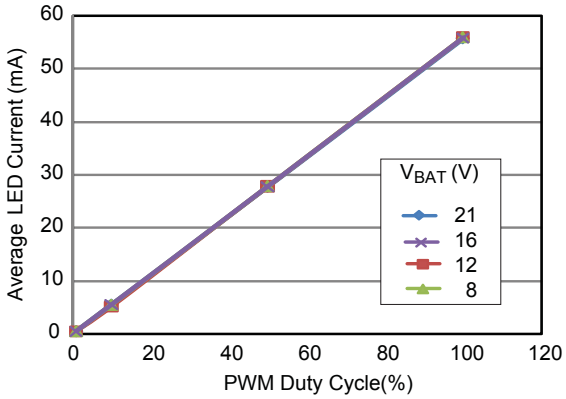


Figure 6. Average LED Current versus PWM Duty Cycle at various V_{BAT} levels, 6 parallel strings with 9 series LEDs each, I_{LED} = 55 mA per channel, f_{PWM} = 200 Hz

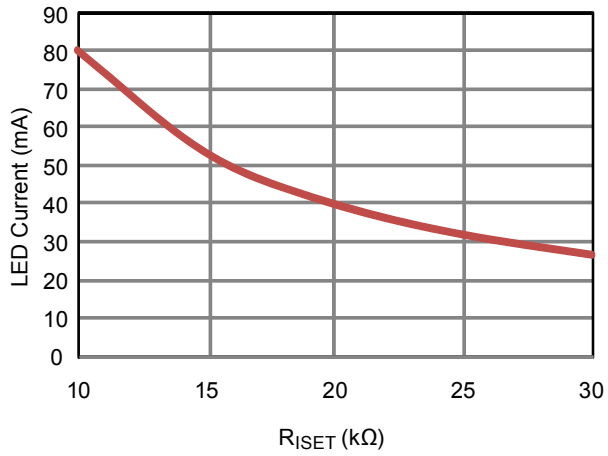


Figure 7. LED Current versus R_{ISET}

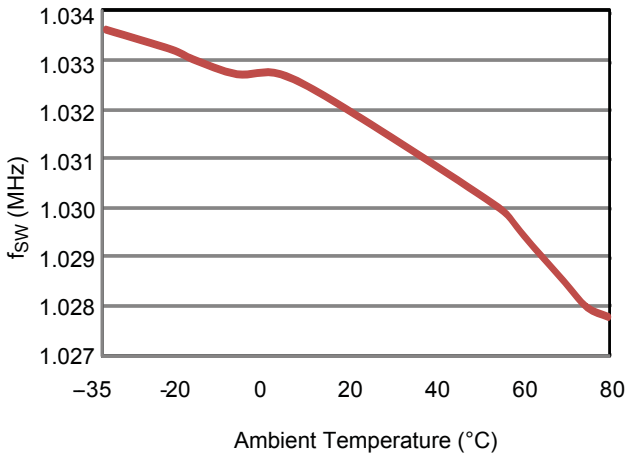


Figure 8. Switching Frequency versus Ambient Temperature

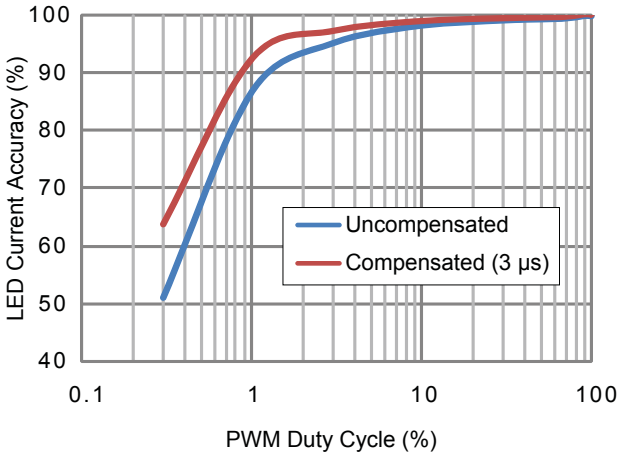


Figure 9. LED Current Accuracy versus PWM Duty Cycle, LED Current Accuracy normalized to the 100% Current level, V_{BAT} = 12 V, 6 parallel strings with 9 series LEDs each, I_{LED} = 55 mA per channel f_{PWM} = 200 Hz

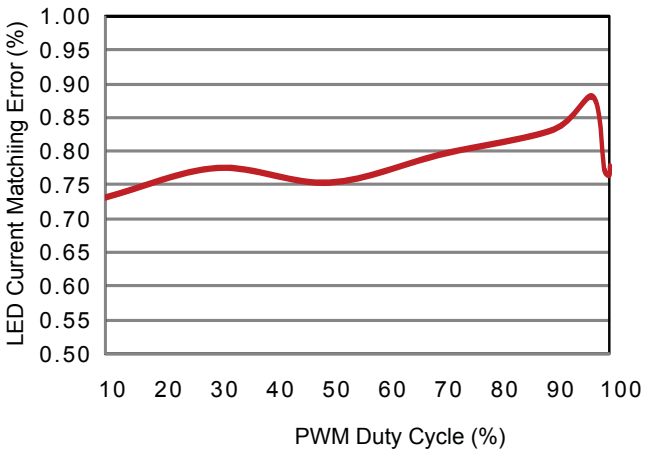


Figure 10. LED Current Matching Error versus PWM Duty Cycle, V_{BAT} = 12 V, 6 parallel strings with 9 series LEDs each, I_{LED} = 55 mA per channel, f_{PWM} = 200 Hz

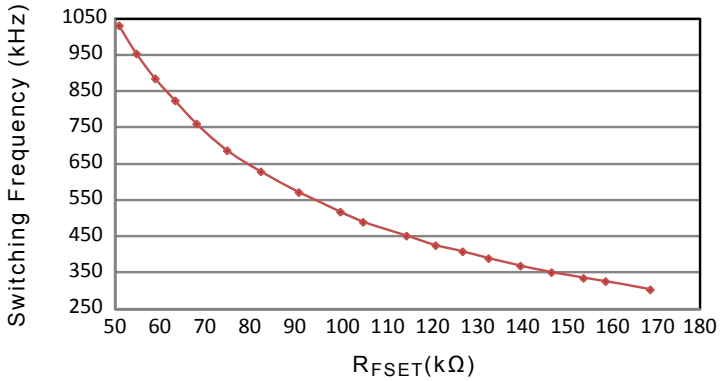
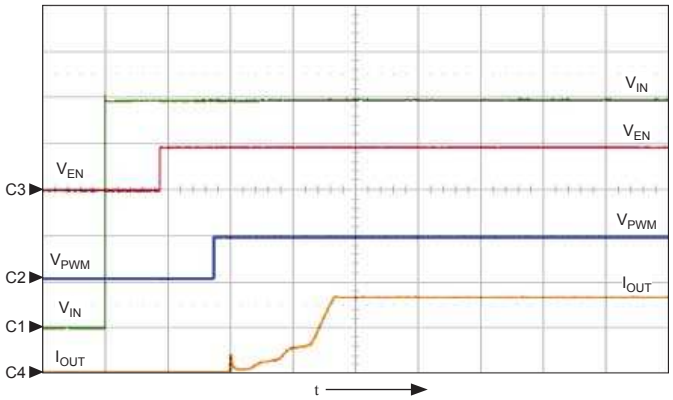


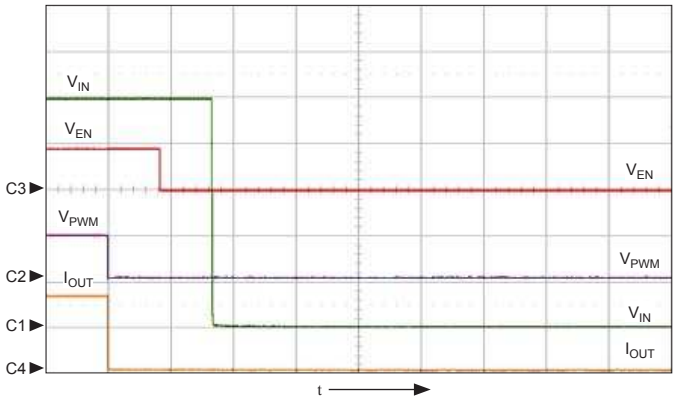
Figure 11. Switching Frequency versus R_{FSET}

Typical Power Sequencing Waveforms

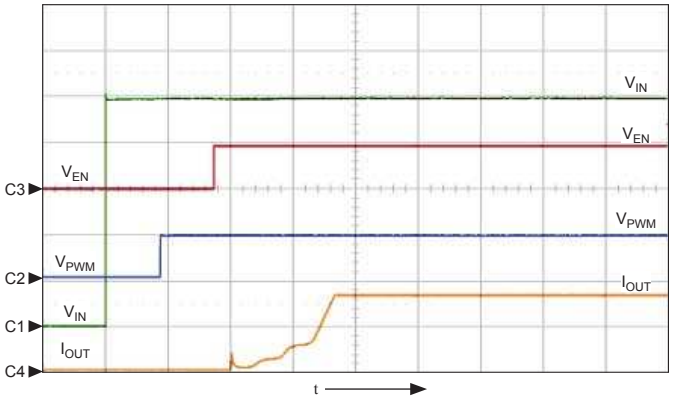
Turn-on sequence
$V_{IN} – V_{EN} – V_{PWM}$



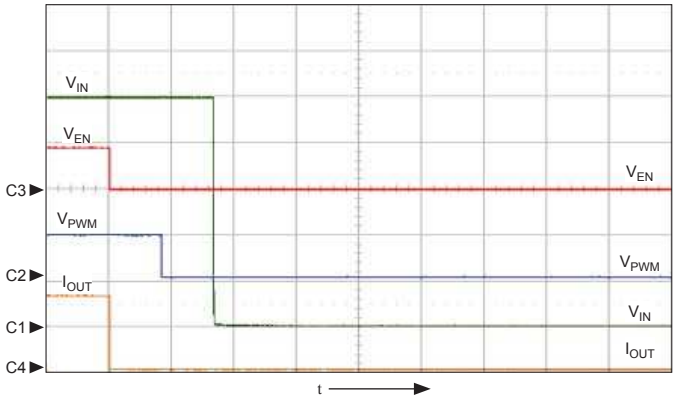
Turn-off sequence
$V_{PWM} – V_{EN} – V_{IN}$



Turn-on sequence
$V_{IN} – V_{PWM} – V_{EN}$



Turn-off sequence
$V_{EN} – V_{PWM} – V_{IN}$



C1: V_{IN}, 1 V / div.
C2: V_{PWM}, 5 V / div.
C3: V_{EN}, 5 V / div.
C4: I_{OUT}, 200 mA / div.
Time: 2 ms / div.

Fig 12. Alternative Turn-On and Turn-Off sequences: (top) $V_{EN} –V_{PWM} –V_{EN}$, (bottom) $V_{VPWM} –V_{EN} –V_{PWM}$, with 6 parallel strings with 9 series LEDs each, V_{BAT} = 12 V, V_{PWM} = 5 V (100% Current), V_{IN} = 5 V, V_{EN} = 5 V, I_{LED} = 55 mA per channel

Functional Description

Overview The A8507 is a multi-output WLED/RGB controller for backlighting medium-size displays. It has a integrated gate driver for driving an external N-channel boost MOSFET. The boost controller is fixed frequency current mode converter. The switching frequency can be set in the range from 250 kHz to 1 MHz, by an external resistor, R_{FSET}, connected between FSET and ground.

The external MOSFET switch is protected by pulse-by-pulse current limiting. The current limit is independent of duty cycle, and is set using an external sense resistor, R_{SC}.

The A8507 has six well-matched current sinks that provide regulated current through the LEDs for uniform display brightness. The boost converter is controlled by monitoring all LEDx pins simultaneously and continuously.

LED Current Setting The maximum LED current can be set, at up to 80 mA/channel, through the ISET pin. Connect a resistor, R_{ISET}, between this pin and ground to set the reference current level, I_{SET}. The value of I_{SET} (mA) is determined by:

$$I_{SET} = 1.235 / R_{ISET}\ (k\Omega) \quad . \qquad (1)$$

The resulting current is multiplied internally with a gain of 640 and mirrored on all enabled LEDx pins. This sets the maximum current through each LEDx, referred as the *100% Current*. The LEDx current can be reduced from the 100% Current value by applying an external PWM signal on the PWM pin.

Boost Switching Frequency Setting Connect an external resistor between the FSET pin and GND, to set boost switching frequency, f_{SW} . The value of f_{SW} (MHz) is determined by:

$$f_{SW} = 52 / R_{FSET} \quad , \qquad (2)$$

where f_{SW} is in MHz and R_{FSET} is in kΩ.

Enable The IC turns on when a high signal is applied on the EN pin, and turns off when this pin is pulled low.

PWM Dimming The A8507 has a very wide range for PWM signal input. It can accept a PWM signal from 100 Hz to 5 kHz. When a PWM high signal is applied, the LEDx pins sink 100% Current. When the PWM signal is low, the LED sinks turn off.

Referring to figure 13, there is a ramp-up delay between when the PWM signal is applied and when the current reaches the 90% level. To improve current dimming linearity for PWM pulse widths less than 100 µs, increase the applied PWM pulse-width by 3 µs to compensate for this delay.

Startup Sequence When EN is pulled high, the IC enters soft start. The IC first tries to determine which LEDx pins are being used, by raising the LEDx pin voltage with a small current. After a duration of 512 switching cycles, the LEDx pin voltage is checked. Any LEDx channel with a drain voltage smaller then 100 mV is removed from the control loop.

After the first PWM positive trigger, the boost current is limited to 35% of normal value and all active LEDx pins sink $^1/_{12}$ of the set current until output voltage reaches sufficient regulation level. When the device comes out of soft start, boost current and the LEDx pin currents are set to normal operating level. Within a few cycles, the output capacitor charges to the voltage required to supply full LEDx current. After output voltage, V_{OUT}, reaches the required level, LEDx current toggles between 0% and 100% with each PWM command signal.

In case of a heavy overload on V_{OUT} at startup, the device will stay in soft start mode indefinitely, as the output voltage cannot rise to the LED regulation level.

LED Short Detect Any LEDx pins that have a voltage exceeding the Short Circuit Detect Voltage, V_{SC} , cause the device to shut down and this condition is latched. This faults occurs when multiple LEDs short. In case only a few LEDs short, the IC will continue to work as long as power dissipation in the IC is limited.

Overvoltage Protection The A8507 has an adjustable overvoltage protection feature to protect the external MOSFET against output overvoltage. The overvoltage level can be set, from 36 V to a higher voltage, with an external resistor, R_{OVP}. When the current though the OVP pin exceeds 240 µA, internal OVP comparator goes high and the device shuts down. The OVP

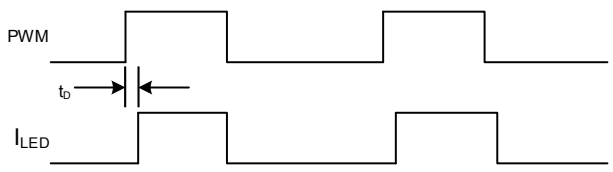


Figure 13. Propagation delay from the PWM signal rising edge to I_{LEDx} reaching the 90% level

fault disables all LEDx strings that are below regulation, thus preventing them from controlling the boost output voltage.

Calculate the value for R_{OVP} (Ω) as follows:

$$R_{OVP} = (V_{OVP} - 36) / 240\ \mu A\ , \quad (3)$$

where V_{OVP} is the required OVP level in V.

Open LED Protection Unused LEDx pins should be connected to GND. During normal operation, if any enabled LED string opens, voltage on the corresponding LEDx pin goes to zero. The boost loop operates in open loop till the OVP level is reached. The A8507 identifies the open LED string when overvoltage is detected. Open strings are then removed from the regulation loop. Afterwards, the boost controller operates in normal manner, and the output voltage is regulated to drive the remaining strings. If the open LED string is reconnected, it will sink current up to the programmed current level.

Note: Open strings are removed from boost regulation, but not disabled. This keeps the string in operation if LEDs open for only a short length of time, or reach OVP level on a transient event.

The disconnected string can be restored to normal mode by reenabling the IC. It can also be restored to normal operation if the fault signal is removed from the corresponding LEDx pin, but an OVP event occurs on any other LEDx pin.

Overcurrent Protection The IC provides pulse-by-pulse current limiting for the boost MOSFET. The current limit level, I_{SC} (A), can be set by selecting the external resistor, R_{SC} (Ω):

$$R_{SC} = 0.095 / I_{SC}\ . \quad (4)$$

If the boost output voltage is unable to reach the regulation target even when the switch is operating at maximum current limit, the boost control loop will force the compensating capacitor, C_{COMP}, to rise in voltage until it reaches the overcurrent fault level (3.4V approximately). The overcurrent fault forces the device into soft start.

Channel Selection The A8507 can be used to drive 1 to 6 LED channels. During startup, the IC detects LED sink pins which are shorted to ground, and disables the corresponding LED channel. Therefore, any unused LED pins must be connected to ground, otherwise the IC will go into overvoltage protection fault during startup. LED pins can be paralleled together for higher current. For example for a 3 parallel string configuration, connect LED1-2, LED3-4, and LED5-6 together to deliver up to 160 mA per LED.

Thermal Shutdown (TSD) The IC shuts down when junction temperature exceeds 165°C. It will recover automatically when the junction temperature falls below 125°C.

VIN Undervoltage Lockout (UVLO) The device is shut down when input voltage, V_{IN}, falls below V_{UVLO}.

Fault Mode The IC functions in various fault states:

Fault State	Auto-Restart	Description
Over-voltage Protection	Yes	Fault occurs when OVP pin exceeds the V_{OVP} threshold. Used to protect the output voltage from damaging the part.
Pulse-by-Pulse Current Limit	Yes	Fault occurs when the current through the external MOSFET increases exceeds such that the voltage across the SENP and SENN pins exceeds 95 mV typical. The MOSFET switch is turned off on a cycle-per-cycle basis.
Overcurrent Protection	Yes	Fault occurs when the COMP pin exceeds the overcurrent detect threshold. Multiple pulse-by-pulse current limits will result in the COMP pin voltage to rise. After a time period determined by the COMP pin current and the output capacitor, C_{OUT}, the COMP voltage will exceed the overcurrent detect threshold, forcing a fault.
Over-temperature Protection	Yes	Fault occurs when the die temperature exceeds the over-temperature threshold, 165°C typical.
LED Short Protection	No	Fault occurs when the LED pin voltage exceeds V_{SC}, 18.7 V typical.
VIN UVLO	No	Fault occurs when VIN drops below V_{UVLO}, 4.0 V typical. This fault resets all latched faults.

Application Information

PCB Layout Guidelines As with any switching power supply, care should be taken in laying out the board. A switching power supply has sources of high dv/dt and high di/dt which can cause malfunction. All general norms should be followed for board layout. Refer to figure 14 for a typical application schematic. The A8507 evaluation board provides a useful model for designing application circuit layouts.

The following guidelines should be observed:

- Place the supply bypass capacitor (C5) close to the VIN pin and the ground plane.
- Route analog ground, digital signal ground, LED ground (LGND pin), and power ground (PGND pin) separately. Connect all these grounds at the common ground plane under the A8507, serving as a star ground.
- Place the input capacitors (C1, C2), inductor (L1), boost diode (D1), MOSFET (Q1), and output capacitors (C3, C4) so that they form the smallest loop practical. Avoid long traces for these paths.
- Place the resistors R_{FSET} and R_{ISET}, and the compensation components (Rz and Cz) close to the FSET, ISET, and COMP pins, respectively. Connect the other ends to the common star ground.
- A8507 has 50 kΩ internal pull-down resistors on the EN and PWM pins to keep these pins low while driving through tri-state state (for example, shutdown). Add external resistors R2 and R3 between the EN and PWM pins and ground, for added noise immunity. Connect these resistors close to the pins and return to the common star ground.
- Sense voltage across R_{SC} with smaller length traces. Place the SENP and SENN traces as close to each other as possible to minimize noise pickup. Connect the SENN trace to the negative end of the resistor and do not connect it to power ground plane.
- Provide a substantial copper plane near MOSFET Q1 and the IC, to provide good thermal conduction.
- Place R_{OVP} as close as possible to the OVP pin. A long trace between R_{OVP} and the OVP pin may pick up switching noises and cause overvoltage protection to trip prematurely.

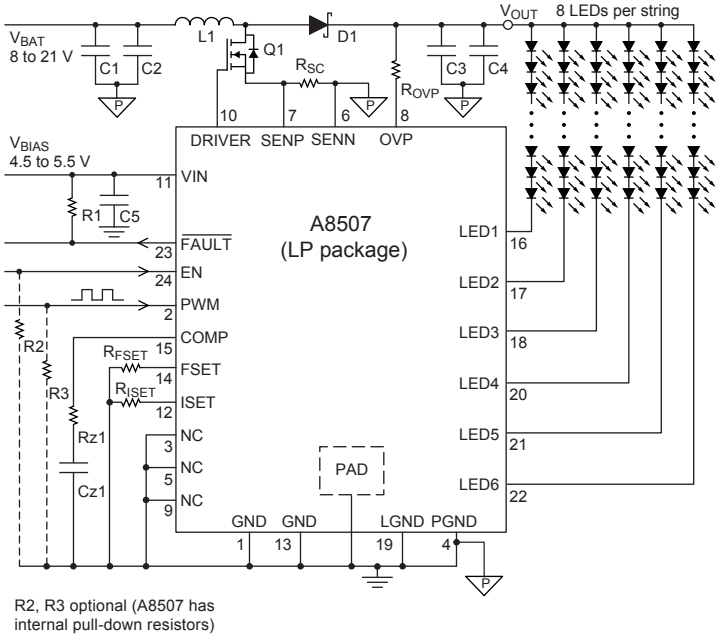
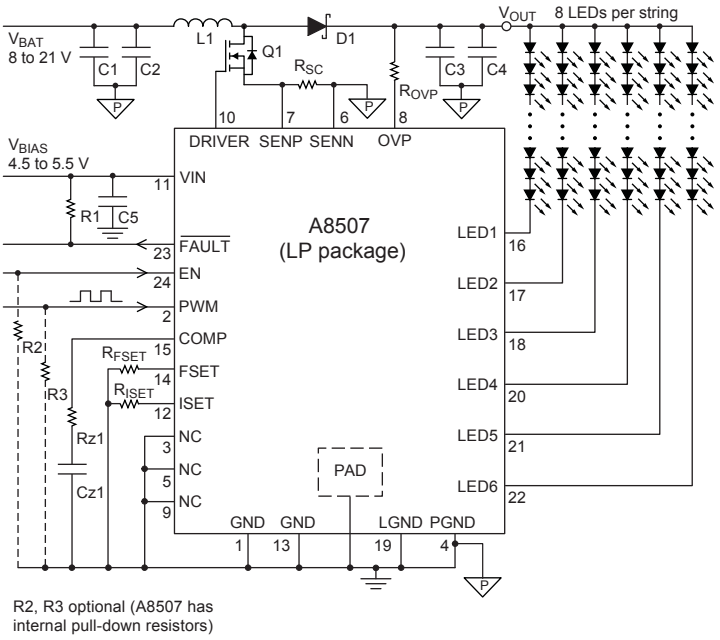
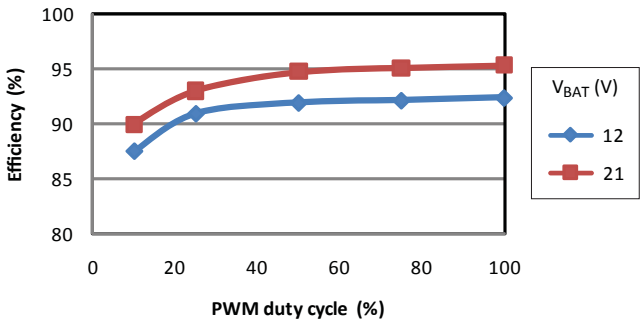


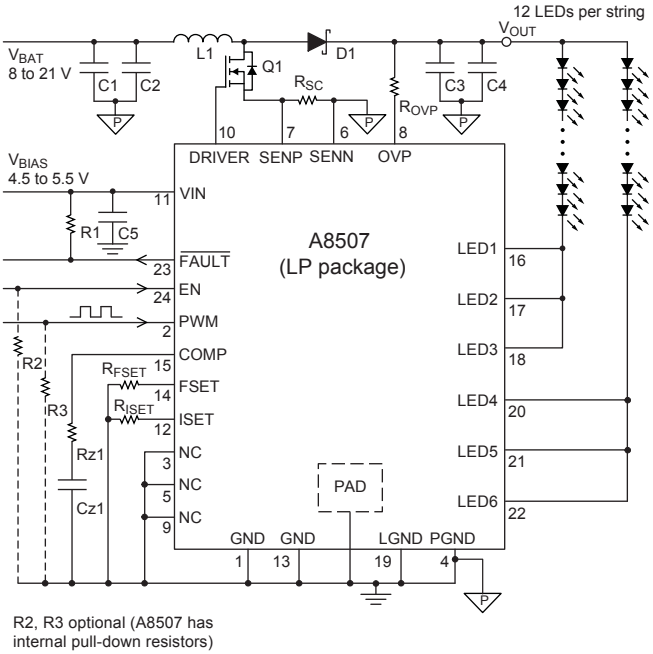
Figure 14. Typical application circuit

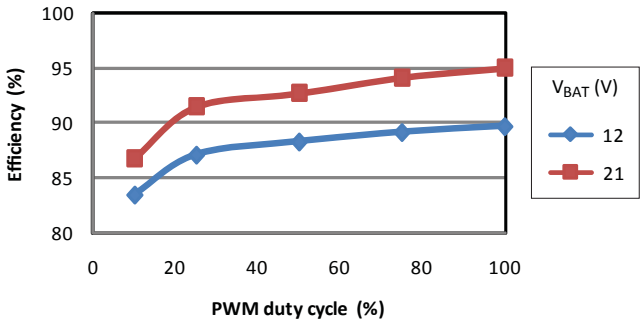




R_{ISET} = 10.0 kΩ, R_{FSET} = 51 kΩ,
R_{OVP} = 0 Ω, Q1=FQB17N08L

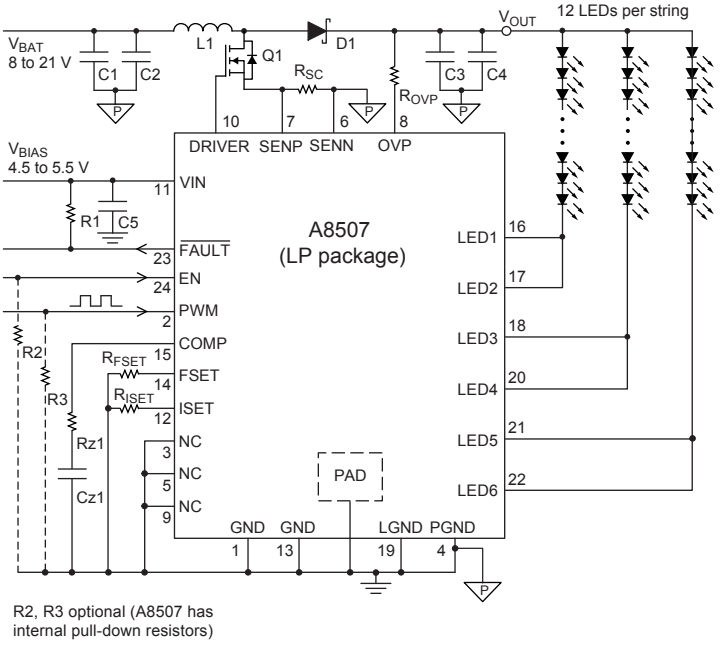
Figure 15. Typical Application with 6 parallel strings, 8 series LEDs each, 80 mA per channel

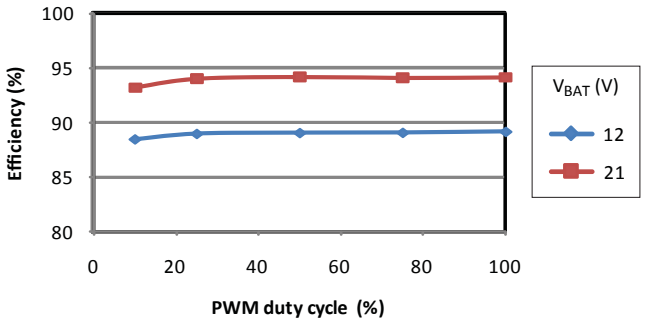




R_{ISET} = 10.0 kΩ, R_{FSET} = 51 kΩ,
R_{OVP} = 36 kΩ, Q1=FQB17N08L

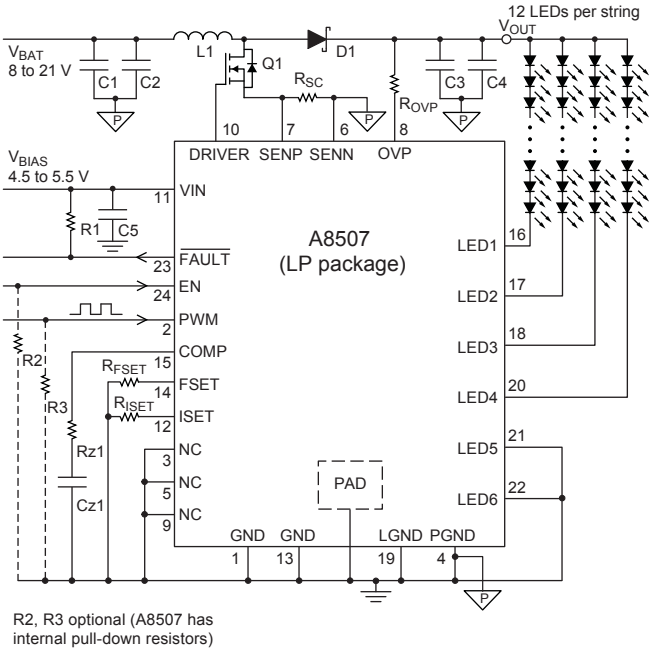
Figure 16. Typical Application with 2 parallel strings, 12 series LEDs each, 240 mA per channel

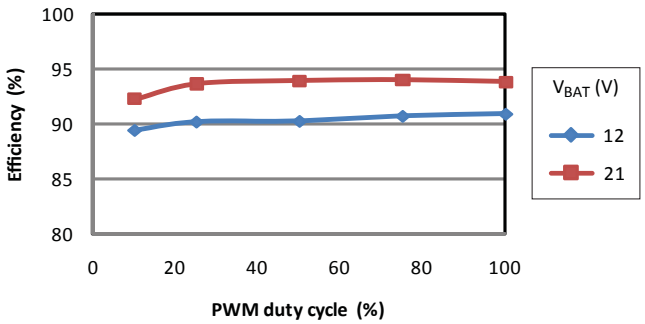




R_{ISET} = 10.0 kΩ, R_{FSET} = 51 kΩ,
R_{OVP} = 36 kΩ, Q1=FQB17N08L

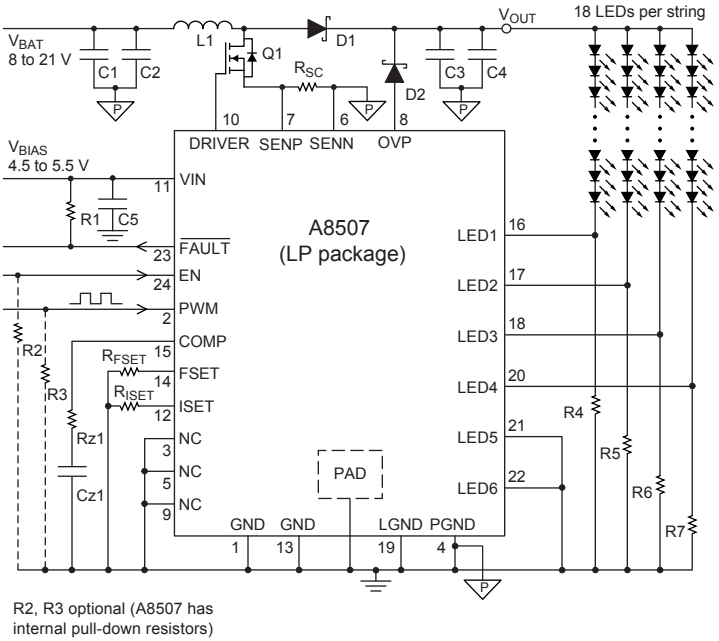
Figure 17. Typical Application with 3 parallel strings, 12 series LEDs each, 160 mA per channel



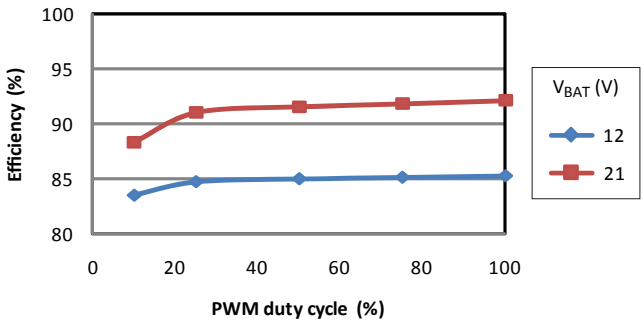


R_{ISET} = 10.0 kΩ, R_{FSET} = 51 kΩ,
R_{OVP} = 36 kΩ, Q1=FQB17N08L

Figure 18. Typical Application with 4 parallel strings, 12 series LEDs each, 80 mA per channel



R2, R3 optional (A8507 has internal pull-down resistors)



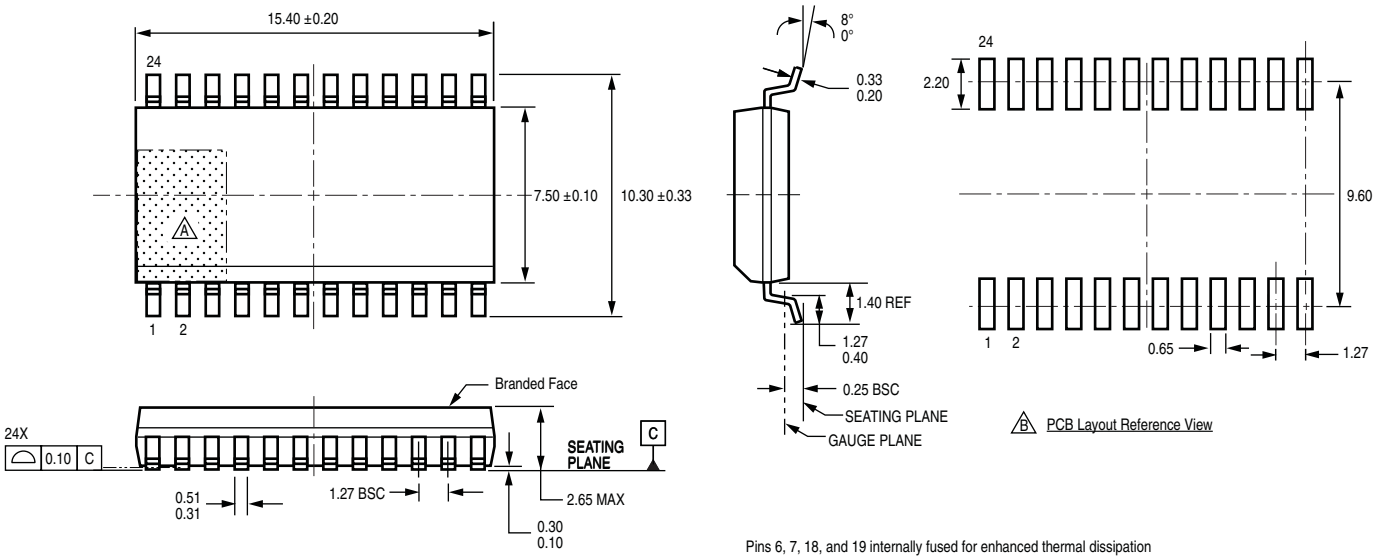
R_{ISET} = 10.0 kΩ, R_{FSET} = 51 kΩ,
D2 = 30 V Zener, Q1=FQB17N08L

For higher output voltage, the voltage on the LEDx pins during PWM off-time may exceed the rated voltage. Connect a resistor from the LEDx pin to GND. Recommended values are:

- C3 = 2.2 µF / 100 V ceramic
- C4 = 10 µF / 100 V electrolytic
- R4 through R7 = 25 kΩ, 0603

Figure 19. Typical Application with 4 parallel strings, 18 series LEDs each, 80 mA per channel

Package LB 24-Pin SOICW with Internally Fused Pins



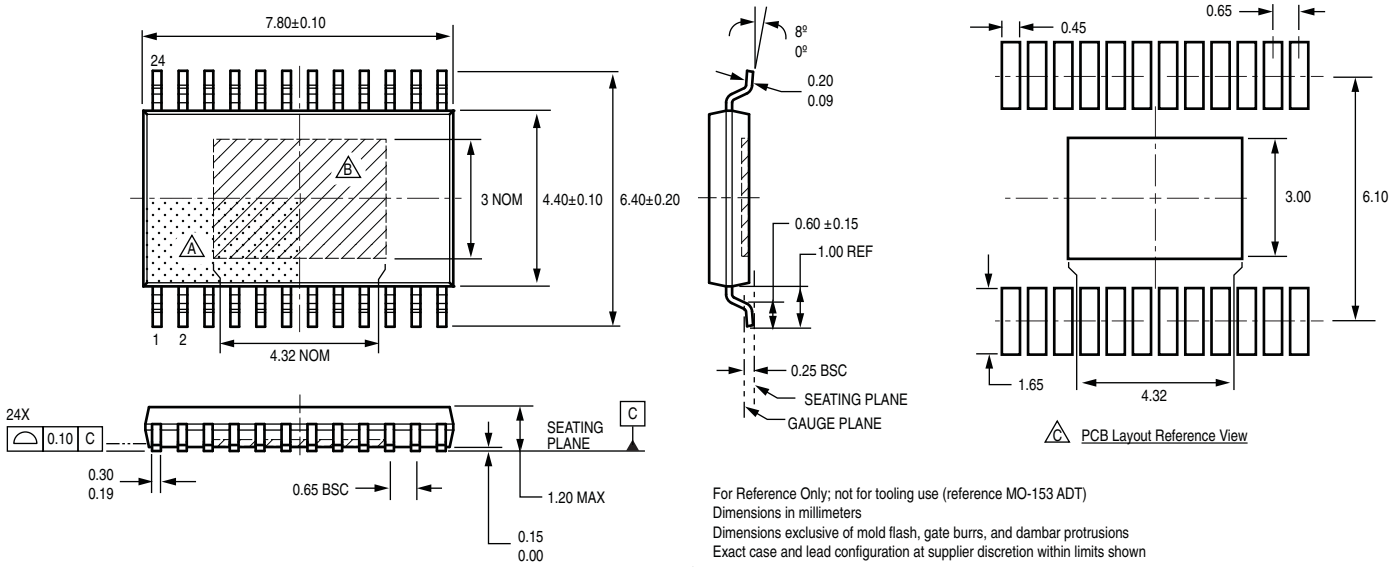
Pins 6, 7, 18, and 19 internally fused for enhanced thermal dissipation

For Reference Only; not for tooling use (reference MS-013AD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Package LP 24-Pin TSSOP with Exposed Thermal Pad



For Reference Only; not for tooling use (reference MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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