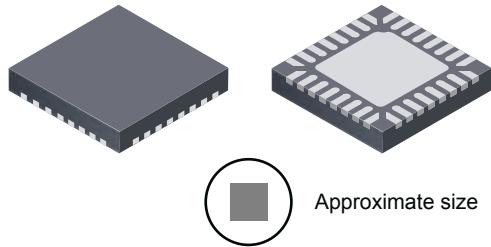


# **Dual DMOS Full Bridge Motor Driver With Serial Port Control and Dual Regulators**

## Features and Benefits

- 3.3/5 V switching regulator
- 1 to 2.5 V configurable linear regulator output
- Dual DMOS full bridge: drive two DC motors or a single stepper motor
- $\pm 1.5$  A, 50 V output rating per bridge
- 4-bit microstepping capability
- Serial port control
- Configurable mixed, fast, and slow current decay
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection
- OCP protection

## Package: 32-contact QFN (suffix ET)



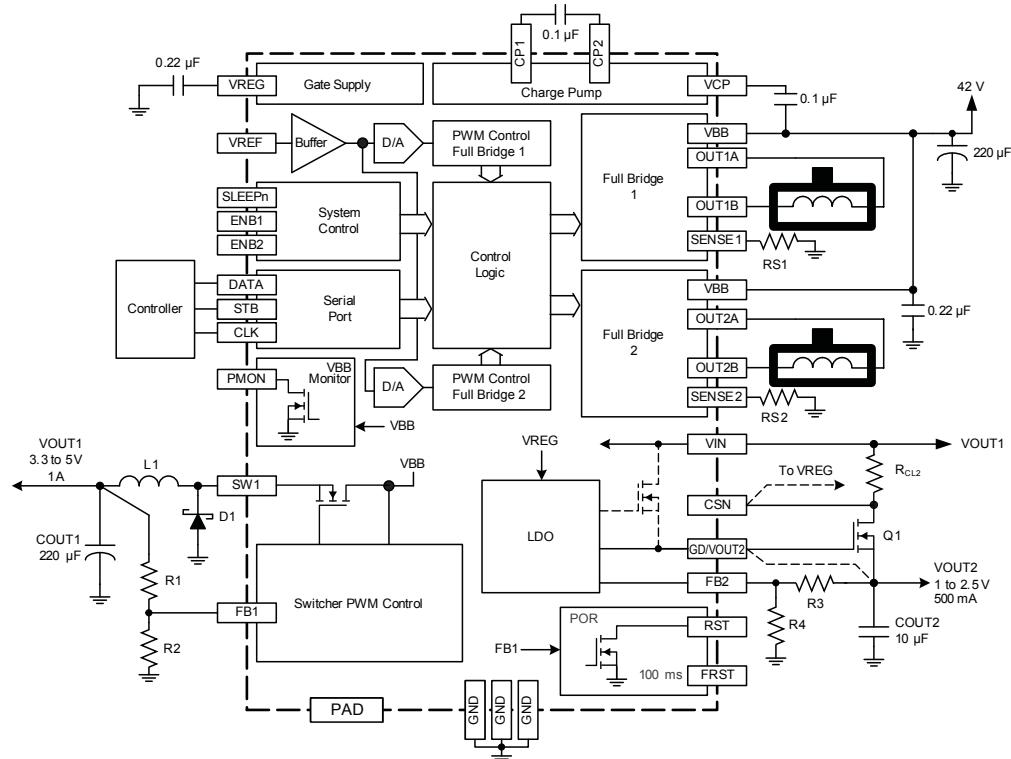
## Description

Designed to provide the motor driver and power supply requirements for printers and office automation equipment. This integrated power IC incorporates two high current, high performance, full bridge outputs, capable of 1.5 A at 50 V. Additionally two power supply rails are provided for microprocessor or DSP supplies. A switching buck regulator steps the supply down to a low voltage output that is adjustable from 3.3 to 5 V. This voltage can be used to supply external 5 V rails, it also feeds back into the part and supplies the integrated linear regulator which is adjustable from 1 to 2.5 V.

The A3998 serial port provides flexible configuration for the dual full bridge motor driver. Two full bridges can be programmed to control one stepper motor or two DC motors. Both bridges have integrated fixed off-time PWM control with programmable decay mode selection.

The A3998 is supplied in a low profile, 32-contact QFN, 5 × 5 mm, 0.90 mm nominal height, with exposed thermal pad (suffix ET). The package is lead (Pb) free with 100% matte-tin leadframe plating.

## Functional Block Diagram



### Selection Guide

Part Number	Packing*
A3998SETTR-T	1500 pieces per 7-in. reel

\*Contact Allegro® for additional packing options



### Absolute Maximum Ratings\*

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	$V_{BB}$		50	V
Output Current	$I_{OUT}$	Motor, DC	1.5	A
		Pulsed, $t_W < 1 \mu s$	6	A
Sense Voltage	$V_{SENSE}$	DC	0.52	V
		$t_W < 1 \mu s$	2.5	V
SW1 Pin Voltage	$V_{SW}$		-1 to 50	V
Logic Pins Voltage Range	$V_{IO}$		-0.3 to 5.5	V
VIN Pin Voltage	$V_{IN}$		-0.3 to 6	V
FB Pins Voltage Range	$V_{FB}$		-0.3 to 5.5	V
VREF Pin Voltage Range	$V_{REF}$		-0.3 to 5.5	V
PMON, RST Pins Voltage Range	$V_{RST}$		-0.3 to 5.5	V
VREG Pin Voltage Range	$V_{REG}$		-0.3 to 8	V
Operating Ambient Temperature	$T_A$	S temperature range	-20 to 85	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

**Thermal Characteristics** may require derating at maximum conditions, see application information

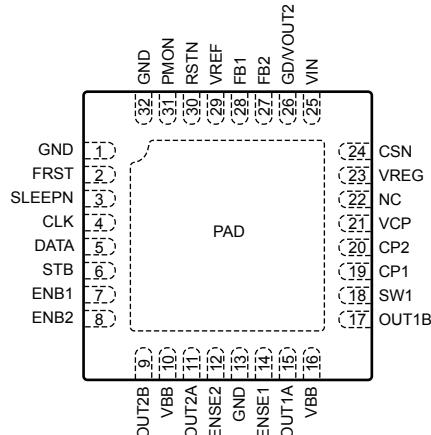
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{QJA}$	4-layer PCB based on JEDEC standard	30	°C/W
		Estimated, on 2-layer PCB with 1 in. <sup>2</sup> of copper area each side	55	°C/W

\*Additional thermal information available on the Allegro website

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### Pin-out Diagram



**Terminal List Table**

Number	Name	Function	Number	Name	Function
1,13,32	GND	Ground	18	SW1	DC to DC switch output
2	FRST	Control logic input	19	CP1	Charge pump capacitor terminal
3	SLEEPN	Control logic input, active low	20	CP2	Charge pump capacitor terminal
4	CLK	Control logic input	21	VCP	Reservoir capacitor terminal
5	DATA	Control logic input	22	NC	No connect
6	STB	Control logic input	23	VREG	Gate supply
7	ENB1	Control logic input	24	CSN	Current Sense/Reg select
8	ENB2	Control logic input	25	VIN	Logic supply/ LDO supply
9	OUT2B	DMOS full bridge 2, output B	26	GD/OUT2	Gate drive output / VOUT2
10, 16	VBB	Motor and switcher supply voltage	27	FB2	Feedback for VOUT2
11	OUT2A	DMOS full bridge 2, output A	28	FB1	Feedback for VOUT1
12	SENSE2	Sense resistor terminal, bridge 2	29	VREF	Analog input
14	SENSE1	Sense resistor terminal, bridge 1	30	RSTN	Reset flag output
15	OUT1A	DMOS full bridge 1, output A	31	PMON	Power monitor flag output
17	OUT1B	DMOS full bridge 1, output B	–	PAD	Exposed thermal pad

ELECTRICAL CHARACTERISTICS<sup>1,2</sup> Valid at  $T_J = 25^\circ\text{C}$ ,  $V_{BB} = 50\text{ V}$ ; unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. <sup>3</sup>	Max.	Unit
Load Supply Voltage Range	$V_{BB}$	Operating	9	—	50	V
Bridge Output On-Resistance	$R_{DS(on)RG}$	Source driver, $I_{OUT} = -1.5\text{ A}$	—	0.5	—	$\Omega$
		Sink driver, $I_{OUT} = 1.5\text{ A}$	—	0.5	—	$\Omega$
VBB Pins Supply Current	$I_{BB}$	$V_{REG}$ regulated, $I_{OUT} = 0\text{ mA}$ , outputs on, PWM = 50 kHz, Duty Cycle = 50%	—	5	10	mA
	$I_{BBS}$	Standby mode, regulator active	—	—	5	mA
VIN Pin Supply Current	$I_{IN}$		—	5	8	mA
<b>Control Logic</b>						
Logic Inputs Voltage Range	$V_{IO}$	Operating	3	—	5.5	V
Logic Input Voltage	$V_{IO(1)}$		$V_{DD} \times 0.55$	—	—	V
	$V_{IO(0)}$		—	—	$V_{DD} \times 0.27$	V
Logic Pins Input Current (Except ENB1,ENB2, FRST pins)	$I_{IO}$	$V_{IN} = 0$ to 5 V	-20	<1.0	20	$\mu\text{A}$
ENB1,ENB2, FRST Pins Input Current	$I_{IO(1)}$	$V_{IN} = 3.3\text{ V}$	—	66	100	$\mu\text{A}$
	$I_{IO(0)}$	$V_{IN} = 0.8\text{ V}$	—	16	40	$\mu\text{A}$
Input Hysteresis	$V_{IOHYS}$		200	—	700	mV
Propagation Delay Time	$t_{pd}$	PWM change to source on	350	550	1000	ns
		PWM change to source off	35	—	250	ns
		PWM change to sink on	350	550	1000	ns
		PWM change to sink off	35	—	250	ns
Crossover Delay	$t_{COD}$		300	425	1000	ns
<b>Supply Monitor</b>						
Reset Timer	$t_{POR}$		70	100	130	ms
RSTN and PMON Pins Output Voltage	$V_{RST}$	$I_{OUT} = 1\text{ mA}$	—	—	0.5	V
RSTN and PMON Pins Output Leakage Current	$I_{leakage}$	$V_{OUT} = 5\text{ V}$	—	—	1	$\mu\text{A}$
Power Monitor Threshold	$V_{PM(th)}$	PMON pin, $V_{BB}$ falling	12	13	14	V
Power Monitor Hysteresis	$V_{PMHYS}$		—	2	—	V
<b>Protection Circuits</b>						
VIN Pin UVLO Threshold	$V_{INUV(th)}$	$V_{IN}$ rising	—	2.8	3	V
VIN Pin UVLO Hysteresis	$V_{INUVHYS}$		—	100	—	mV
VBB Pins UVLO Threshold	$V_{BBUV(th)}$	$V_{BB}$ rising	6.6	7.1	7.6	V
VBB Pins UVLO Hysteresis	$V_{BBUVHYS}$		0.7	0.9	1.1	V
FB1 Pin UVLO Threshold	$V_{FBUV(th)}$	$V_{FB}$ falling	698	735	772	mV
FB1 Pin UVLO Hysteresis	$V_{FBUVHYS}$		—	100	—	mV
Thermal Shutdown Temperature	$T_{JSD}$		155	165	175	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{JSDHYS}$		—	20	—	$^\circ\text{C}$

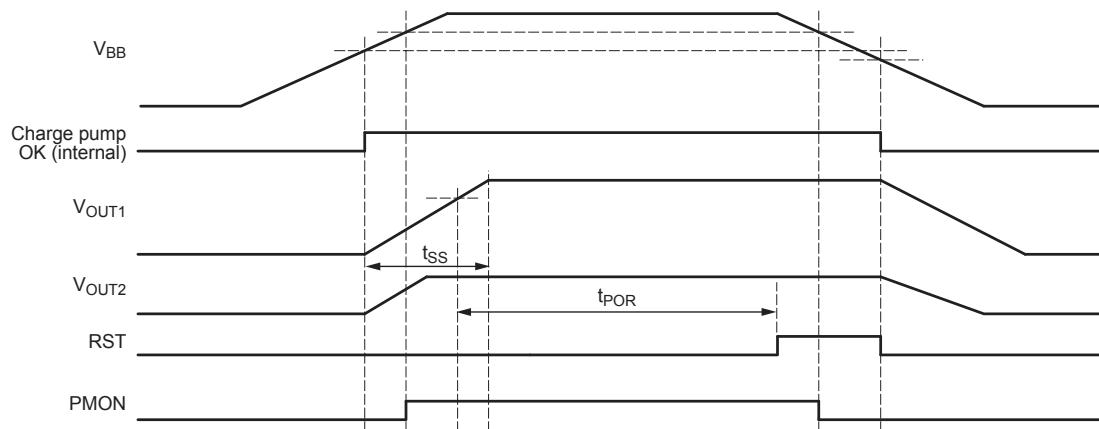
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ELECTRICAL CHARACTERISTICS<sup>1,2</sup> (continued) Valid at  $T_J = 25^\circ\text{C}$ ,  $V_{BB} = 50\text{ V}$ ; unless otherwise specified

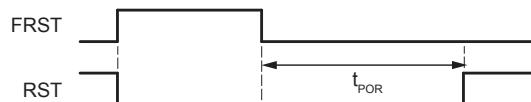
Characteristics	Symbol	Test Conditions	Min.	Typ. <sup>3</sup>	Max.	Unit
<b>DC to DC Converter</b>						
Feedback Voltage Regulation <sup>4</sup>	$V_{FB1}$	Does not include Cycle Skipping mode ( $V = 9$ to $50\text{ V}$ , $I = 100\text{ mA}$ to $1\text{ A}$ )	0.98	1	1.02	V
		Cycle Skipping mode	0.95	1	1.05	V
Feedback Input Bias Current	$I_{FB1}$		-400	-	100	nA
Soft Start Duration	$t_{SS}$	$V_{BB} = 9\text{ V}$	5	10	15	ms
Current Limit	$I_{CLREG}$	$V_{FB} > 400\text{ mV}$	1.5	-	2.7	A
	$I_{CLFB}$	$V_{FB} < 400\text{ mV}$	.5	-	1.2	A
Fixed Off-time	$t_{OFF}$	$V_{OUT}$	-	4	-	$\mu\text{s}$
Buck Switch On-Resistance	$R_{DS(on)SW}$	$I = 1\text{ A}$ , $T_J = 25^\circ\text{C}$	-	0.6	-	$\Omega$
<b>Low Drop-Out Regulator</b>						
Feedback Voltage	$V_{FB2}$	$I = 0$ to $500\text{ mA}$	.98	1	1.02	V
Internal Current Limit	$I_{CL2}$	CSN connected to VREG	525	-	750	mA
External Current Limit Threshold	$V_{CL2}$	CSN connected to sense resistor	180	200	220	mV
VIN Pin Voltage Range	$V_{IN}$		$V_{OUT} + 0.6$	-	5.5	V
<b>Control Circuit</b>						
VREF Pin Input Voltage Range	$V_{REFRNG}$	Operating	0.0	-	2.6	V
Reference Input Current	$I_{REF}$	$V_{REF} = 2.0$ , $V_{BB} = 0$ to $50\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
Transconductance Error <sup>5</sup>	$Gm_{ERR}$	$V_{REF} = 2.0$ , DAC = 15	-4	-	4	%
		$V_{REF} = 2.0$ , DAC = 3	-10	-	10	%
Internal Oscillator Frequency	$f_{osc}$		3.4	4	4.6	MHz

<sup>1</sup>Negative current is defined as coming out of (sourcing) the specified device pin.<sup>2</sup>Specified limits are tested at a single temperature and assured over the range  $0^\circ\text{C}$  to  $125^\circ\text{C}$  by design and characterization.<sup>3</sup>Typical data is for design information only.<sup>4</sup>Average value of  $V_{OUT}$  relative to target.<sup>5</sup> $Gm_{ERR} = [(V_{REF} \times \text{Current\_Ratio} / 5) - V_{SENSE}] / (V_{REF} \times \text{Current\_Ratio} / 5)$ .

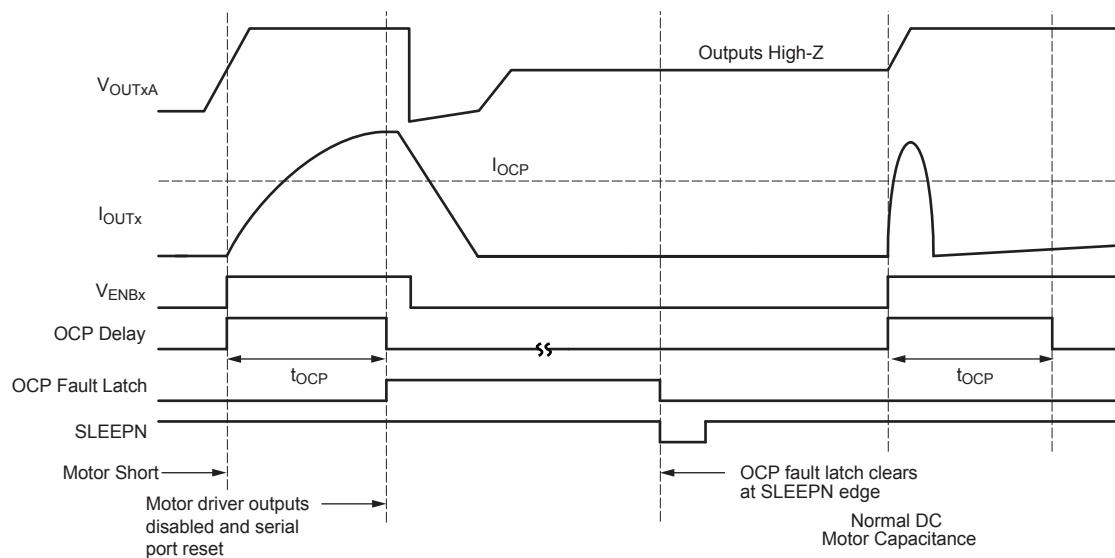
**Normal Power-up Timing Diagram**



**RST Function Timing with FRST Input**



**Overcurrent Protection (OCP) Timing Diagram**



## Functional Description

## Voltage Regulators

## Switching Regulator

An adjustable fixed off-time, peak current controlled buck regulator is used to provide external voltage to microprocessors or DSPs. The switcher output is fed back into the device and provides low voltage logic supply for the IC, improving overall efficiency. The regulator can operate in both continuous and discontinuous modes. An internal blanking circuit filters out transients due to the reverse recovery of the external clamp diode.

The switching regulator fixed off-time of approximately  $4\ \mu\text{s}$  is appropriate for the  $V_{\text{OUT}1}$  range from 3.3 to 5 V.

**Light Load Regulation** The switching regulator enters Cycle Skipping mode at light load conditions to maintain reasonable voltage regulation. As the output current decreases, there remains some energy that is stored during the power switch minimum on-time. The stored energy is transferred to the output capacitor and the output voltage begins to increase. To prevent energy

in the inductor from pumping the supply voltage up, the A3998 can skip PWM cycles. Cycle skipping mode can be activated any time there is discontinuous current in the inductor.

**Soft Start** An internal ramp generator and counter allow the output to ramp-up slowly. This limits the maximum demand on the external power supply by controlling the inrush current required to charge the external capacitor and any DC load at start-up. Internally, the ramp is set to 10 ms nominal rise time.

**Shorted Load** The regulator incorporates an overcurrent limit to handle shorted load conditions at the regulator output. For low output voltages at power-up, and in the case of a short, the off-time is extended to prevent loss of control of the current limit due to the minimum on-time of the switcher.

The overcurrent limit has a foldback feature to reduce the current limit when the output is overloaded (see figure 2). The voltage at the feedback pin (FB) is monitored to determine which current limit level to use. As the feedback voltage rises above approximately 400 mV, the foldback circuit is disabled.

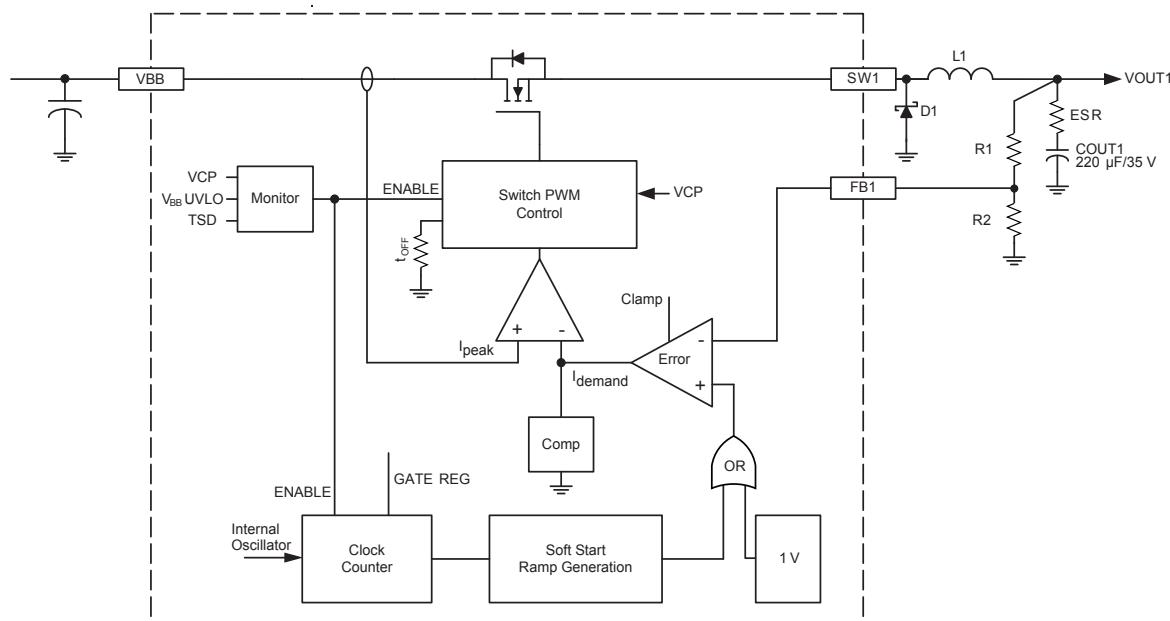


Figure 1. Implementation of switcher circuit; see table 3 for external component specifications.

**Linear Regulator**

An adjustable voltage rail from 1 to 2.5 V is integrated into the device. The switcher output is fed back into the device through the VIN pin and supplies the integrated linear pass element. To reduce power dissipation in the A3998, the linear regulator can be configured to drive the gate of an external N-channel FET. Using the external FET significantly reduces power dissipation in the IC and can allow the device to operate in high ambient temperature environments.

The regulator has two configurations: Internal mode and External mode. External mode is used to minimize power dissipation. In External mode current is limited by selection of the sense resistor, RCL. Internal mode is selected by connecting pin CSN to the

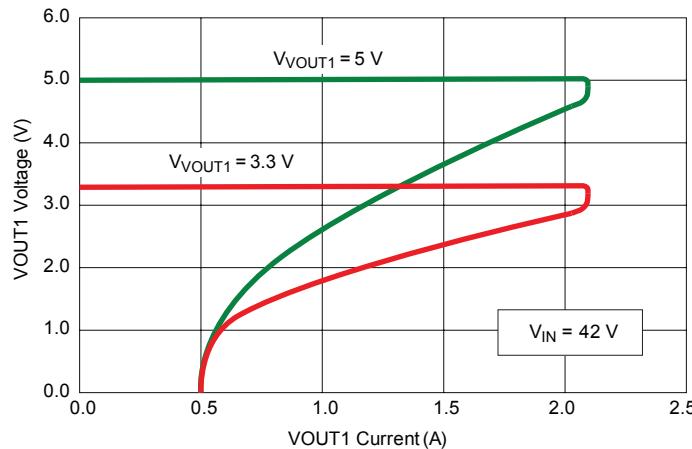


Figure 2. Switcher current limit with foldback

VREG pin. Both internal and external configurations are current limited.

**Internal Configuration** When the internal pass element is configured the internal current limit is fixed at  $I_{CL2}$ . The regulator has overcurrent protection with foldback. Figure 3 shows the  $I \cdot V$  characteristic of the linear regulator.

**External Configuration** When the external pass element is configured the current is adjustable by selecting the value of a current limit resistor  $R_{CL2}$ . When the voltage across the resistor equals  $V_{CL2}$  the regulator enters current limit and will fold back according to the waveform shown in figure 3. To calculate the current limit use the formula below:

$$V_{CL2} / I_{LIM} = R_{CL} \quad (1)$$

where  $I_{LIM}$  is the target current limit.

**Serial Port****Serial Port Writing**

The serial port is accessed for writing only, using the STB (Strobe), CLK (clock), DATA and SLEEPN pins. Addressing consists of word selection bits (D15:D14) followed by the bit values for each parameter in the word. Timing requirements are shown in figure 4.

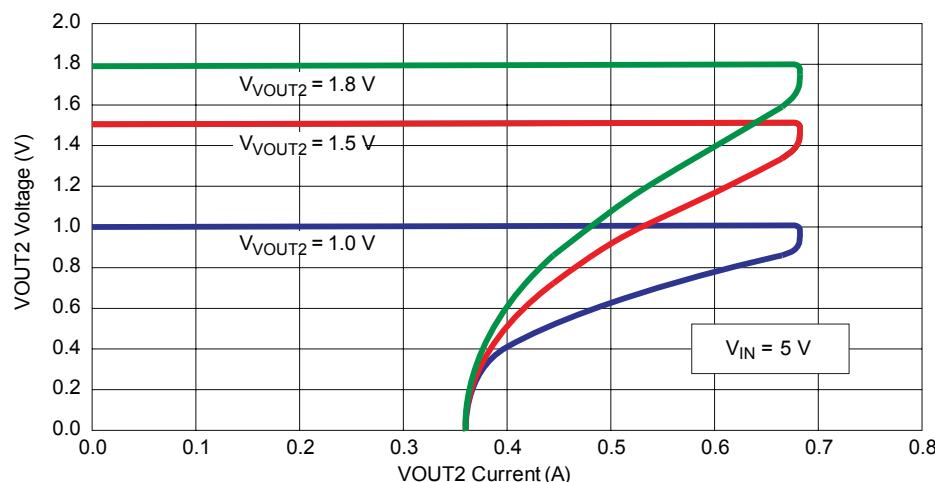


Figure 3. Linear current limit with foldback

**Configuration Register**

A configuration register supporting four 16-bit words can be set using the serial port.

The Configuration register is volatile memory accessed through the serial port. The bit descriptions are shown in table 1. At a power-on reset (POR), the bits are set to their default values, all zeros with the exception of the MSB of the fixed off-time parameters, which are set to one.

**Motor Driver****Full Bridge Output Current Regulation**

Maximum load current is regulated by an Internal PWM mode, fixed off-time current control circuit. When the outputs of the DMOS full bridges are turned on, current increases in the motor winding until it reaches a value given by:

$$I_{\text{TRIP}} = V_{\text{REF}} \times \text{Current Ratio} / (5 \times R_S) \quad (2)$$

where  $R_S$  is the value of the sense resistor  $R_S$ , and the Current Ratio is as shown in table 2.

At the trip point, the sense comparator resets the source enable latch, turning off the source driver. At this point, load inductance causes the current to recirculate for the serial port programmed fixed off-time period. The current path during recirculation is determined by the configuration of slow/mixed decay mode and the synchronous rectification control bits.

**Fixed Off-Time**

The PWM timer is programmable via the serial port to provide fixed off-time PWM signals to the A3998 internal control block.

Five bits (word 0/1, D6:D2) are available for each full bridge to adjust the fixed off-time,  $t_{\text{OFF}}$ , when Internal PWM current control mode is selected.

The off-time is defined by the following equation:

$$t_{\text{OFF}} = (1 + N) \times T_{\text{OSC}} \times 8 - T_{\text{OSC}} \quad (3)$$

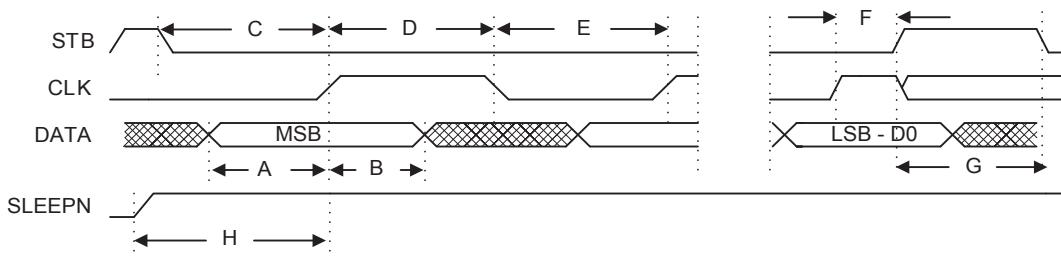
where  $N$  is the word value, from 0 to 31, and  $T_{\text{OSC}}$  is the period of the internal oscillator.

For example, given the internal oscillator frequency,  $f_{\text{OSC}}$ , of 4 MHz (typ) ( $T_{\text{OSC}} = 250$  ns), the fixed off-time is adjustable from 2 to 64  $\mu$ s in increments of 2  $\mu$ s.

**PWM Control Mode**

The selection of Internal or External PWM control mode for each full bridge is made in the Configuration register.

- Selection of Internal control mode (word 2, D0 and D7) sets the Internal PWM Decay Mode (Mixed or Slow), and allows the configuration of Fixed Off-Time and Fast Decay Time. In Mixed Decay mode, during the first portion of the off-time period, the A3998 operates in Fast Decay mode, until the Fast Decay time count is reached. The rest of the fixed off-time period the A3998 operates in Slow Decay mode. If the Fast Decay Time duration is longer than the Fixed Off-Time duration, the device effectively operates in Fast Decay mode throughout the period.
- Selection of External control mode (word 2, D1 and D8) sets the External PWM Decay Mode (Fast or Slow). In this mode, a chopping signal on the Enable pins (ENBx) are used to provide external PWM current control.



A. Minimum Data Setup Time	15 ns	E. Minimum Clock Low Pulse Width	50 ns
B. Minimum Data Hold Time	10 ns	F. Minimum Setup Clock Rising Edge to Strobe	50 ns
C. Minimum Setup Strobe to Clock Rising Edge	50 ns	G. Minimum Strobe Pulse Width	50 ns
D. Minimum Clock High Pulse Width	50 ns	H. Minimum Sleep to Clock Setup Time	100 ns

Figure 4. Serial Port Timing Diagram

**Phase Control**

This setting sets the relative states of the full-bridge outputs. This determines if the device operates in the forward or reverse (relative) direction:

Serial Port Configuration Bit (Word 2)	Phase			
	D2/D9	State	OUTA	OUTB
0	Reverse	Low	High	
1	Forward	High	Low	

**Enable Logic**

The ENB1 and ENB2 input terminals are provided for external PWM control of the two full bridges. When ENBx is set to logic high, output on the corresponding full bridge is enabled. When set to logic low, the bridge output is chopped.

**Fast Decay Time**

Four bits (word 0/1, D10:D7) are available for each full bridge to set the Fast Decay portion,  $t_{FD}$ , of the fixed off-time when Internal PWM control, Mixed Decay mode is selected.

The Fast Decay portion is defined by:

$$t_{FD} = (1 + N) \times T_{OSC} \times 8 - T_{OSC} \quad (4)$$

where N is the word value, from 0 to 15.

For example, given the internal oscillator frequency,  $f_{OSC}$ , of 4 MHz (typ) ( $T_{OSC} = 250$  ns), the fixed off-time is adjustable from 2 to 32  $\mu$ s in increments of 2  $\mu$ s. For  $t_{FD} > t_{OFF}$ , the device effectively operates in Fast Decay mode.

**PWM Blank Timer**

When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike from erroneously resetting the source enable latch, the sense comparator is blanked.

The programmable blanking function is enabled while the blank timer runs, which is after the off-time counter expires. When the Enable (ENBx) signal is chopped, or the Phase setting in the Configuration register is changed, a PWM-off cycle is initiated and the blank timer is reset.

**Blank Time** Two bits (word 0/1, D1:D0) are available for each full bridge to set the current sense comparator blank time when any output driver is switched on. The settings are according to the following table ( $T_{OSC}$  is the period of the internal oscillator):

Serial Port Configuration Bit (Word 0/1)	Blank Time		
	D1	D0	
0	0	0	$4 \times T_{OSC}$
0	0	1	$6 \times T_{OSC}$
1	0	0	$12 \times T_{OSC}$
1	1	1	$24 \times T_{OSC}$

For example, given the internal oscillator frequency,  $f_{OSC}$ , of 4 MHz (typ) ( $T_{OSC} = 250$  ns), the blank time is adjustable from 1 to 6  $\mu$ s.

**Synchronous Rectification**

When a PWM-off cycle is triggered, either by an Enable chop command or an Internal PWM control mode Fixed Off-Time cycle, the load current recirculates according to the decay mode selected by the Configuration register settings. After a short crossover delay, the synchronous rectification feature turns-on the appropriate MOSFET (or pair of MOSFETs, for the Mixed Decay portion of the off-time) during the current decay and effectively shorts-out the body diodes with the low  $R_{DS(on)}$  driver. This lowers power dissipation significantly and can eliminate the requirement for external Schottky diodes.

Synchronous rectification can be configured in active mode or passive mode via the serial port (word 0/1, D11):

- Active mode prevents reversal of load current by turning-off synchronous rectification when a zero current level is detected.
- Passive mode allows reversal of current, but turns-off synchronous rectification if the load current inversion ramps up to the  $I_{TRIP}$  current limit (see equation 1).

**SLEEPN Pin** Active low input signal to reset serial port Configuration register and enter Standby mode. During Standby mode, the regulators can still operate.

### Protection

**Switching Regulator** The buck switch is disabled under the following fault conditions:

- $V_{BB} < V_{BBUV(th)}$
- $V_{CP} < V_{BB} + 5\text{ V}$
- Thermal shutdown fault

**Thermal Protection** A thermal shutdown circuit turns-off all drivers and disables the switching regulator in the event of a fault due to excessive junction temperature. The serial port Configuration register is not reset.

Shutdown occurs when the junction temperature reaches  $T_{JSD}$ ,  $165^\circ\text{C}$  (typ). Thermal shutdown has a hysteresis,  $T_{JSDHYS}$ , of approximately  $20^\circ\text{C}$  (typ). The outputs of the device remain disabled until the fault condition is removed.

**PMON Pin** Open drain output, logic high indicates  $V_{BB}$  is above the UVLO threshold.

**Undervoltage Lockout** At power-up, and in the event of low  $V_{IN}$ , the UVLO circuit disables the drivers and the serial port Configuration register is reset to the default, POR state.

**OCP** When an overcurrent event is detected, the serial port Configuration register is reset to the default (POR) state. This

fault is latched and can only be reset by cycling the power to the A3998 ( power-on reset, POR) or by cycling Standby mode (via the SLEEPN pin).

Note: An overcurrent fault event will not be generated during a shorted load condition if the blank time is programmed shorter than the  $t_{OCP}$ . In this case, the overcurrent protection is still active, however, the internal current control circuit will operate as normal and terminate the source driver on-state upon completion of the blank time, before the OCP can trip the fault line and reset the serial port.

### Power-On Reset

**FRST Pin** Active high input signal forces reset (POR).

**RSTN Pin** An open drain output, RSTN will be low if either of following conditions are true:

- $V_{FBI} < V_{FBUV(th)}$
- FRST high

If neither of the conditions are true, there will be a 100 ms delay before RSTN goes high. (See RST Function with FRST Input timing diagram.)

**Table 1. Configuration Register Bit Map**

Bit #	Function	Reset (POR) Value
<b>Word 0</b>		
D0	Bridge 1 Blank Time LSB	0
D1	Bridge 1 Blank Time MSB	0
D2	Bridge 1 Off Time LSB	0
D3	Bridge 1 Off Time Bit 1	0
D4	Bridge 1 Off Time Bit 2	0
D5	Bridge 1 Off Time Bit 3	0
D6	Bridge 1 Off Time MSB	1
D7	Bridge 1 Fast Decay LSB	0
D8	Bridge 1 Fast Decay Bit 1	0
D9	Bridge 1 Fast Decay Bit 2	0
D10	Bridge 1 Fast Decay MSB	0
D11	Bridge 1 Synchronous Rectification Control: 0 = Active 1 = Passive	0
D12	Unused	0
D13	Unused	—
D14	Word Select 0 = 0	—
D15	Word Select 1 = 0	—
<b>Word 1</b>		
D0	Bridge 2 Blank Time LSB	0
D1	Bridge 2 Blank Time MSB	0
D2	Bridge 2 Off Time LSB	0
D3	Bridge 2 Off Time Bit 1	0
D4	Bridge 2 Off Time Bit 2	0
D5	Bridge 2 Off Time Bit 3	0
D6	Bridge 2 Off Time MSB	1
D7	Bridge 2 Fast Decay LSB	0
D8	Bridge 2 Fast Decay Bit 1	0
D9	Bridge 2 Fast Decay Bit2	0
D10	Bridge 2 Fast Decay MSB	0
D11	Bridge 2 Synchronous Rectification Control: 0 = Active 1 = Passive	0
D12	Unused	0
D13	Unused	—
D14	Word Select 0 = 1	—
D15	Word Select 1 = 0	—

*Continued on the next page...*

**Table 1. Configuration Register Bit Map (continued)**

Bit #	Function	Reset (POR) Value
<b>Word 2</b>		
D0	Bridge 2 Internal PWM Mode: 0 = Mixed decay mode 1 = Slow decay mode	0
D1	Bridge 2 External PWM Mode (ENB2 chopping): 0 = Fast decay mode 1 = Slow decay mode	0
D2	Bridge 2 Phase	0
D3	Bridge 2 DAC LSB (Current Ratio bit)	0
D4	Bridge 2 DAC Bit 2 (Current Ratio bit)	0
D5	Bridge 2 DAC Bit 3 (Current Ratio bit)	0
D6	Bridge 2 DAC Bit 4 (Current Ratio bit)	0
D7	Bridge 1 Internal PWM Mode: 0 = Mixed decay mode 1 = Slow decay mode	0
D8	Bridge 1 External PWM Mode (ENB1 chopping): 0 = Fast decay mode 1 = Slow decay mode	0
D9	Bridge 1 Phase	0
D10	Bridge 1 DAC LSB (Current Ratio bit)	0
D11	Bridge 1 DAC Bit 2 (Current Ratio bit)	0
D12	Bridge 1 DAC Bit 3 (Current Ratio bit)	0
D13	Bridge 1 DAC Bit 4 (Current Ratio bit)	0
D14	Word Select 0 = 0	—
D15	Word Select 1 = 1	—

*Continued on the next page...*

Table 1. Configuration Register Bit Map (continued)

Bit #	Function	Reset (POR) Value
<b>Word 3</b>		
D0	Thermal Monitor: 0 = Normal function 1 = RSTN = thermal analog output, $V = K \times T_J$	0
D1	Charge Pump: 0 = Normal Operation 1 = Disable Charge Pump	0
D2	Reserved For Test	0
D3	Reserved For Test	0
D4	Reserved For Test	0
D5	Reserved For Test	0
D6	Reserved For Test	0
D7	Reserved For Test	0
D8	Reserved For Test	0
D9	Reserved For Test	0
D10	Reserved For Test	0
D11	Reserved For Test	0
D12	Reserved For Test	0
D13	Reserved For Test	0
D14	Word Select 0 = 1	—
D15	Word Select 1 = 1	—

**Table 2. Current Ratio Configuration\***

DAC Bit 4	DAC Bit 3	DAC Bit 2	DAC LSB	Current Ratio (%)
1	1	1	1	100.0
1	1	1	0	95.65
1	1	0	1	91.30
1	1	0	0	86.95
1	0	1	1	82.61
1	0	1	0	78.26
1	0	0	1	73.91
1	0	0	0	69.56
0	1	1	1	60.87
0	1	1	0	52.17
0	1	0	1	43.48
0	1	0	0	34.78
0	0	1	1	26.08
0	0	1	0	17.39
0	0	0	1	0
0	0	0	0	Disabled

\*Internal PWM control mode selected

## Application Information

## PCB Layout

## Switcher

The board layout has a significant impact on the performance of the device. It is important to isolate high current ground returns, in order to minimize ground bounce that could produce reference errors in the device. The method used to isolate power ground from noise sensitive circuitry is a star ground. This approach makes sure the high current components such as the input capacitor, output capacitor, and diode have very low impedance paths to each other. Figure 5 illustrates the technique. The ground from each of the components should be very close to each other and be connected on the same surface as the components. Internal ground planes should not be used for the star ground connection, because vias add impedance to the current path. In order to further reduce noise effects on the PCB, noise sensitive traces should not be connected to internal ground planes.

The feedback network from the switcher output should have an independent ground trace that goes directly to the exposed pad underneath the device. The exposed pad should be connected to internal ground planes and to any exposed copper used for heat dissipation. If the grounds from the device also are connected directly to the exposed pad, the ground reference from the feedback network will be less susceptible to noise injection or ground bounce.

To reduce radiated emissions from the high frequency switching nodes it is important to have an internal ground plane directly under the LX node. The plane should not be broken directly under the switching path because the lowest impedance path for radiated emissions is back to the star ground using the ground plane directly under the signal trace. If another trace does break the return path, the energy will have to find another path, which is through radiated emissions or through stray eddy currents.

## Motor Driver

In order to use PWM current control, a low-value resistor is placed between the LSSx pin and ground for current sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account. When selecting a value for the sense resistor be sure not to exceed the maximum voltage on the SENSEx pin of  $\pm 500$  mV at maximum load. During overcurrent events, this rating may be exceeded for short durations.

## Thermal Considerations

The PCB should have a thick ground plane. For optimum electrical and thermal performance, the A3998 must be soldered directly onto the board. On the underside of the A3998 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad must be soldered directly to an exposed surface on the PCB in order to achieve optimal thermal conduction. Thermal vias are used to transfer heat to other layers of the PCB. The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically  $100\ \mu\text{F}$ ) in parallel with a lower valued ceramic capacitor placed as close as practicable to the device.

## Switching Regulator Component Selection

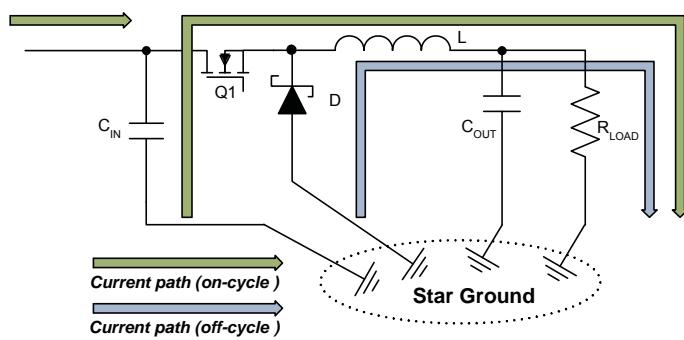
External component recommended values are provided in table 3.

$V_{\text{OUT1}}$  The regulator requires an external clamping diode, D1, inductor, L1, and filter capacitor, COUT1 (see figure 1).

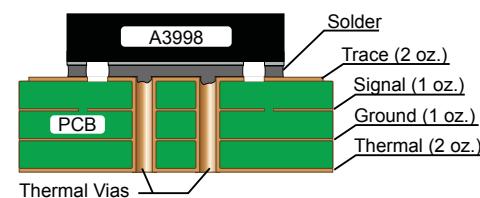
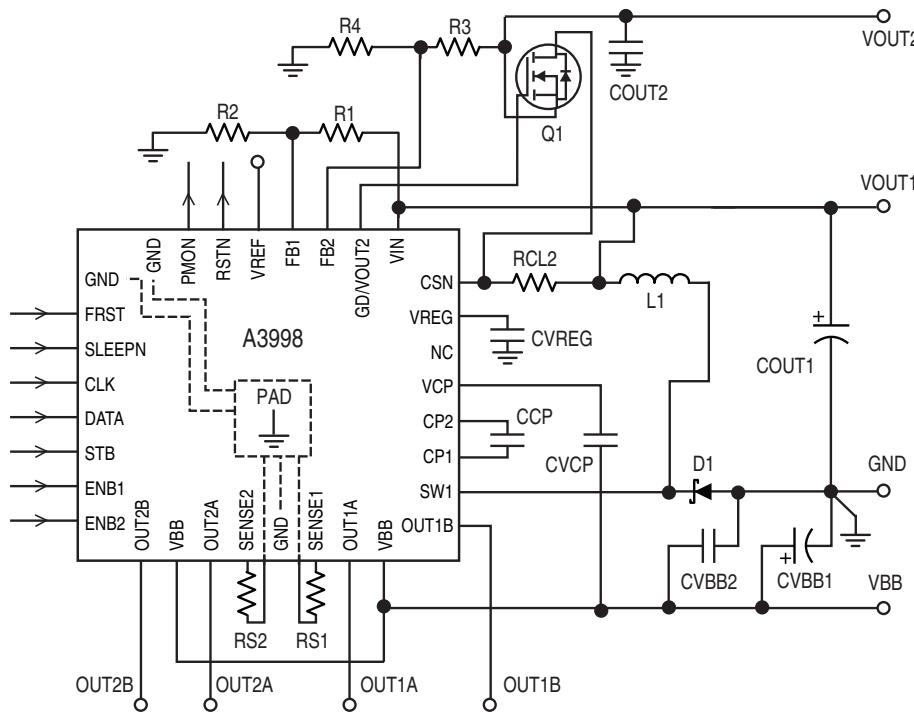
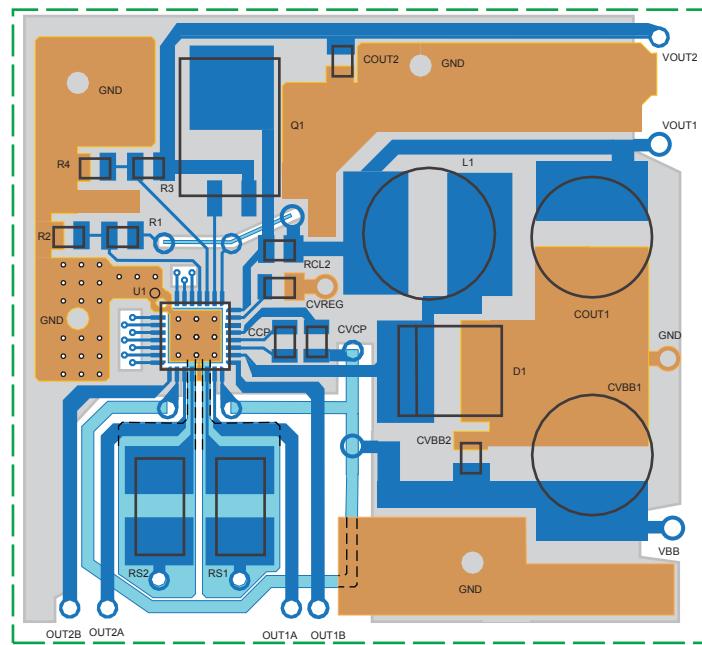
The output voltage is determined by an external resistive voltage divider, according to the following formula:

$$V_{\text{OUT1}} = V_{\text{FB1}} \times (1 + R1 / R2) \quad (5)$$

Figure 5. Star Ground Connection



## PCB Layout Diagram



The total resistance from  $V_{OUT1}$  to FB1 to GND should be less than  $10\text{ k}\Omega$ .

**D1** The Schottky catch diode should be rated to handle 1.2 times the maximum load current. The voltage rating should be higher than the maximum input voltage expected during any operating condition. The duty cycle for high input voltages can be very close to 100%.

**L1** The inductor must be rated to handle the total load current and the value chosen must keep the ripple current to a reasonable value. The ripple current,  $I_R$ , can be calculated by:

$$I_R = V_{L(OFF)} \times (t_{OFF} / L) \quad (6)$$

where

$$V_{L(OFF)} = V_{OUT1} + V_f + I_{av} \times R_L \quad (7)$$

The switching frequency can then be estimated by:

$$f_{PWM} = 1 / (t_{ON} + t_{OFF}) \quad (8)$$

where

$$t_{ON} = I_R \times L / V_{L(ON)} \quad (9)$$

and

$$V_{L(ON)} = V_{BB} - I_{av} \times R_{DS(on)} - I_{av} \times R_L - V_{OUT1} \quad (10)$$

Higher inductor values can be chosen to lower the ripple current. This may be an option if it is required to increase the total maximum current available that can be drawn from the switching regulator. The maximum total current available is:

$$I_{LOAD(max)} = I_{CL(min)} - I_R / 2 \quad (11)$$

Where  $I_{CL(min)}$  is from the Electrical Characteristics table.

**COUT1** The output capacitor main consideration is voltage ripple on the output. For electrolytic output capacitors, a low ESR type is recommended. The peak to peak output ripple is simply:

$$I_{R(pp)} = I_R \times ESR \quad (12)$$

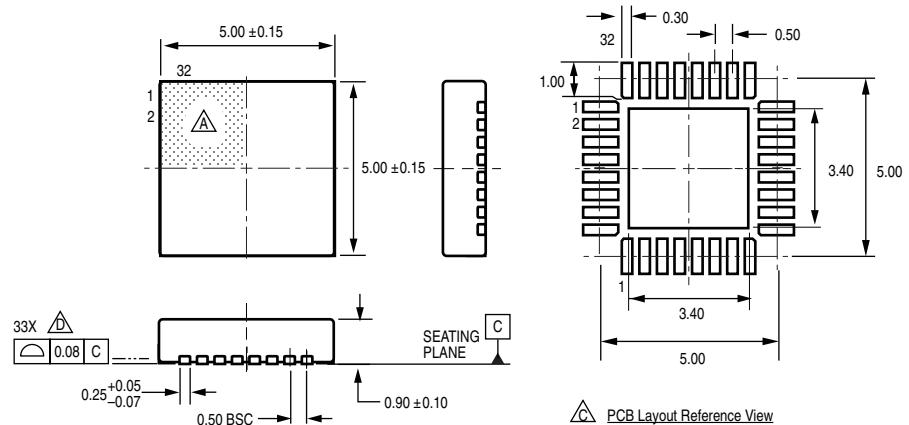
Note that the ripple current can be decreased by increasing the inductor value. The minimum voltage rating of the capacitor is 10 V, however, because ESR decreases with voltage, the most cost effective choice may be a higher rated voltage.

**Vout2** This output requires a 10  $\mu\text{F}$  ceramic output capacitor, COUT2.

**Table 3. Recommended Components**

Configuration		Component			
Output	$f_{PWM}$	Symbol	Description	Representative Component	
$V_{OUT1x}$					
5 V / 1 A	220 kHz	L1	68 $\mu\text{H}$	3BSumida RCH1216BNP-680K	
		COUT1	220 $\mu\text{F}$ / 25 V, ESR = 72 m $\Omega$	Rubycon ZL 25ZL220M8x11.5	
		D1	60 V / 3 A Schottky diode	NSQ03A06	
		R1	2 k $\Omega$		
		R2	499 $\Omega$		
3.3V/1A	230 kHz	L1	68 $\mu\text{H}$	4BSumida RCH1216BNP-680K	
		COUT1	220 $\mu\text{F}$ / 25 V, ESR = 72 m $\Omega$	Rubycon ZL 25ZL220M8x11.5	
		D1	60 V / 3 A Schottky diode	Vishay SS36	
		R1	2 k $\Omega$		
		R2	866 $\Omega$		
$V_{OUT2x}$					
		Q1	External MOSFET - $C_{gs} < 1000\text{ pF}$		
		RSx	Sense resistor		
		COUT2	10 $\mu\text{F}$ / 10 V X5R		
		R3, R4			

## Package ET, 32-Pin QFN



Concept Drawing For Reference Only; not for tooling use  
(reference JEDEC MO-220VHHD-6)

Dimensions in millimeters

Exact case and lead configuration at supplier discretion within limits shown

▲ Terminal #1 mark area

▲ Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

▲ Reference land pattern layout (reference  
IPC7351 QFN50P500X500X100-33V6M);  
All pads a minimum of 0.20 mm from all adjacent pads; adjust as  
necessary to meet application process requirements and PCB layout  
tolerances; when mounting on a multilayer PCB, thermal vias at the  
exposed thermal pad land can improve thermal dissipation (reference  
EIA/JEDEC Standard JESD51-5)

▲ Coplanarity includes exposed thermal pad and terminals

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