

### Typical Applications

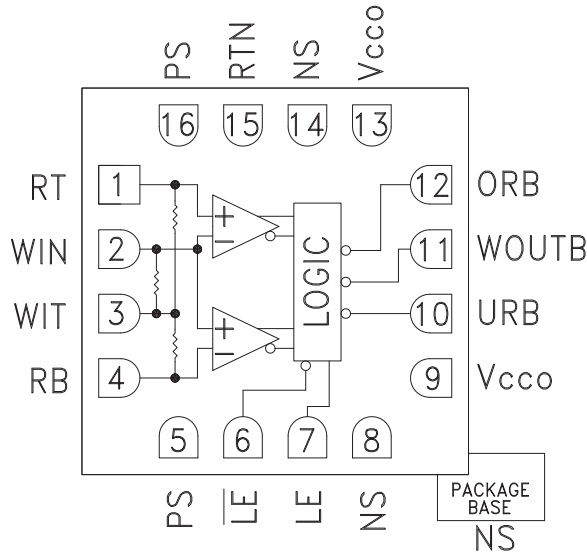
The HMC974LC3C is ideal for:

- ATE Applications
- High Speed Instrumentation
- Clock and Data Restoration
- Semiconductor Test Systems
- EW Systems - Threshold Detection

### Features

- Propagation delay: 88 ps
- Overdrive & Slew Rate Dispersion: 20 ps
- Minimum Detectable Pulse Width: 60 ps
- Differential Latch Control
- Power Dissipation: 240 mW
- 16 Lead 3x3mm SMT Package: 9mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC974LC3C is a SiGe monolithic, ultra fast window comparator with level latched output driver with reduced swings. The window comparator is based on the HMC674LC3C single comparator and incorporates two such comparators and additional output logic. Three output ports detect whether an analog input signal is above, below or between two reference levels supplied at its input as shown on the timing diagram herein.

The outputs are single-ended negative logic. Incorporating two proven comparators at the input provides good DC and dynamic matching and reduces the input capacitance. The reduced swing output stages are designed to directly drive 400 mV into 50 Ohms terminated to a voltage  $V_{TERM} = V_{CCO} - 2V$ .

HMC974LC3C features high speed latches that can either be enabled to latch the output data, or can be left in the transparent mode to implement a tracking window comparator.

### Electrical Specifications, $T_A = +25^\circ C$

$NS = -3V, PS = +3.3V, V_{CCO} = +2V, V_{TERM} = 0V, V_{CM} = 0V, V_{OD} = 50mV$  [1]

| Parameter                       | Conditions           | Min. | Typ. | Max | Units |
|---------------------------------|----------------------|------|------|-----|-------|
| <b>DC INPUT CHARACTERISTICS</b> |                      |      |      |     |       |
| Offset voltage                  |                      | -10  | ±4   | 10  | mV    |
| Bias current                    | WIT Termination Open | -30  | 20   | 30  | uA    |
| Differential voltage (max)      |                      | -2   |      | 2   | V     |
| Input impedance WIN to WIT      |                      |      | 50   |     | Ohms  |
| Input impedance RT to WIT       |                      |      | 50   |     | Ohms  |
| Input impedance RB to WIT       |                      |      | 50   |     | Ohms  |
| Common Mode Input Voltage Range |                      | -1.5 |      | 1.5 | V     |
| Input Capacitance               |                      |      | 1    |     | pF    |


**Electrical Specifications, (continued)**

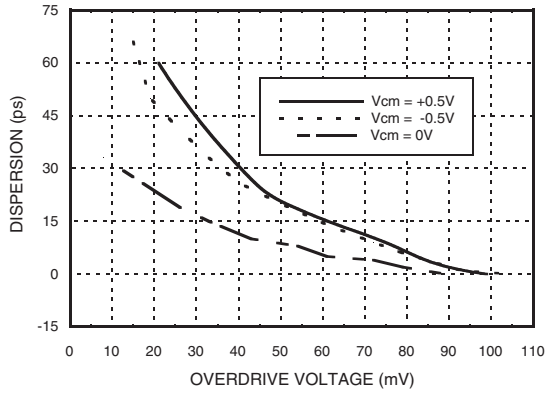
| Parameter  | Conditions                                  | Min. | Typ. | Max  | Units                  |
|--|---|------|------|------|------------------------|
| <b>LATCH ENABLE CHARACTERISTICS</b>  |   |      |      |      |                        |
| LE / $\overline{\text{LE}}$ "L"  |   |      | 1.6  |      | V                      |
| LE / $\overline{\text{LE}}$ "H"  |   |      | 2.4  |      | V                      |
| LE / $\overline{\text{LE}}$ Impedance<br>(if not driven the device is unlatched) |   |      | 7.8  |      | kOhms                  |
| <b>DC OUTPUT CHARACTERISTICS</b>   |   |      |      |      |                        |
| Output Voltage High Level, VOH (50 Ohms to 0V)                                   |   |      | 1.06 |      | V                      |
| Output Voltage Low Level, VOL (50 Ohms to 0V)                                    |   |      | 0.73 |      | V                      |
| Output Voltage Swing   |   | 320  | 365  | 410  | mV                     |
| <b>AC PERFORMANCE</b>  |   |      |      |      |                        |
| Propagation Delay Dispersion vs. VOD   | For VOD > 50mV                              |      | 20   |      | ps                     |
| Rise Time (each output), tr  | 20% to 80%                                  |      | 25.3 |      | ps                     |
| Fall Time (each output), tf  | 80% to 20%                                  |      | 21.9 |      | ps                     |
| Minimum Detectable Pulse Width   | VCM = 0V;<br>$\pm 100$ mV Overdrive Voltage |      | 60   |      | ps                     |
| Equivalent Input Bandwidth [2]   |   |      | 11   |      | GHz                    |
| Input-to-Output Delay  |   |      | 88   |      | ps                     |
| Latch-to-Output Delay  |   |      | 83   |      | ps                     |
| Max. Input Slew Rate   |   |      | 5    |      | V/ns                   |
| Noise (RTI)  |   |      | 6    |      | nV/ $\sqrt{\text{Hz}}$ |
| Random Jitter (rms)  | at 5 Gbps with $\pm 100$ mV<br>overdrive    |      | 0.2  |      | ps rms                 |
| Deterministic Jitter (pp)  | at 5 Gbps with $\pm 100$ mV<br>overdrive    |      | 2    |      | ps                     |
| <b>POWER SUPPLIES (including load)</b>   |   |      |      |      |                        |
| IPS  |   | 13.4 | 14.9 | 16.5 | mA                     |
| INS  |   | 28.3 | 29.9 | 31.6 | mA                     |
| Icco   |   | 70   | 72.3 | 79.6 | mA                     |
| Pd   |   |      | 240  |      | mW                     |

[1] Vcco can be set between +3.3V and 0V; Vterm = Vcco-2V  
RSPECL levels are obtained with Vcco=+3.3V and Vterm=+1.3V;  
RSECL levels are obtained with Vcco=0V and Vterm= -2 V

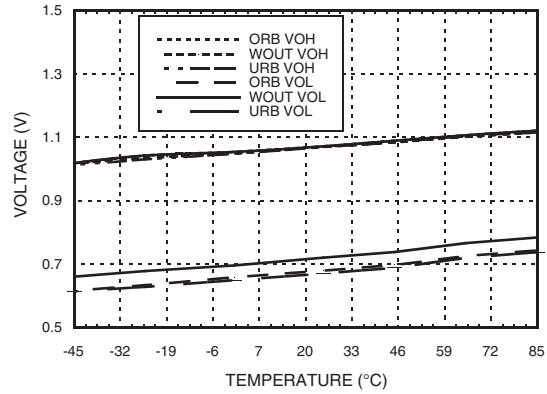
[2] Equivalent Input Bandwidth is calculated with the following formula:  $B_{\text{weq}} = 0.22/f$  (TRCOMP2-TRIN2) where TRIN is the 20%/80% transition time of a quasi-Gaussian signal applied to the comparator input, and TRCOMP is the effective transition time digitized by the comparator.



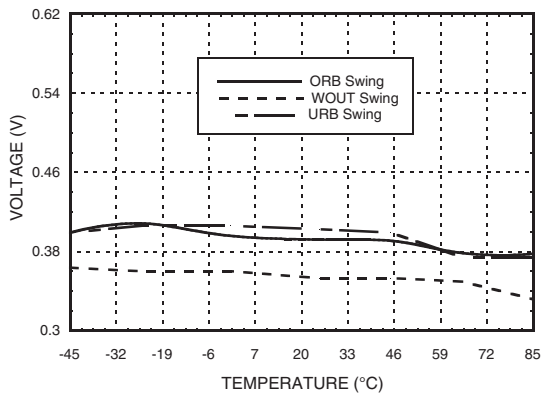
**Dispersion vs. Overdrive Voltage**



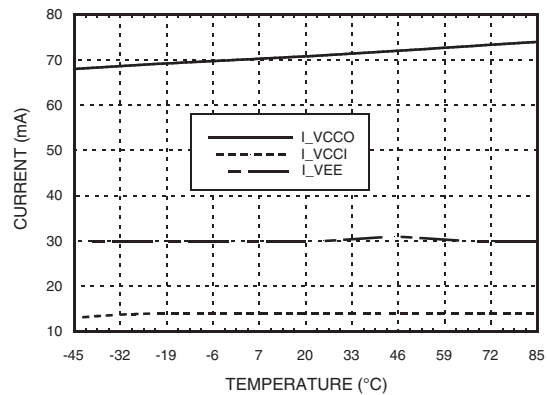
**Output Voltage vs. Temperature**



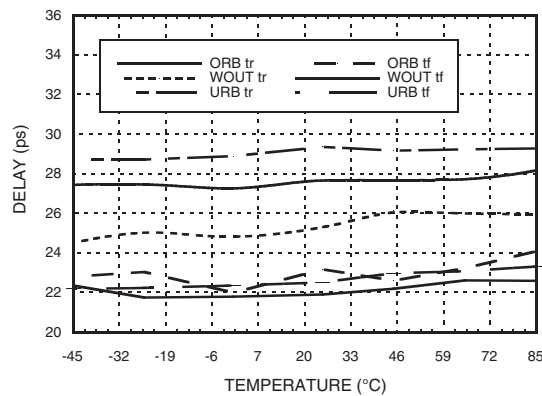
**Output Voltage Swing vs. Temperature**



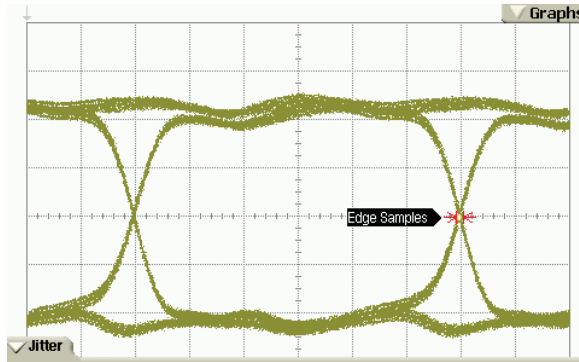
**Power Supply Currents**



**Output Rise / Fall Time**

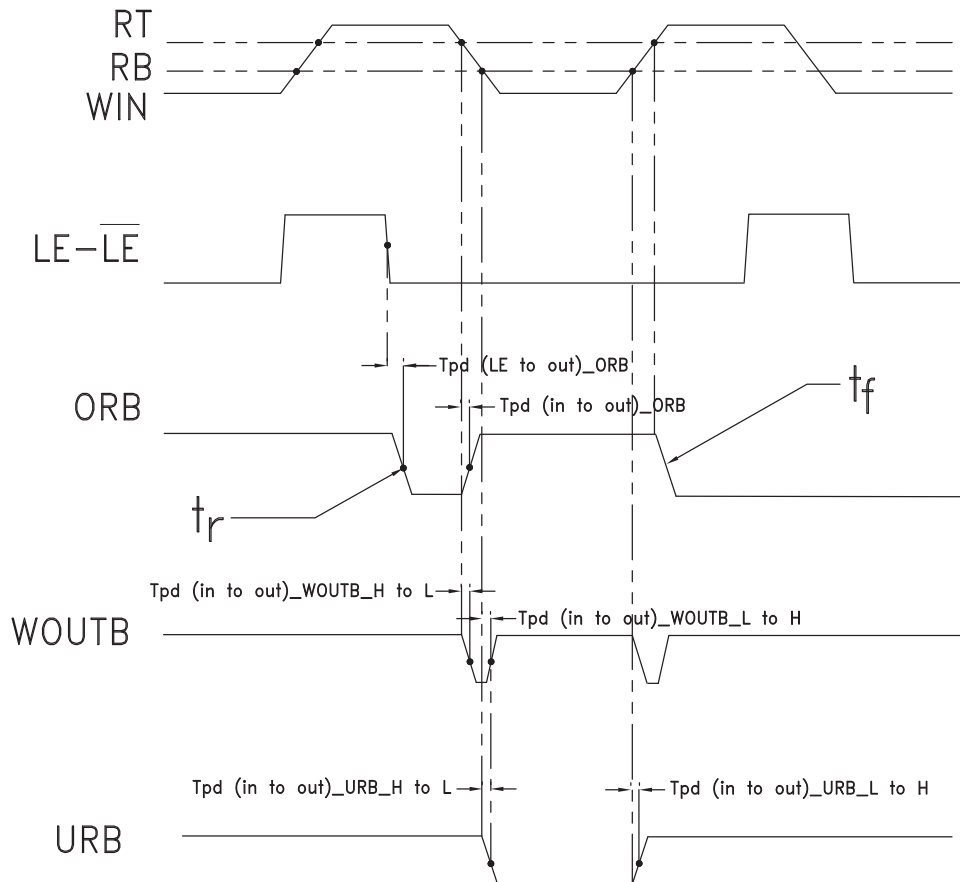


**Eye Diagram @ 5 Gbps**



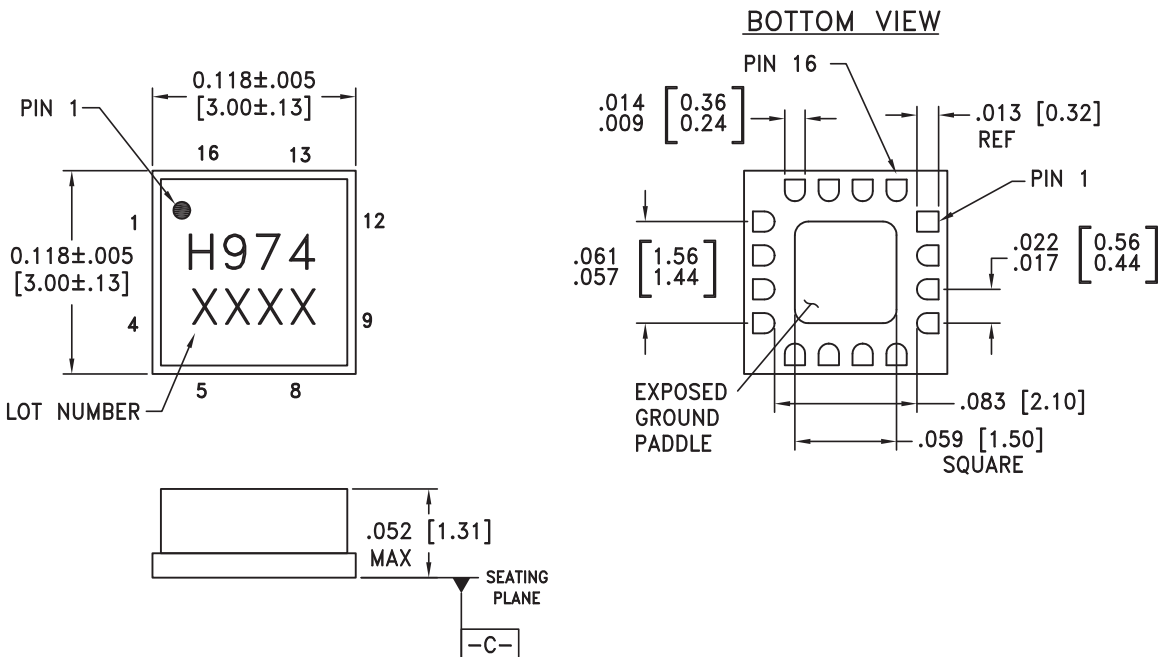
| Parameter      | Conditions          |
|----------------|---------------------|
| Bit Rate       | 5 Gbps              |
| Pattern Length | 2 <sup>15</sup> - 1 |
| DJ (p-p)       | 2.15 ps             |
| Vertical Scale | 80 mV / div         |
| Time Scale     | 33.3 ps / div       |

**Timing Diagram**



**Absolute Maximum Ratings**

|   |                 |
|---|-----------------|
| Input Supply Voltage (V <sub>cci</sub> to GND)                            | -0.5V to +4V    |
| Output Supply Voltage (V <sub>cco</sub> to GND)                           | -0.5V to +4V    |
| Positive Supply Differential (V <sub>cci</sub> - V <sub>cco</sub> )       | -0.5V to +3V    |
| Input Voltage   | -2V to +2V      |
| Differential Input Voltage  | -2V to +2V      |
| Output Current  | 40 mA           |
| Junction Temperature  | 125°C           |
| Continuous P <sub>diss</sub> (T = 85°C)<br>(Derate 20.4 mW/°C above 85°C) | 0.816 W         |
| Thermal Resistance (R <sub>th</sub> ) (Junction to Lead)                  | 49 °C/W         |
| Storage Temperature   | -65°C to +150°C |
| Operating Temperature   | -40°C to +85°C  |

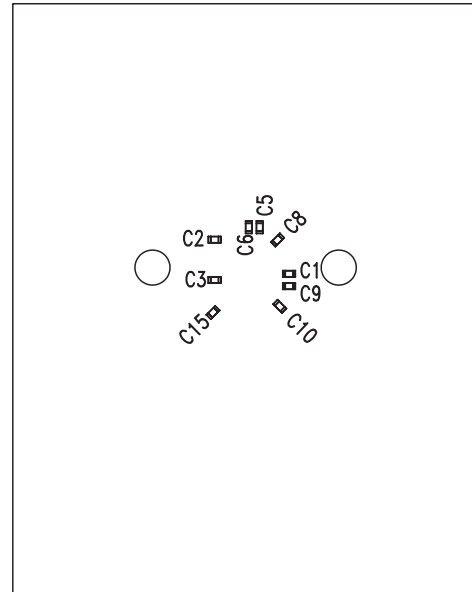
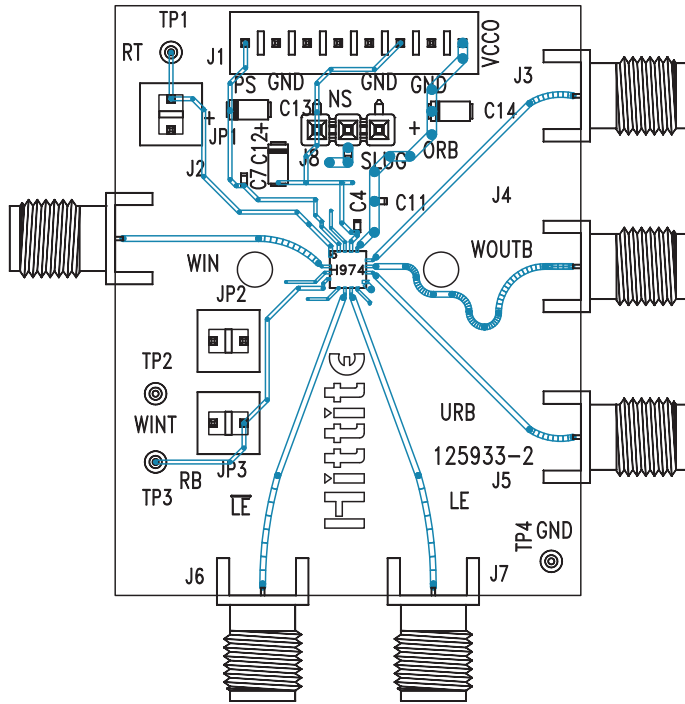

**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**
**7**
**COMPARATORS - SMT**
**Outline Drawing**

**NOTES:**

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:  
30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO NS.

### Pin Descriptions

| Pin Number | Function        | Description  | Interface Schematic |
|------------|-----------------|--|---------------------|
| 1          | RT              | Termination resistor for reference top.  |                     |
| 2          | WIN             | Window analog input.   |                     |
| 3          | WIT             | Window CM for termination resistors.   |                     |
| 4          | RB              | Termination resistor return for reference bottom.  |                     |
| 5, 16      | PS              | Positive supply voltage input stage.   |                     |
| 6          | $\overline{LE}$ | Latch enable input pin, inverting side.  |                     |
| 7          | LE              | Latch enable input pin, non-inverting side.  |                     |
| 8, 14      | NS              | Negative power supply, -3V.  |                     |
| 9, 13      | Vcco            | Positive supply voltage for the output stage.  |                     |
| 10         | URB             | Under-range output. URB is asserted low when the analog input voltage is below RB.       |                     |
| 11         | WOUTB           | Window Output. WOUTB is asserted low when the analog input voltage is between RB and RT. |                     |
| 12         | ORB             | Over-range output. ORB is asserted low when the analog input voltage range is above RT.  |                     |
| 15         | RTN             | Return for ESD protection.   |                     |
|            | Package Base    | Exposed paddle should be connected to NS (negative power supply, -3V)                    |                     |

### Evaluation PCB



### List of Materials for Evaluation PCB 129538 [1]

| Item                           | Description                      |
|--------------------------------|----------------------------------|
| J1                             | Conn Header 8 Pos Vert Tin       |
| J2 - J7                        | K Connector, SRI                 |
| J8                             | Terminal Strip, Single Row 3 Pin |
| JP1, JP2                       | Conn Header 2 Pos Vert Tin       |
| C1 - C3, C5, C6, C8 - C10, C15 | 100 pF Capacitor, 0402 Pkg.      |
| C4, C7, C11                    | 330 pF Capacitor, 0402 Pkg.      |
| C12 - C14                      | 4.7 μF Capacitor, Tantalum       |
| TP1 - TP4                      | DC Pin                           |
| U1                             | HMC974LC3C Window Comparator     |
| PCB [2]                        | 125933 Evaluation Board          |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to NS. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



**Application Circuit**

