HMC838LP6CE

v05.0612

FRACTIONAL-N PLL WITH INTEGRATED VCO
795 - 945, 1590 - 1890, 3180 - 3780 MHz

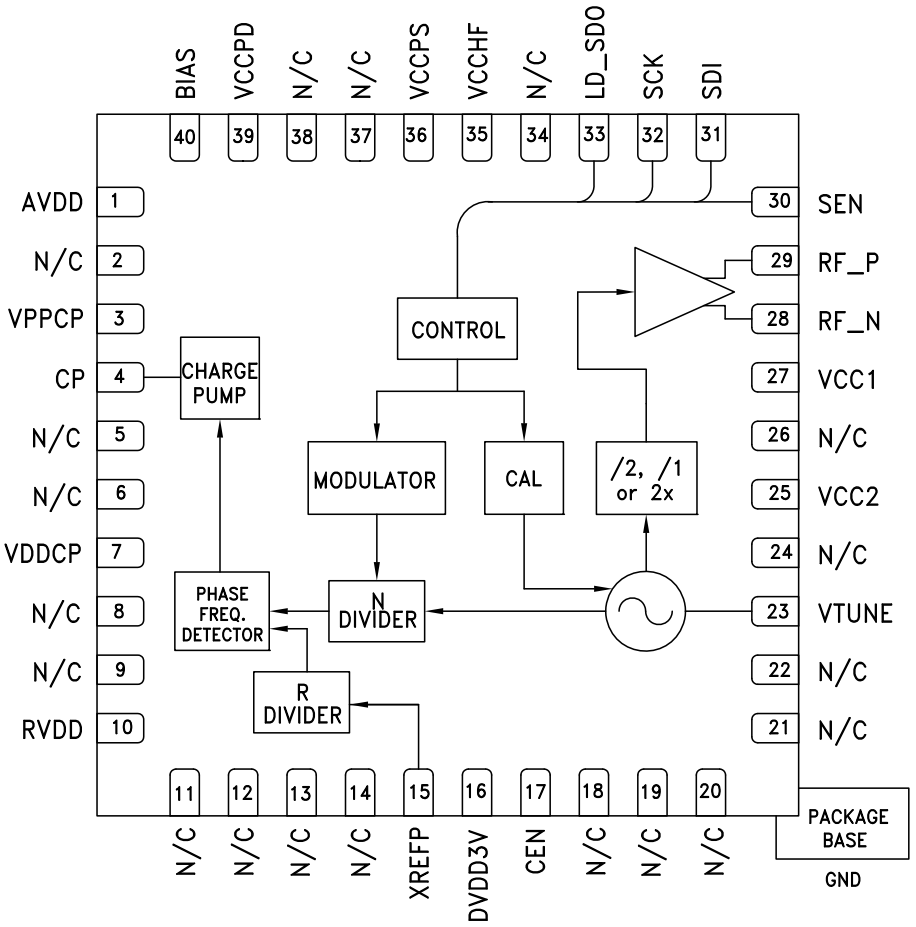
Features

- Tri-band RF Bandwidth: 795 - 945, 1590 - 1890, 3180 - 3780 MHz
- Ultra Low Phase Noise -111 dBc/Hz in Band Typ.
- Figure of Merit (FOM) -227 dBc/Hz
- < 180 fs RMS Jitter
- 24-bit Step Size, Resolution 3 Hz typ
- Exact Frequency Mode
- Built-in Digital Self Test
- 40 Lead 6x6 mm SMT Package: 36 mm^2

Typical Applications

- Cellular/4G Infrastructure
- Repeaters and Femtocells
- Communications Test Equipment
- CATV Equipment
- Phased Array Applications
- DDS Replacement
- Very High Data Rate Radios

Functional Diagram



FRACTIONAL-N PLL WITH INTEGRATED VCO
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General Description

The HMC838LP6CE is a fully functioned Fractional-N Phase-Locked-Loop (PLL) with an Integrated Voltage Controlled Oscillator (VCO). The PLL consists of an integrated low noise VCO with a tri-band output, an autocalibration subsystem for low voltage VCO tuning, a very low noise digital Phase Detector (PD), a precision controlled charge pump, a low noise reference path divider and a fractional divider.

The fractional PLL features an advanced delta-sigma modulator design that allows both ultra-fine step sizes and low spurious products. The phase detector (PD) features cycle slip prevention (CSP) technology to allow faster frequency hopping times. Ultra low in-close phase noise and low spurious also allows wider loop bandwidths for faster frequency hopping and low micro-phonics.

For theory of operation and register map refer to the "PLLs with Integrated VCOs - RF VCOs Operating Guide". To view the Operating Guide, please visit www.hittite.com and choose HMC838LP6CE from the "Search by Part Number" pull down menu.

Electrical Specifications, T_A = +25° C, VPPCP, VDDCP, VCC1, VCC2 = 5V ±4%; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3V ±6% GNDCP = GNDLS = Ground Paddle = 0V, 50 MHz Reference Unless Otherwise Noted

Parameter	Condition	Min.	Typ.	Max.	Units
RF Output Characteristics					
VCO Frequency at PLL Input		1590	1710	1890	MHz
RF Output Frequency at $f_{VCO}/2$		795	855	945	MHz
RF Output Frequency at f_{VCO}		1590	1710	1890	MHz
RF Output Frequency at $2f_{VCO}$		3180	3420	3780	MHz
RF Output Power at $f_{VCO}/2$		7.5	10	12.5	dBm
RF Output Power at f_{VCO}		4.5	7.5	11	dBm
RF Output Power at $2f_{VCO}$		-9	-4	1	dBm
VCO Tuning Sensitivity	Measured at fo, 2V (N= 0/15/31)	8	11	16	MHz/V
VCO Supply Pushing	Measured at fo, 2V		1.3		MHz/V
RF Output fo/2 Harmonic	Doubler Mode		-24		dBc
RF Output 3fo/2 Harmonic	Doubler Mode		-38		dBc
RF Output 2nd Harmonic	fo/2/fo/2fo		-25 / -22 / -28		dBc
RF Output 5fo/2 Harmonic	Doubler Mode		-50		dBc
RF Output 3rd Harmonic	fo/2/fo/2fo		-29 / -32 / -50		dBc
RF Output 7fo/2 Harmonic	Doubler Mode		-57		dBc
RF Output 4th Harmonic	fo/2/fo/2fo		-30 / -42 / -57		dBc
RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +3) dynamically max	20		524,283	
REF Input Characteristics					
Ref Input Frequency	Synthesizer phase noise can degrade by about 5dB when operating with a reference frequency near the low end of this range.	10	50	200	MHz
Ref Input Range	AC Coupled	1	2	3.3	Vpp
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	

Electrical Specifications (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
Phase Detector (PD)					
PD Frequency Fractional Feedback Mode	[1]	0.1		100	MHz
PD Frequency Fractional Feedforward Mode (and Register 6 [17:16] = 10)		0.1		80	MHz
PD Frequency Integer Mode	[1]	0.1		125	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	Input Referred, Maximum CP Current				
100 Hz			-132		dBc/Hz
1 kHz			-142		dBc/Hz
10 kHz	Add 1 dB for Fractional	-151	-149	-147	dBc/Hz
100 kHz	Add 3 dB for Fractional	-155	-153	-151	dBc/Hz
Logic Inputs					
VIH Output High Voltage		DVDD3V-0.4		DVDD3V	V
VIL Output Low Voltage		0		0.4	V
Logic Outputs					
VOH Output High Voltage		DVDD3V-0.4		DVDD3V	V
VOL Output Low Voltage		0		0.4	V
Power Supply Voltages					
Analog 3.3V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD	3.0	3.3	3.5	V
Digital Supply	DVDD3V	3.0	3.3	3.5	V
Analog 5V Supplies	VPPCP, VDDCP, VCC1, VCC2	4.8	5	5.2	V
Power Supply Currents					
+5V Analog Charge Pump	VPPCP, VDDCP		5.3		mA
+5V VCO, PLL Buffer and RF Buffer	VCC1 + VCC2 (fo / 2 / fo / 2fo)		88 / 72 / 71		mA
+3.3V Analog	AVDD, VCCHF, VCCPS, VCCPD, RVDD		45		mA
+3.3V Digital	DVDD3V		6.5		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		10	200	µA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
VCO Open Loop Phase Noise at fo/2					
10 kHz Offset			-93		dBc/Hz
100 kHz Offset			-123		dBc/Hz
1 MHz Offset			-148		dBc/Hz
10 MHz Offset			-163		dBc/Hz
100 MHz Offset			-166		dBc/Hz

Note 1: This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional feedback mode, the maximum PFD rate = fvco/20 or 100 MHz, whichever is less.

Electrical Specifications (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
VCO Open Loop Phase Noise at fo					
10 kHz Offset			-88		dBc/Hz
100 kHz Offset			-118		dBc/Hz
1 MHz Offset			-143		dBc/Hz
10 MHz Offset			-162		dBc/Hz
100 MHz Offset			-168		dBc/Hz
VCO Open Loop Phase Noise at 2fo					
10 kHz Offset			-81		dBc/Hz
100 kHz Offset			-112		dBc/Hz
1 MHz Offset			-135		dBc/Hz
10 MHz Offset			-157		dBc/Hz
100 MHz Offset			-160		dBc/Hz
Closed Loop Phase Noise PLL + VCO at fvco/2					
Integer, 50 MHz PD	1 kHz Offset		-119		dBc/Hz
Integer, 50 MHz PD	10 kHz Offset		-123		dBc/Hz
Integer, 50 MHz PD	100 kHz Offset		-119		dBc/Hz
Fractional, 50 MHz PD	1 kHz Offset		-113		dBc/Hz
Fractional, 50 MHz PD	10 kHz Offset		-115		dBc/Hz
Fractional, 50 MHz PD	100 kHz Offset		-121		dBc/Hz
Closed Loop Phase Noise PLL + VCO at fvco					
Integer, 50 MHz PD	1 kHz Offset		-114		dBc/Hz
Integer, 50 MHz PD	10 kHz Offset		-118		dBc/Hz
Integer, 50 MHz PD	100 kHz Offset		-113		dBc/Hz
Fractional, 50 MHz PD	1 kHz Offset		-107		dBc/Hz
Fractional, 50 MHz PD	10 kHz Offset		-108		dBc/Hz
Fractional, 50 MHz PD	100 kHz Offset		-115		dBc/Hz
Closed Loop Phase Noise PLL + VCO at 2fo					
Integer, 50 MHz PD	1 kHz Offset		-108		dBc/Hz
Integer, 50 MHz PD	10 kHz Offset		-112		dBc/Hz
Integer, 50 MHz PD	100 kHz Offset		-107		dBc/Hz
Fractional, 50 MHz PD	1 kHz Offset		-100		dBc/Hz
Fractional, 50 MHz PD	10 kHz Offset		-102		dBc/Hz
Fractional, 50 MHz PD	100 kHz Offset		-109		dBc/Hz
Synthesizer Figure of Merit	Normalized 1 Hz				
Integer Mode	Measured w/ 50 MHz PD at 30 kHz Offset		-229		dBc/Hz
Fractional Mode	Measured w/ 50 MHz PD at 30 kHz Offset		-227		dBc/Hz

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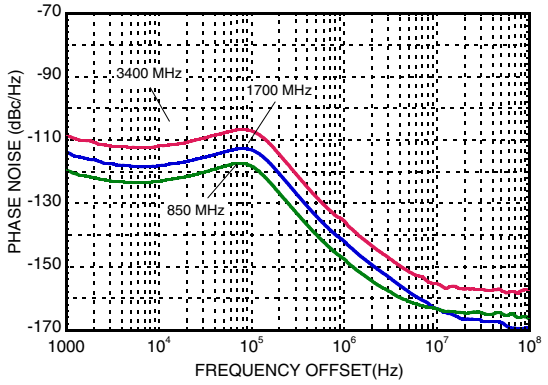
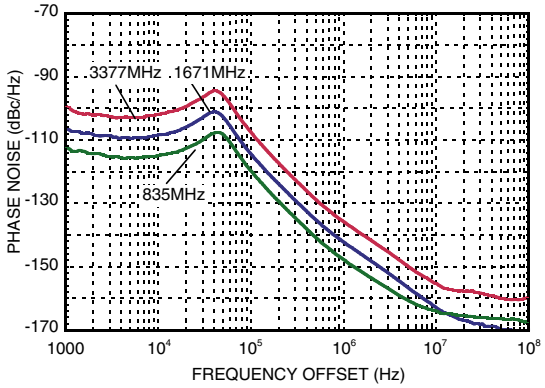
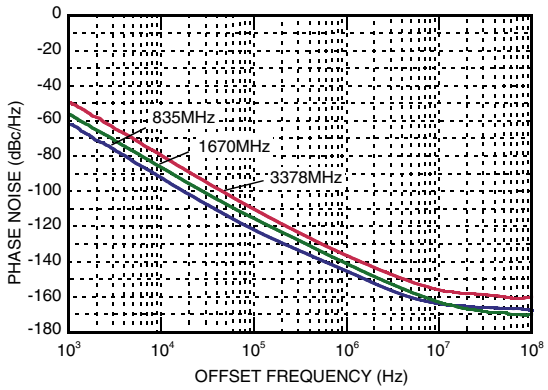
Closed Loop Integer Phase Noise



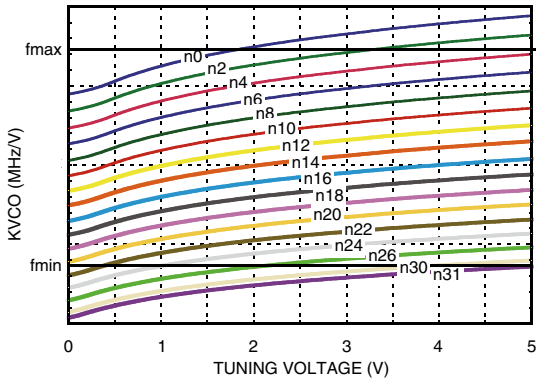
Typical Closed Loop Fractional Phase Noise [1]



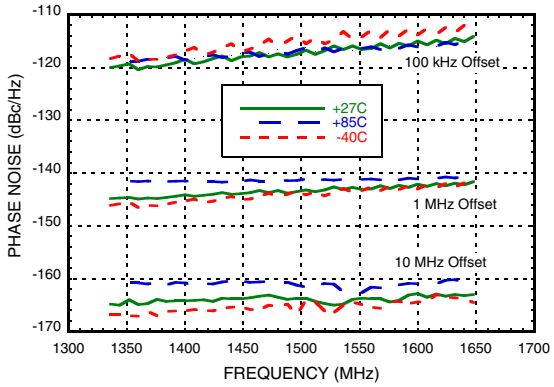
Free Running Phase Noise



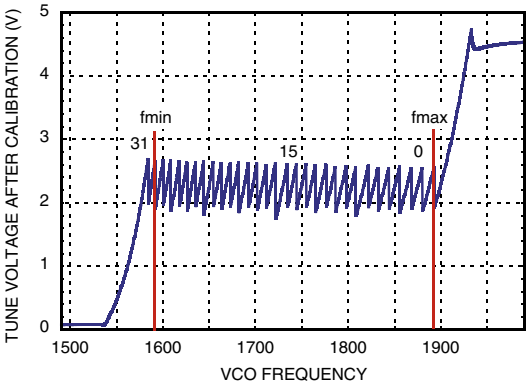
Typical Tuning Curves vs. Switch Position



Free Running VCO Phase Noise Over Temperature

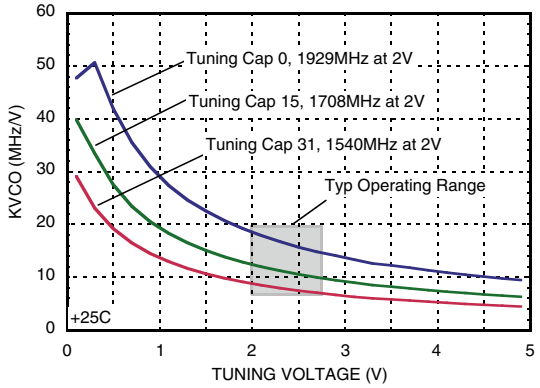


Typical VCO Tuning Voltage After Calibration

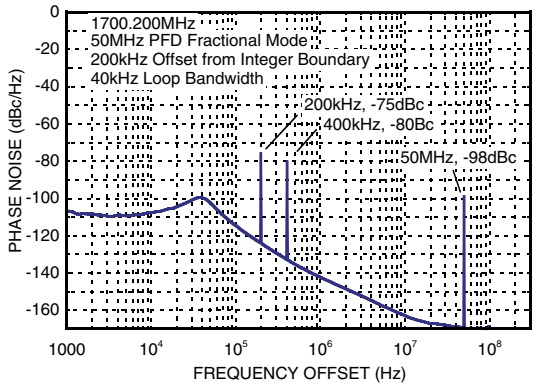


[1] Fractional Mode, 50 MHz Crystal, R=1

Typical VCO Sensitivity vs. Cap @ Fo Voltage



Typical Spurious @ 200 kHz from Integer Boundary



Typical Output Power - Narrow Band Match

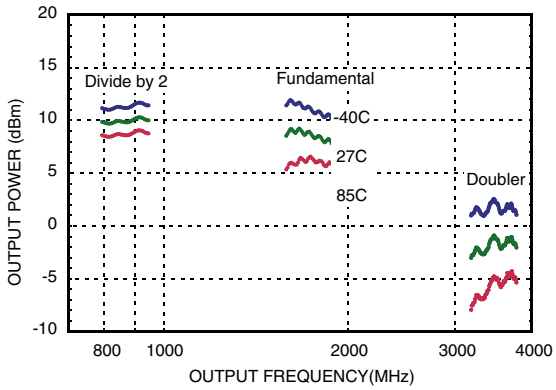
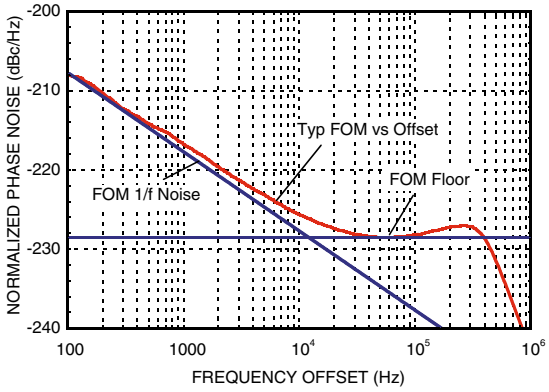


Figure of Merit



Pin Descriptions

Pin Number	Function	Description
1	AVDD	DC Power Supply for analog circuitry.
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 34, 37, 38	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	Power Supply for charge pump analog section
4	CP	Charge Pump Output
7	VDDCP	Power Supply for the charge pump digital section
10	RVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	VCO Analog Supply 2
27	VCC1	VCO Analog Supply 1
28	RF_N [1]	RF Positive Output
29	RF_P [1]	RF Negative Output
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	DC Power Supply for Analog Circuitry
36	VCCPS	DC Power Supply for Analog Prescaler
39	VCCPD	DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V ±20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10GΩ meter such as Agilent 34410A, normal 10MΩ DVM will read erroneously.

[1] For doubler mode of operation, pin 28 (RF_N) and pin 29 (RF_P) outputs must be shorted together.

Absolute Maximum Ratings

AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS	-0.3V to +3.6V
VPPCP, VDDCP, VCC1	-0.3V to +5.5V
VCC2	-0.3V to +5.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 125°C
Maximum Junction Temperature	150 °C
Thermal Resistance (Θ_{JC}) [junction to case (ground paddle)]	9 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

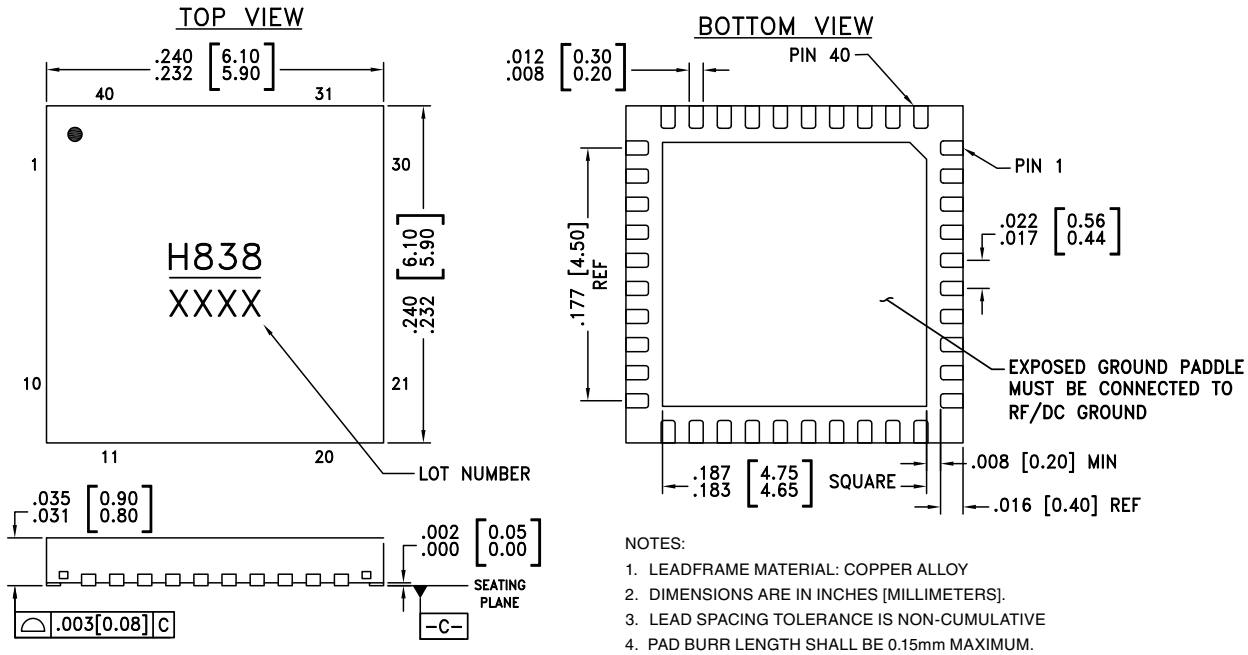
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Condition	Min.	Typ.	Max.	Units
Temperature					
Junction Temperature		-	-	125	°C
Ambient Temperature		-40	-	85	°C
Supply Voltage					
AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS		3.0	3.3	3.5	V
VPPCP, VDDCP, VCC1, VCC2		4.8	5	5.2	V

[1] Layout design guidelines set out in Qualification Test Report are strongly recommended.

Outline Drawing



NOTES:

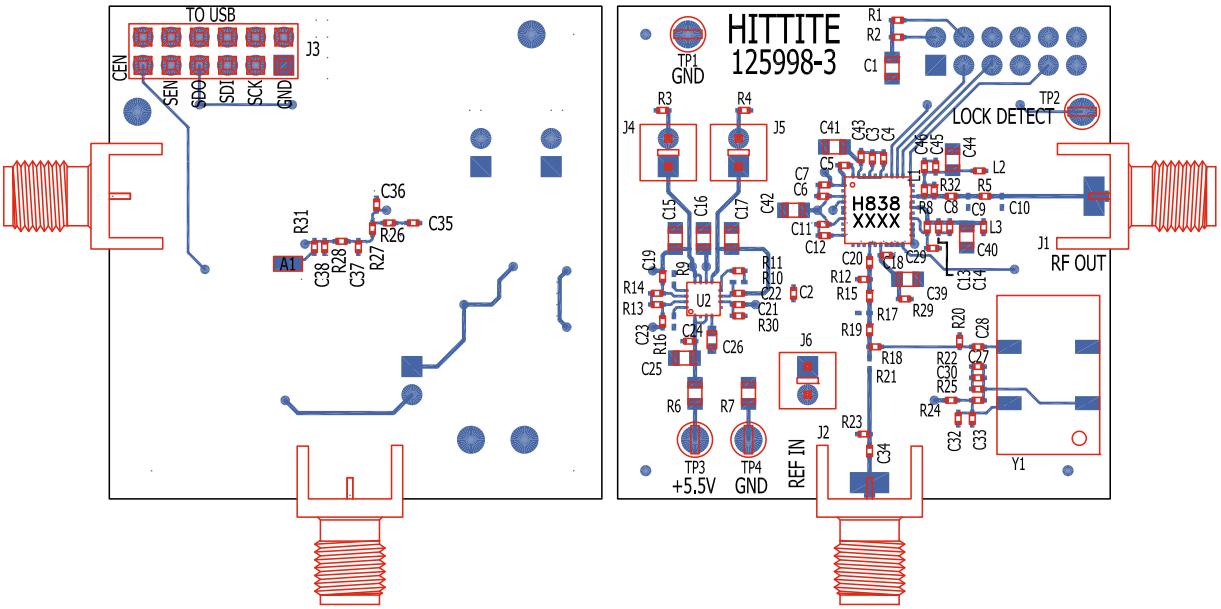
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC838LP6CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H838 XXXX

[1] 4-Digit lot number XXXX

Evaluation PCB, fo & fo/2 Modes



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC838LP6CE from the "Search by Part Number" pull down menu to view the product splash page.

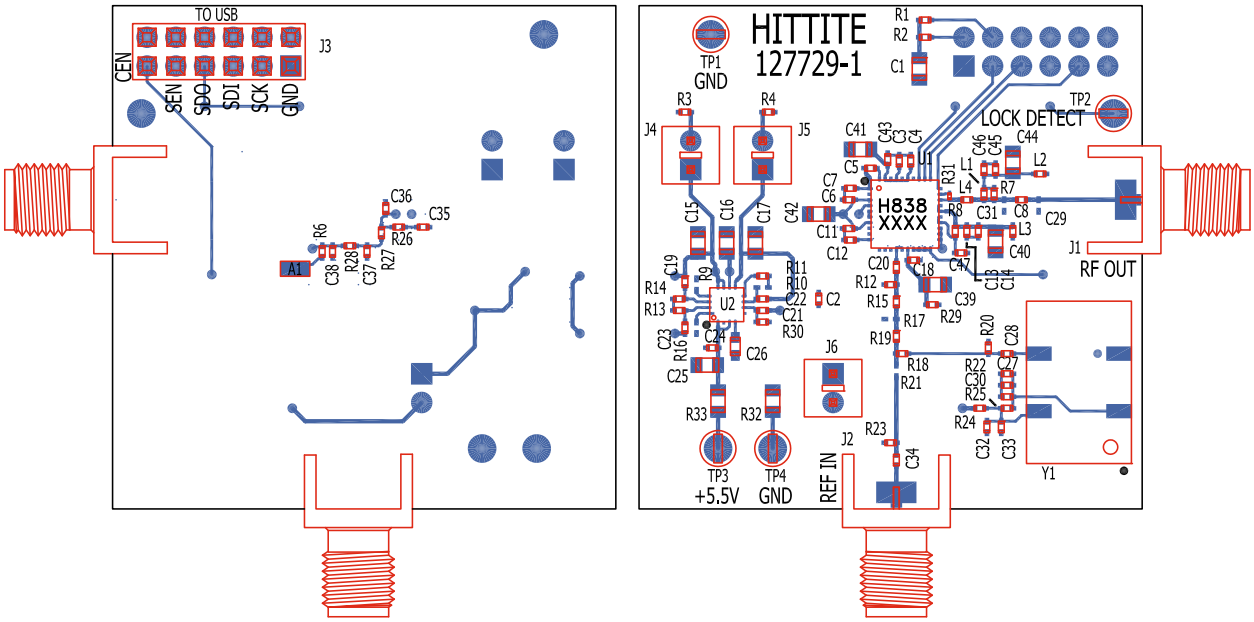
List of Materials for Evaluation PCB 129511, fo & fo/2 Mode [1]

Item	Description
J1, J2	PCB Mount SMA RF Connector
J3	Dual Row Terminal Strip
J4 - J6	Connector Header
C1, C15 - C17, C25	10 µF Capacitor, 0805 Pkg.
C2, C3, C6, C7, C11, C12, C14, C18, C27, C43, C45	0.47 µF Capacitor, 0402 Pkg.
C4, C13	22 pF Capacitor, 0402 Pkg.
C5, C33	1000 pF Capacitor, 0402 Pkg.
C8	1.8 pF Capacitor, 0402 Pkg.
C19 - C24, C28, C30, C32, C34	0.1 µF Capacitor, 0402 Pkg.
C26	1 µF Capacitor, 0603 Pkg.
C29	47 pF Capacitor, 0402 Pkg.
C35	3300 pF Capacitor, 0402 Pkg.
C36	270 pF Capacitor, 0402 Pkg.
C37, C38	68 pF Capacitor, 0402 Pkg.
C39 - C42, C44	4.7 µF Tantalum Capacitor, 0805 Pkg
R1, R2, R5, R8, R11, R15, R18, R19, R21, R24	0 Ohm Resistor, 0402 Pkg.
R3, R4	1 Ohm Resistor, 0402 Pkg.
R6, R7	0 Ohm Resistor, 0805 Pkg.
R12, R20, R29	51 Ohm Resistor, 0402 Pkg.
R22, R25	20 kOhm Resistor, 0402 Pkg.
R26 - R28	1k Ohm Resistor, 0402 Pkg.
L1	6.8 nH Inductor, 0402 Pkg.
TP3, TP4	Test Point PC Compact SMT
U1	HMC838LP6CE PLL with Integrated VCO
U2	HMC860LP3E Low Noise Quad Linear Regulator
Y1	3.3V, 50 MHz VCXO Crystal Oscillator
PCB [2]	125998 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR and FR4

Evaluation PCB, 2xfo Mode



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Evaluation PCB Schematic

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List of Materials for Evaluation PCB 129512, 2xfo Mode [1]

Item	Description
J1, J2	PCB Mount SMA RF Connector
J3	Dual Row Terminal Strip
J4 - J6	Connector Header
C1, C15 - C17, C25	10 µF Capacitor, 0805 Pkg.
C2, C3, C6, C7, C11, C12, C14, C18, C27, C43, C45	0.47 µF Capacitor, 0402 Pkg.
C4, C13	22 pF Capacitor, 0402 Pkg.
C5, C33	1000 pF Capacitor, 0402 Pkg.
C8	8.2 pF Capacitor, 0402 Pkg.
C19 - C24, C28, C30, C32, C34	0.1 µF Capacitor, 0402 Pkg.
C26	1 µF Capacitor, 0603 Pkg.
C29	1 pF Capacitor, 0402 Pkg.
C35	3300 pF Capacitor, 0402 Pkg.
C36	270 pF Capacitor, 0402 Pkg.
C37, C38	68 pF Capacitor, 0402 Pkg.
C39 - C42, C44	4.7 µF Tantalum Capacitor, 0805 Pkg
C46	27 pF Capacitor, 0402 Pkg.
C47	47 pF Capacitor, 0402 Pkg.
R1, R2, R8, R11, R15, R18, R19, R21, R24	0 Ohm Resistor, 0402 Pkg.
R3, R4	1 Ohm Resistor, 0402 Pkg.
R12, R20, R29	51 Ohm Resistor, 0402 Pkg.
R13, R14, R30	220 kOhm Resistor, 0402 Pkg.
R22, R25	20 kOhm Resistor, 0402 Pkg.
R26 - R28	1 kOhm Resistor, 0402 Pkg.
R31	0 Ohm Resistor, 0201 Pkg.
R32, R33	0 Ohm Resistor, 0805 Pkg.
L1	10 nH Inductor, 0402 Pkg.
L2, L3	47 nH Inductor, 0402 Pkg.
L4	1 nH Inductor, 0402 Pkg.
TP3, TP4	Test Point PC Compact SMT
U1	HMC838LP6CE PLL with Integrated VCO
U2	HMC860LP3E Low Noise Quad Linear Regulator
Y1	3.3V, 50 MHz VCXO Crystal Oscillator
PCB [2]	127729 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR and FR4

Notes: