Power System Sequencer
TRKF- 44D62ER

On Board Power System Controller **RoHS Compliant**

- Digital Signal Processor (DSP) Based with Bel Firmware
- Provides Power Up and Power Down Sequencing Logic
- Stand Alone or Command Based Feature Set
- Fault Detection and Reporting
- 44 Pin 10mm x 10mm TQFP package
- I2C, SMBus, or PMBus compatible serial interface options
- Configurable through serial interface, Customizable through software
- 3V3 logic levels
- Voltage Margining via Closed Loop Trim
- Programmed parameters saved in non volatile memory
- Intelligent configuration capability

Description

This on board power system controller provides a cost effective high performance solution for controlling, monitoring, and sequencing multiple Point of Load (POL) converters on a system board. The sequencer uses a digital signal processor (DSP) engine and Bel's firmware to implement a portfolio of board level control features typically required in a multiple voltage configuration. The solution can control and monitor up to four PoL converters and monitor up to two analog inputs. The 44 pin TRKF-44D62ER is derived from Bel's 64 pin TRKF-64D82ER platform with less I/O offering a lower cost option for smaller boards.

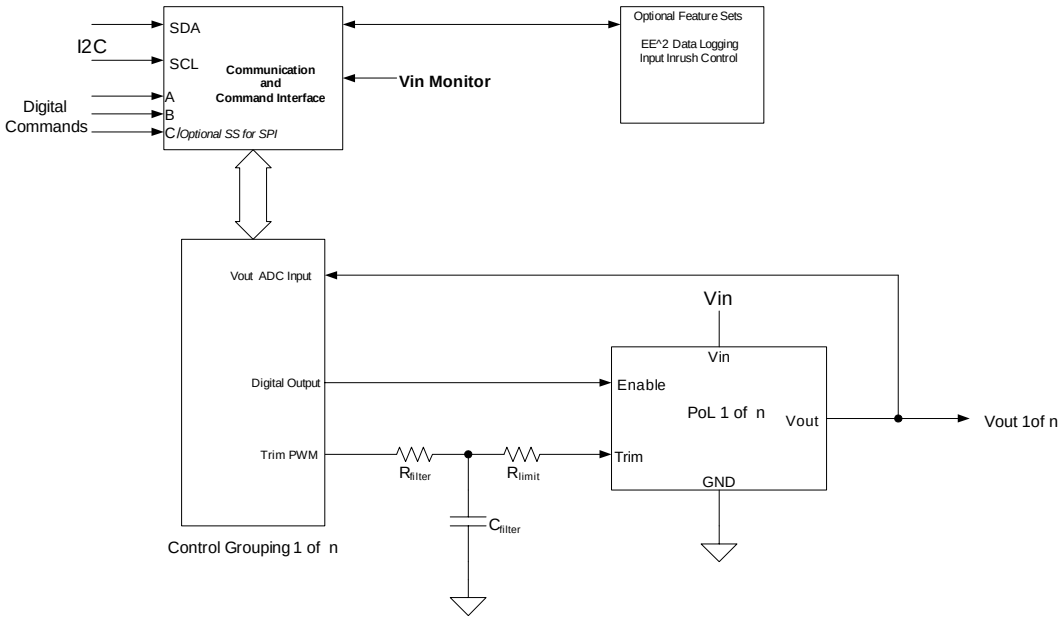


Figure 1
Functional Block Diagram

I/O Definitions

Pin No.	Pin Name	Type	Signal Description
1	I2CDATA	I2C	I2C DATA
2	POL_4_ENABLE	Output	POL 4 Enable
3	POL_3_ENABLE	Output	POL 3 Enable
4	POL_2_ENABLE	Output	POL 2 Enable
5	POL_1_ENABLE	Output	POL 1 Enable
6	VSS	Power	3.3V Power Input Return
7	VCAP/VDDCORE	Power	Core Decoupling Capacitor
8	IOPIF_ENABLE	Output	
9	RESET_OUT	Output	Reset signal
10	POL_4_MGN_PWM	PWM Margin out	POL 4 PWM Trim
11	POL_3_MGN_PWM	PWM Margin out	POL 3 PWM Trim
12	PWR_GOOD	Output	System power good signal
13	WARNING	Output	Warning signal
14	POL_2_MGN_PWM	PWM Margin out	POL 2 PWM Trim
15	POL_1_MGN_PWM	PWM Margin out	POL 1 PWM Trim
16	AVSS	Power	Analog Ground
17	AVDD	Power	Filtered VDD (analog VDD)
18	MCLR*	Input/Power	Master clear reset
19	REF_IN	Analog input	Vref+
20	REF_RETURN	Analog input	Vref-
21	POL_MONITOR_1	Analog Input	POL 1 Monitor
22	POL_MONITOR_2	Analog input	POL 2 Monitor
23	POL_MONITOR_3	Analog input	POL 3 Monitor
24	POL_MONITOR_4	Analog input	POL 4 Monitor
25	VIN_MONITOR	Analog input	Vin Monitor
26	ANALOG_MON_X	Analog input	Vcc CMD Measure
27	ANALOG_MON_Y	Analog Input	PIF Output Measure
28	VDD	Power	3.3V Power Input
29	VSS	Power	3.3V Power Input Return
30	BOARD_SEATED	Digital input	Indicates if board plugged in
31	MFG_MODE	Digital input	Indicates if in manufacturing mode
32	SPARE1	I/O	Spare I/O
33	VID_INPUT_6	Digital input	
34	VID_INPUT_5	Digital input	
35	VID_INPUT_4	Digital input	
36	VID_INPUT_3	Digital input	
37	VID_INPUT_2	Digital input	
38	VID_INPUT_1	Digital input	
39	VSS	Power	3.3V Power Input Return
40	VDD	Power	3.3V Power Input
41	MGN_HI_N/ICD_SDA	Digital input	Mgn_hi / ICD debug port
42	MGN_LO_N/ICD_SCL	Digital input	Mgn_lo / ICD debug port
43	RESET_IN	Digital input	Reset input from SP
44	I2CCLOCK	I2C	I2C CLOCK

Powering the Sequencer

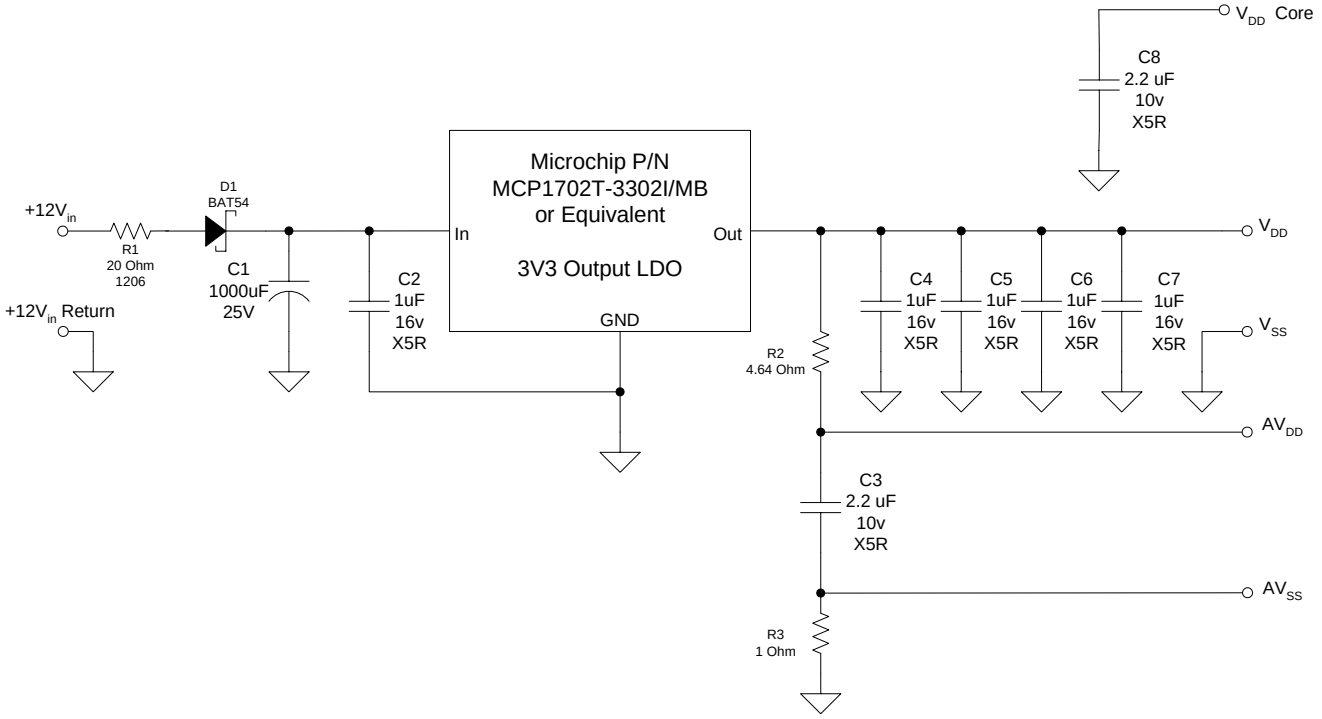


FIGURE 2
V_{DD} Interface

Figure 2 is a schematic of the typical V_{DD} interface to the sequencer IC. A Microchip LDO, P/N MCP1702T-3302I/MB, is used to produce the 3.3V V_{DD} supply to the DSP. This device is in a SOT89 package and in most applications will be sufficient in size to handle the power dissipation when powering the circuit from a 12V source. Capacitors C4, C5, C6, and C7 are the decoupling capacitors for the DSP and they should be located directly across each pair of V_{DD} and V_{SS} pins on the DSP IC. The 44 pin device has a V_{DD} core pin which is used to decouple the internally generated core voltage. Capacitor C8 is the decoupling capacitor for the VDD core which is not required with the 44 pin device. This decoupling capacitor should be a low ESR ceramic capacitor and can be as large as 10uF. Capacitor C3 is the decoupling capacitor for the analog V_{DD} (AV_{DD}) and it should be located directly across the AV_{DD} and AV_{SS} pins on the DSP IC. Resistor R2 in combination with C3 provides a filter for the analog V_{DD}. Resistor R3 is intended to separate AV_{SS} from V_{SS}. Capacitor C2 is the input decoupling capacitor for the LDO and it should be connected directly across the LDO's input and ground pins. Capacitor C1 is used as a hold up capacitor. Its purpose is to hold up the supply voltage to the LDO and maintain a stable V_{DD} for the DSP for a short period after the +12V_{in} source is removed. This would be desired if a short communication stream is required during power down or if storing system data to EE memory is required during power down. The Schottky diode D1 prevents C1 from being discharged after +12V_{in} is removed. Resistor R1 is used to protect D1 during the inrush event associated with the application of the +12V_{in}. The single pulse peak current rating for a typical BAT54 diode is approximately 600mA. If the rise time of the +12V source is slow enough to limit the peak charging current into C1 it is possible to eliminate R1. Assuming a 40mA current draw by the DSP C1 will provide approximately 188 uS of hold up time per uF of capacitance.

Using the PWM Trim Outputs

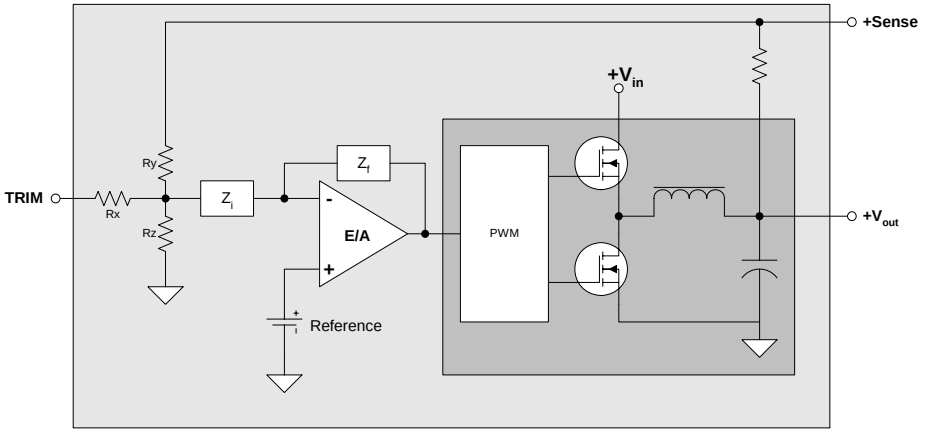


Figure 3A.

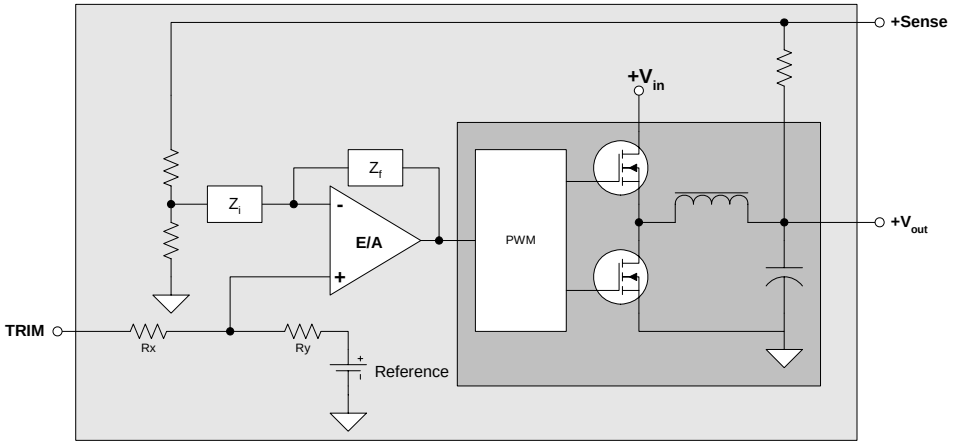


Figure 3B.

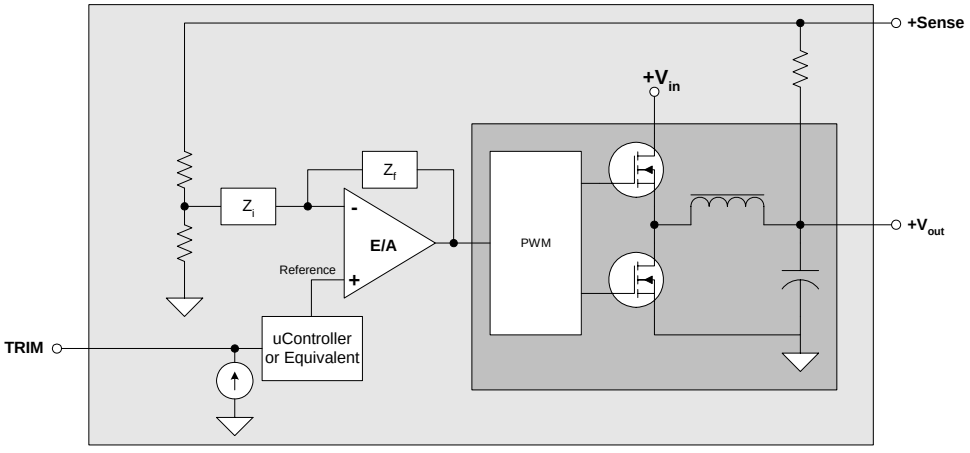


Figure 3C.

The drawings in figure 3 show the three most common trim methods used in PoL converters. In all of these schemes a power conversion stage contains a PWM device that receives a control voltage from an error amplifier. The error amplifier (E/A) compares a scaled version of the output voltage to a reference. The output voltage of the converter module is simply the reciprocal of the scaling factor multiplied by the reference value. The output voltage can be adjusted by changing this scaling factor (Figure 3A) or by modifying the reference (Figures 3B, C).

The most common trim method is shown in figure 3A. The popularity of this method stems from the fact that most highly integrated PWM control IC's have an internal reference that is not accessible and cannot be controlled externally. In this scheme the output is scaled by adding a resistor from the trim pin to ground. This modifies the feedback divider and moves the output voltage to a higher value. The output can also be modified by superimposing an offset voltage on the feedback divider by connecting a voltage source to the trim pin through a resistor. Either of these two approaches will move the output voltage to a new value. The common characteristic of modules with this trim scheme is that a lower value trim resistor to ground will cause a higher output voltage or a larger voltage superimposed on the trim pin will cause V_{out} to decrease.

Some PoL converters incorporate the trim scheme shown in figure 3B. With this method the feedback ratio is kept constant and the reference value is modified to move the output voltage. The common characteristic of modules with this trim scheme is that a lower value trim resistor to ground will cause a lower output voltage and a larger voltage superimposed on the trim pin will cause V_{out} to increase.

The method shown in figure 3C is occasionally used. This is similar to the method in figure 3B except the modification of the reference is mapped through a device such as a microcontroller. This is the least common of the 3 methods and requires the vendor's data sheet to determine the trim characteristic because the micro controller can map the reference in many different ways.

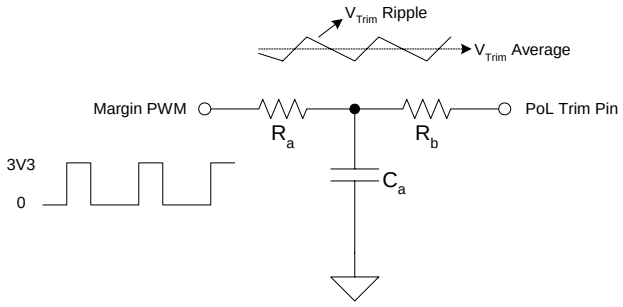


Figure 4A

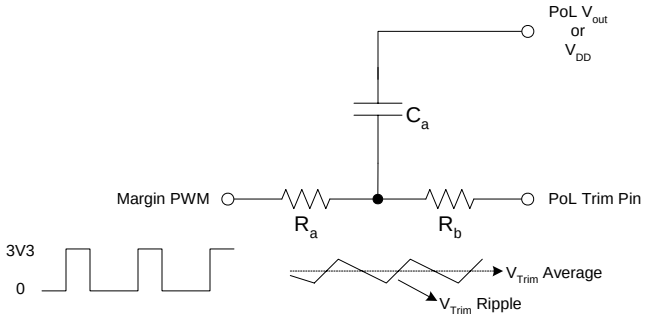


Figure 4B

The power sequencer has the ability to do independent closed loop trim and closed loop margining of the output voltage for each PoL controlled by the device. Each PoL's output voltage is monitored and by an analog to digital converter (ADC) in a continuous loop. In firmware the most recent measured output voltage is compared against the desired value and the PoL's output is adjusted by delivering a trim value to the corresponding PoL's trim pin. This trim voltage is created from a digital PWM output and an external low pass filter. Each digital PWM is labeled <PoL "n" Margin PWM> where n indicates a specific converter which corresponds to the monitoring channel labeled with the same "n" value. The external low pass filter creates a DC value from the PWM signal which is then delivered to each PoL converter through a range limiting resistor.

Figure 4 shows the typical circuits used to interface the sequencers Margin PWM signals to PoL converters. In each of the circuits shown R_a and C_a construct a low pass filter while R_b is used to limit the trim range. The effective trim voltage is equal to the Margin PWM duty cycle multiplied by V_{DD} and is controllable in 1024 steps from 0 to V_{DD}. The effective trim resistor value is equal to $R_a + R_b$. R_a and C_a are chosen to reduce the trim voltage ripple. Typical values for Ra and Ca are 1K for Ra and 0.22uF to 1uF for C_a. R_b is used to limit the

control range and should be selected based on the desired control range and the trim equation for the PoL. This trim equation is usually available from the PoL manufactures data sheet. The sequencer learns the trim direction by making a minor adjustment to the Margin PWM and then determining the direction that V_{out} moves based on this stimulus. Once the trim direction is known it knows whether increment or decrement the TRIM PWM value until the desired V_{out} is achieved. The accuracy of the active trim is a function of the ADC accuracy which is mostly controlled by accuracy of the applied reference to the sequencers V_{ref} pins.

Either circuit in Figure 4 will work with any of the trim methods shown in Figure 3. When interfacing to PoL modules that use the trim method in Figure 3A the circuit in Figure 4B is the optimum interface configuration. By connecting the filter capacitor Ca to the PoL's Vout or to a positive voltage reference the effective of filtering the Margin PWM signal remains intact. With this method there will not be a discharged capacitor connected to ground that could cause the PoL's output to overshoot during power up as this capacitor becomes charged. In the case that the circuit in figure 4A is used with the trim configuration in Figure 3B the sequencer will pre-charge the capacitor before enabling the PoL converter and then decrement the Margin PWM to achieve the desired V_{out}. This requires additional start up time during system initialization. When interfacing to PoL converters of the type shown in Figure 3B the interface circuit in figure 4A is optimum.

Monitoring Via ADC Channels

The imbedded ADC channels are converted as 10 bit results with full scale equal to a chosen reference. The device is intended to be powered from a 3V3 source and can be configured to use this source as the ADC reference or to use an externally provided reference. Closed loop margining and set point adjustments always use the entire 10 bit result to trim the output voltages to loaded values. Monitored voltages are reported via I2C communication using PMBus data formats as defined in the separate communication manual. The voltage range reported is determined by the entered set points. Any monitored output that is greater than the ADC reference or that can be margined above this reference should have a voltage divider to limit the maximum input to the corresponding ADC channel to a value equal or less than the ADC reference. Monitored voltages below the chosen ADC reference do not require this voltage divider. A four sample moving average is used to filter the ADC results. In most cases this will eliminate the need for external filtering.

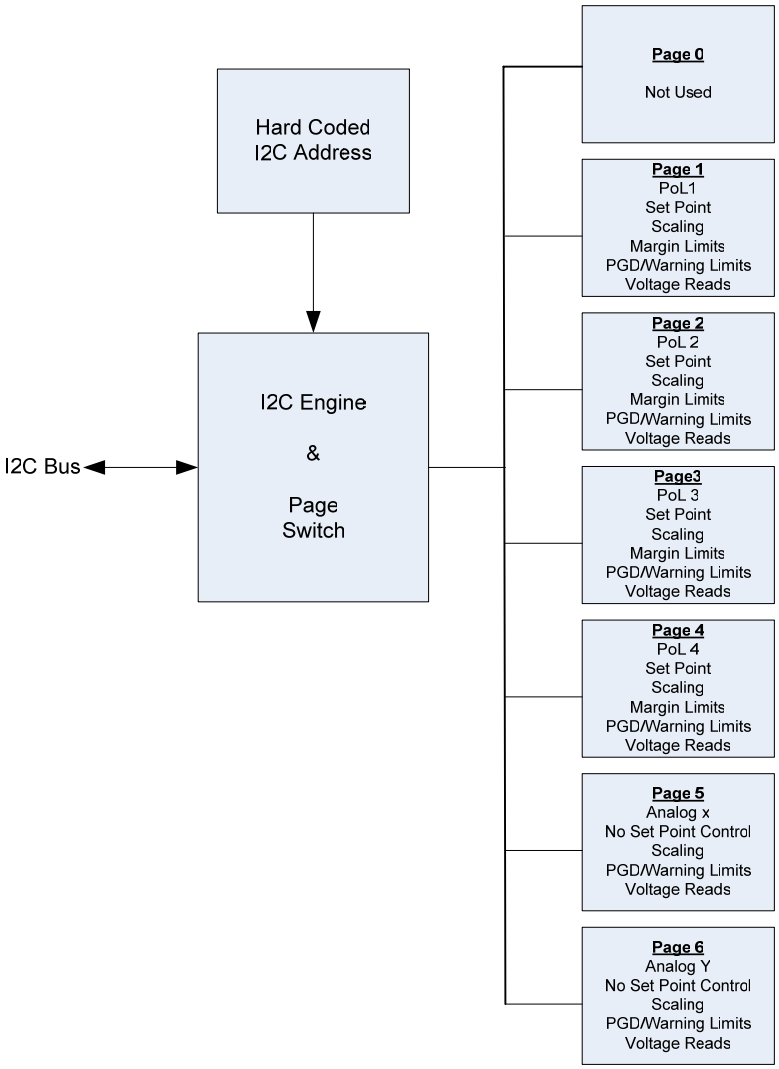
The input voltage (V_{in}) monitoring channel requires a voltage divider so that V_{in} maximum is scaled to a value less than the maximum value of the ADC reference.

Connecting the Control and Monitoring

The three primary control interface signals to the attached PoL converters are an enable signal, a voltage monitoring signal, and trim control signal. The enable signals are labeled <PoL "n" Enable>. The Monitoring signals are labeled <PoL Monitor "n">. The trim signals are labeled <PoL "n" Margin PWM>. Each n'th PoL converter is required to share the corresponding enable, monitor, and trim signals. For example the first PoL converter attached to the controller is PoL 1. PoL 1 should use <PoL 1 Enable>, <PoL Monitor 1>, and PoL 1 Margin PWM, etc.. The installed firmware assumes that the connections are made this way when controlling system.

Communicating to the Device

Serial communication is achieved via an I2C bus. The communication protocol is derived from the PMBus command set and is defined in a separate communications manual. The communications manual also defines the protocol for device programming via embedded boot loader software.


Hard Coded
I2C Address
I2C Engine
&
Page
Switch
I2C Bus
Page 0
Not Used
Page 1
PoL1
Set Point
Scaling
Margin Limits
PGD/Warning Limits
Voltage Reads
Page 2
PoL 2
Set Point
Scaling
Margin Limits
PGD/Warning Limits
Voltage Reads
Page3
PoL 3
Set Point
Scaling
Margin Limits
PGD/Warning Limits
Voltage Reads
Page 4
PoL 4
Set Point
Scaling
Margin Limits
PGD/Warning Limits
Voltage Reads
Page 5
Analog x
No Set Point Control
Scaling
PGD/Warning Limits
Voltage Reads
Page 6
Analog Y
No Set Point Control
Scaling
PGD/Warning Limits
Voltage Reads

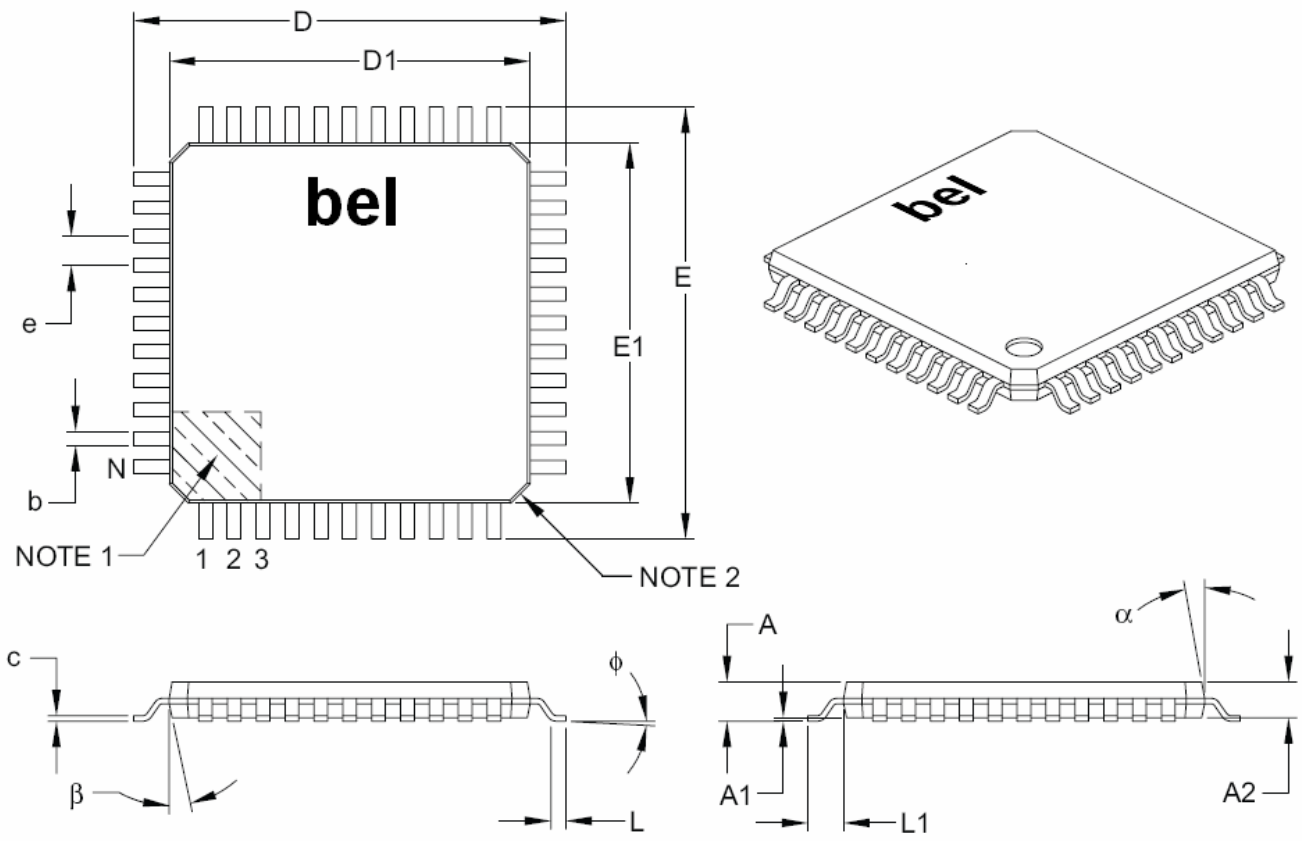
Absolute Maximum Ratings

Ambient temperature under bias..... .-40℃ to +85℃
Storage temperature ..... -65℃ to +150℃
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any combined analog and digital pin and MCLR, with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any digital-only pin with respect to V_{SS} ..... -0.3V to +5.6V
Voltage on V_{DDCORE} with respect to V_{SS} ..... 2.25V to 2.75V
Maximum current out of V_{SS} pin .....300 mA
Maximum current into V_{DD} pin ....250 mA
Maximum output current sunk by any I/O pin.....4 mA
Maximum output current sourced by any I/O pin .....4 mA
Maximum current sunk by all ports .....200 mA
Maximum current sourced by all ports .....200 mA

Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Input Voltage Range	V_{DD}	3.0	3.30	3.6	VDC	
Input Current	I_{DD}		58		mA	+85C
Logic Low Input Level	V_{IL}	V_{SS}		0.2*V_{DD}	VDC	
Logic High Input Level	V_{IH}	0.8*V_{DD}		V_{DD}	VDC	
Logic Low Output Level	V_{OL}			0.4	VDC	V_{DD} = 3.3V
Logic High Output Level	V_{OH}	2.4			VDC	V_{DD} = 3.3V, I_{OH} = -3.0mA
VDD Rise Rate	SV_{DD}	0.05			V/uS	0 to 3.3V in 100mS
Capacitance I/O Pin to GND	C_{IO}			50	pF	
I2C Bus Capacitance	C_B			400	pF	SCl and SDA
PWM Series Resistor	R_{PWM}	1			KΩ	External Series Resistor
Margin PWM Frequency	F_{PWM}		10		KHz	
Reference Input	Vref	AV_{SS} + 1.7		AV_{DD}	VDC	

Mechanical Outline



Bel 44-pin 10x10x1mm TQFP Sequencer

Figure 5A

44-Lead Plastic Thin-Quad Flatpack, 10 x 10 x 1mm Body				
	Units	**Millimeters**		
	Dimension Units	Min	Nom	Max
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Champers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Figure 5B

RoHS Compliance

Complies with the European Directive 2002/95/EC, calling for the elimination of lead and other hazardous substances from electronic products.