HMC624LP4 / 624LP4E

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 6 GHz

Typical Applications

The HMC624LP4(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

0.5 dB LSB Steps to 31.5 dB

Power-Up State Selection

High Input IP3: +55 dBm

Low Insertion Loss: 2.2 dB @ 3.5 GHz

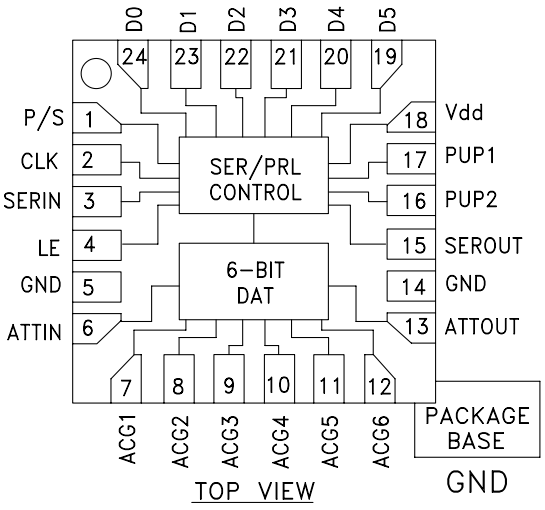
TTL/CMOS Compatible, Serial, Parallel or Latched Parallel Control

±0.25 dB Typical Step Error

Single +3V or +5V Supply

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

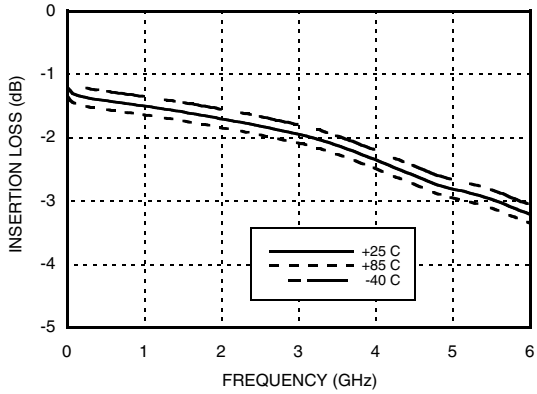
The HMC624LP4(E) is a broadband 6-bit GaAs IC Digital Attenuator in a low cost leadless SMT package. This versatile digital attenuator incorporates off-chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 6 bit parallel word. The HMC624LP4(E) also features a user selectable power up state and a serial output port for cascading other Hittite serial controlled components. The HMC624LP4(E) is housed in a RoHS compliant 4x4 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25° C, 50 Ohm System, with Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 3 GHz 3.0 - 6.0 GHz		1.8 2.8	2.4 3.8	dB dB
Attenuation Range			31.5		dB
Return Loss (ATTIN, ATTOUT, All Atten. States)	DC - 6 GHz		15		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	DC - 0.8 GHz 0.8 - 6.0 GHz	± (0.10 + 5% of Atten. Setting) Max. ± (0.30 + 3% of Atten. Setting) Max.			dB dB
Input Power for 0.1 dB Compression	DC - 6 GHz		30		dBm
Input Third Order Intercept Point (Two-Tone Input Power = 10 dBm Each Tone)	DC - 6 GHz		55		dBm
Switching Speed tRise, tFall (10 / 90% RF) rON , tOFF (50% LE to 10 / 90% RF)	DC - 6 GHz		 100 150		 ns ns

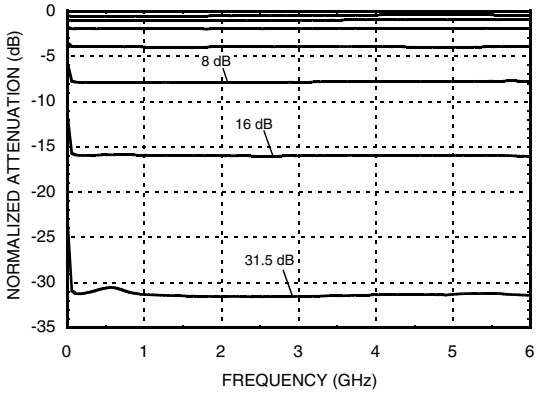
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 6 GHz

Insertion Loss vs. Temperature [1]



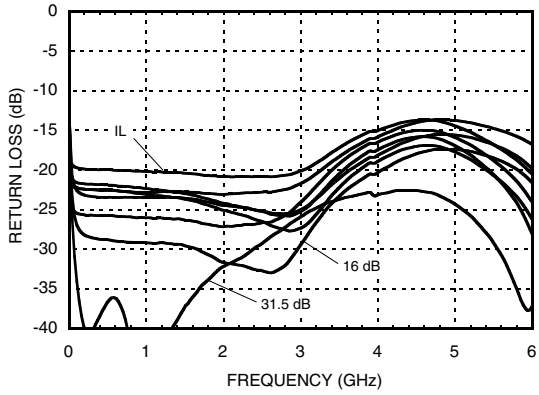
Normalized Attenuation [1]

(Only Major States are Shown)



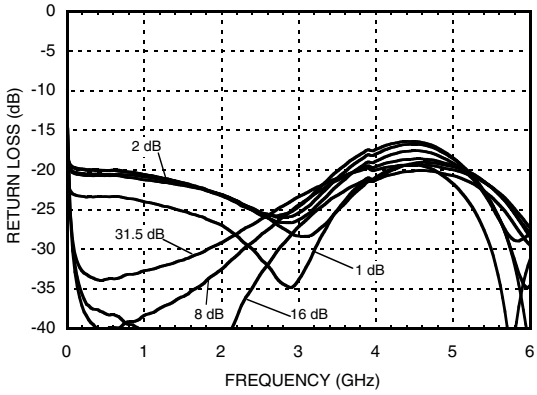
Input Return Loss [1]

(Only Major States are Shown)

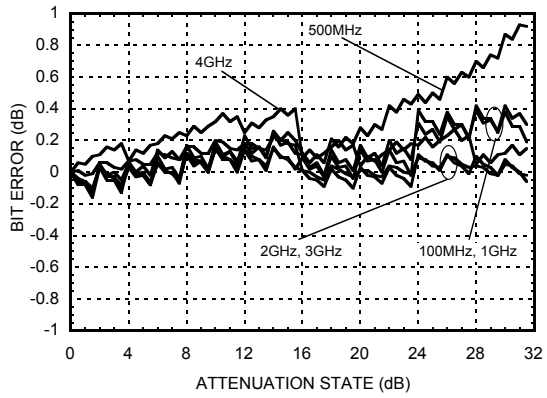


Output Return Loss [1]

(Only Major States are Shown)

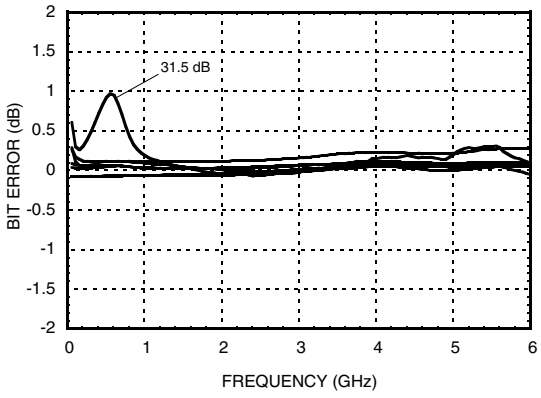


Bit Error vs. Attenuation State [2]



Bit Error vs. Frequency [2]

(Only Major States are Shown)

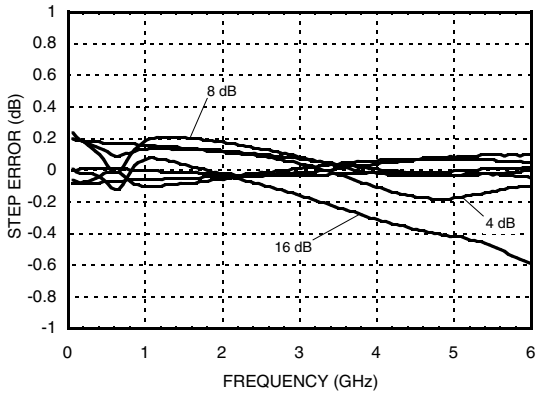


[1] Data taken with bias tees on input and output RF ports. Vdd = +5V & Vctl = 0/+5V.

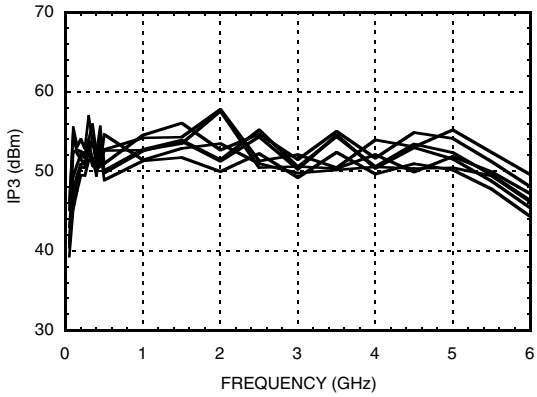
[2] C1, C6 = 330pF. Vdd = +5V & Vctl = 0/+5V.

[3] C1, C6 = 330pF. Vdd = +3V & Vctl = 0/+3V.

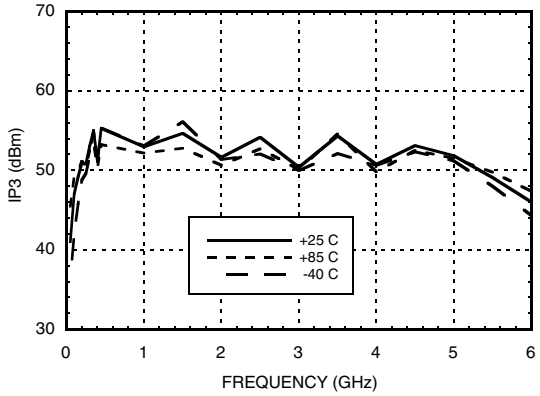
Worst Case Step Error Between Successive Attenuation States [2]



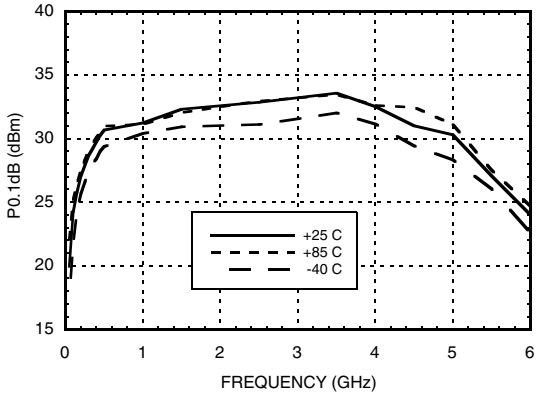
IP3 @ Major Attenuation States [2]



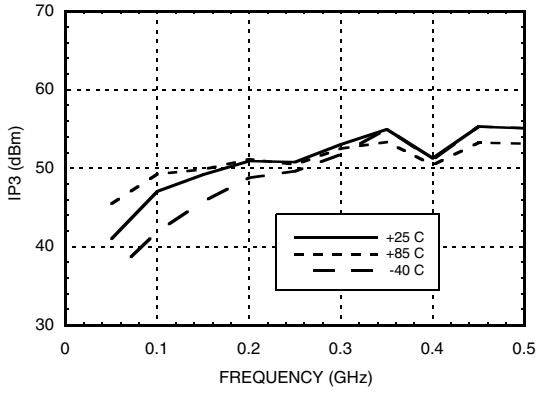
IP3 vs. Temperature, Min. Attn State [2]



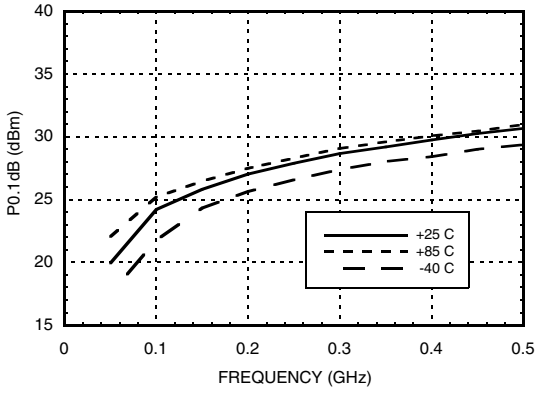
P0.1dB vs. Temperature, Min. Attn State [2]



IP3 vs. Temperature, Min. Attn State [2]
(Low Frequency Detail)

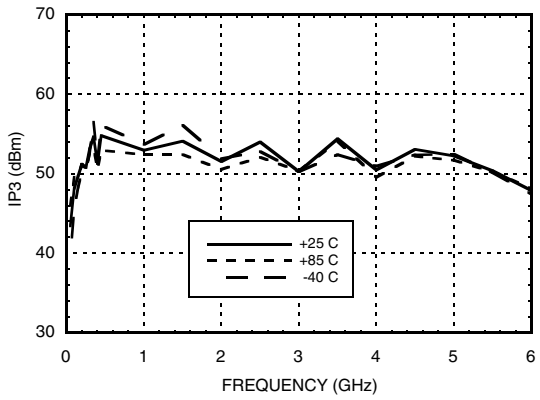


P0.1dB vs. Temperature, Min. Attn State [2]
(Low Frequency Detail)

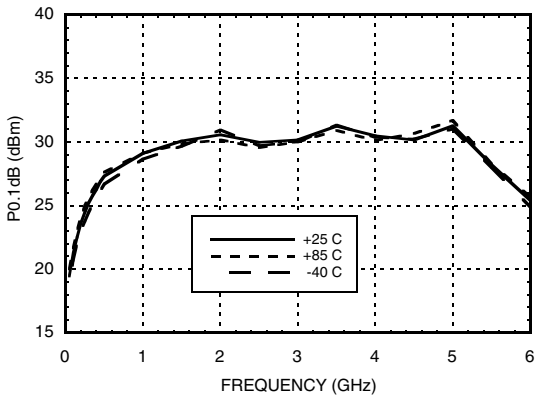


[1] Data taken with bias tees on input and output RF ports. Vdd = +5V & Vctl = 0/+5V.
[2] C1, C6 = 330pF. Vdd = +5V & Vctl = 0/+5V.
[3] C1, C6 = 330pF. Vdd = +3V & Vctl = 0/+3V.

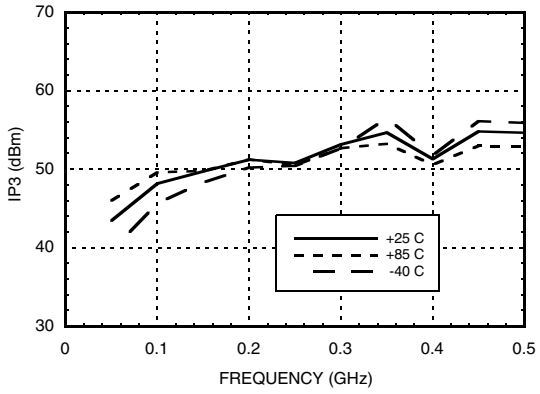
IP3 vs. Temperature, Min. Attn State [3]



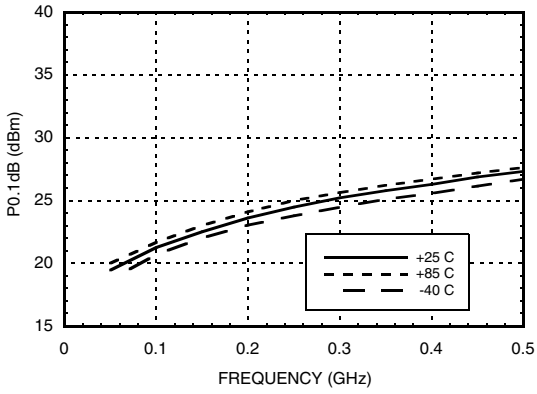
P0.1dB vs. Temperature, Min. Attn State [3]



IP3 vs. Temperature, Min. Attn State [3]
(Low Frequency Detail)



P0.1dB vs. Temperature, Min. Attn State [3]
(Low Frequency Detail)

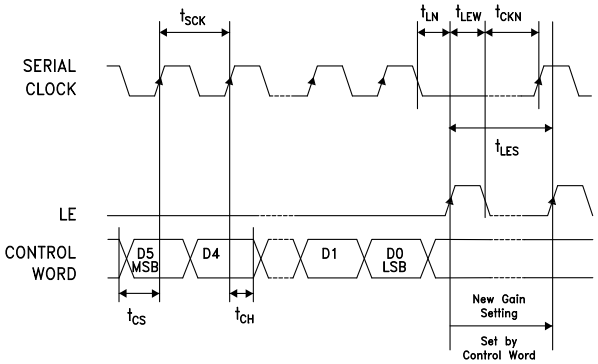


Serial Control Interface

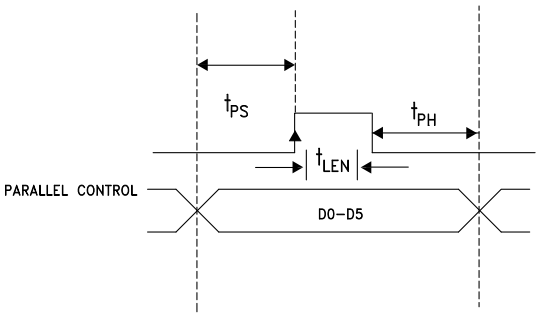
The HMC624LP4E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). The serial control interface is activated when P/S is kept high. The 6-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches are used, sufficient debouncing should be provided. When LE is high, 6-bit data in the serial input register is transferred to the attenuator. When LE is high CLK is masked to prevent data transition during output loading.

When P/S is low, 3-wire SPI interface inputs (SERIN, CLK, LE) are disabled and the input register is loaded with parallel digital inputs (D0-D5). When LE is high, 6-bit parallel data changes the state of the part per truth table.

For all modes of operations, the state will stay constant while LE is kept low.



Timing Diagram (Latched Parallel Mode)



Parameter	Min. [1]	Typ. [1]
Min. serial period, t_{SCK}	70 ns	
Control set-up time, t_{CS}	15 ns	
Control hold-time, t_{CH}		20 ns
LE setup-time, t_{LN}	15 ns	
Min. LE pulse width, t_{LEW}		10 ns
Min LE pulse spacing, t_{LES}		630 ns
Serial clock hold-time from LE, t_{CKN}		10 ns
Hold Time, $t_{PH.}$		0 ns
Latch Enable Minimum Width, t_{LEN}		10 ns
Setup Time, t_{PS}		2 ns

Parallel Mode
(Direct Parallel Mode & Latched Parallel Mode)

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the control voltage inputs D0-D5 directly. The LE (Latch Enable) must be at a logic high at all times to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the control voltage inputs D0-D5 and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram above for reference.

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is set to logic HIGH at power-up, the logic state of D0-D5 determines the power-up state of the part per truth table. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

Bias Voltage

Vdd (V)	Idd (Typ.) (mA)
3	1.8
5	2.0

Control Voltage Table

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.5V @ <1 µA	0 to 0.8V @ <1 µA
High	2 to 3V @ <1 µA	2 to 5V @ <1 µA

[1] Vdd = 5V

PUP Truth Table

LE	PUP1	PUP2	Relative Attenuation
0	0	0	-31.5
0	1	0	-24
0	0	1	-16
0	1	1	Insertion Loss
1	X	X	0 to -31.5 dB

Note: The logic state of D0 - D5 determines the power-up state per truth table shown below when LE is high at power-up.

Truth Table

Control Voltage Input						Reference Insertion Loss
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB
Any combination of the above states will provide an attenuation equal to the sum of the bits selected.						

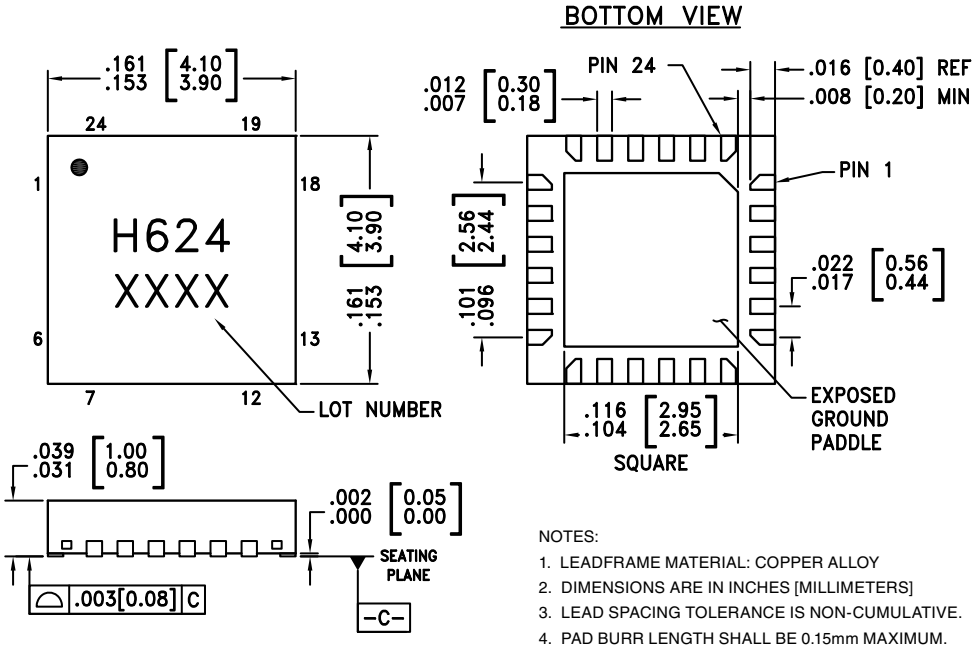
0.5 dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 6 GHz

Absolute Maximum Ratings

RF Input Power (DC - 6 GHz)	28 dBm (T = +85 °C)
Digital Inputs (P/S, CLK, SERIN, LE, PUP1, PUP2, D0-D5)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.6V
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 9.8 mW/°C above 85 °C) [1]	0.635 W
Thermal Resistance	102 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +90 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

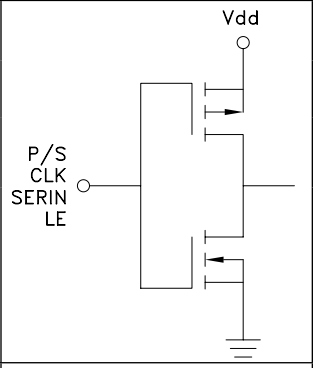
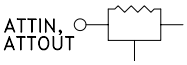
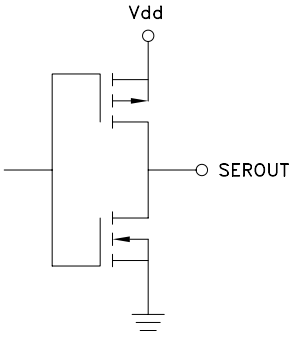
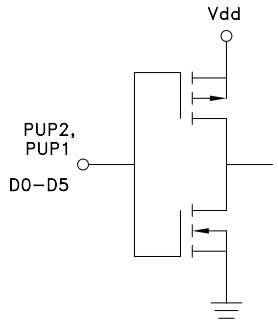
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

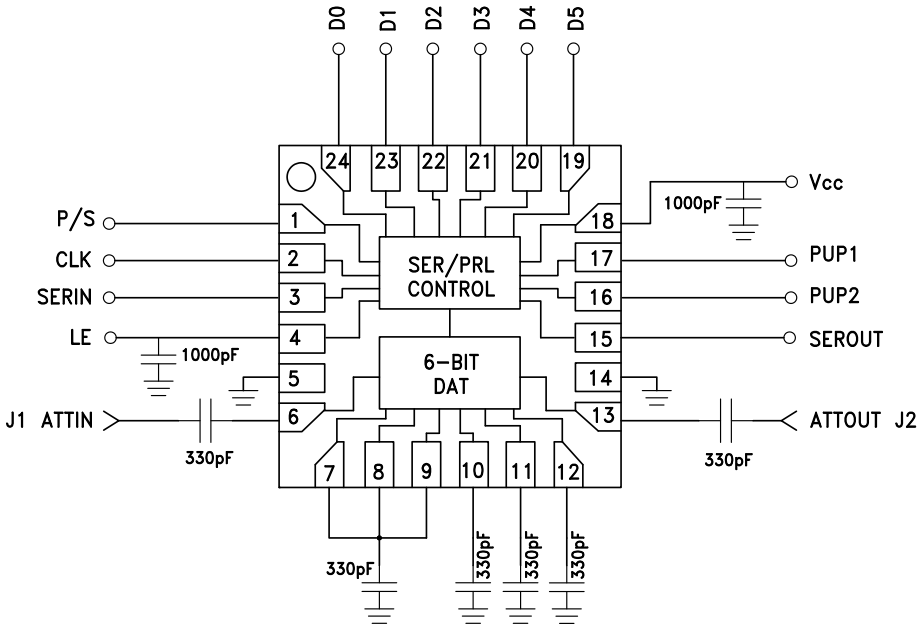
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC624LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H624 XXXX
HMC624LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H624 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

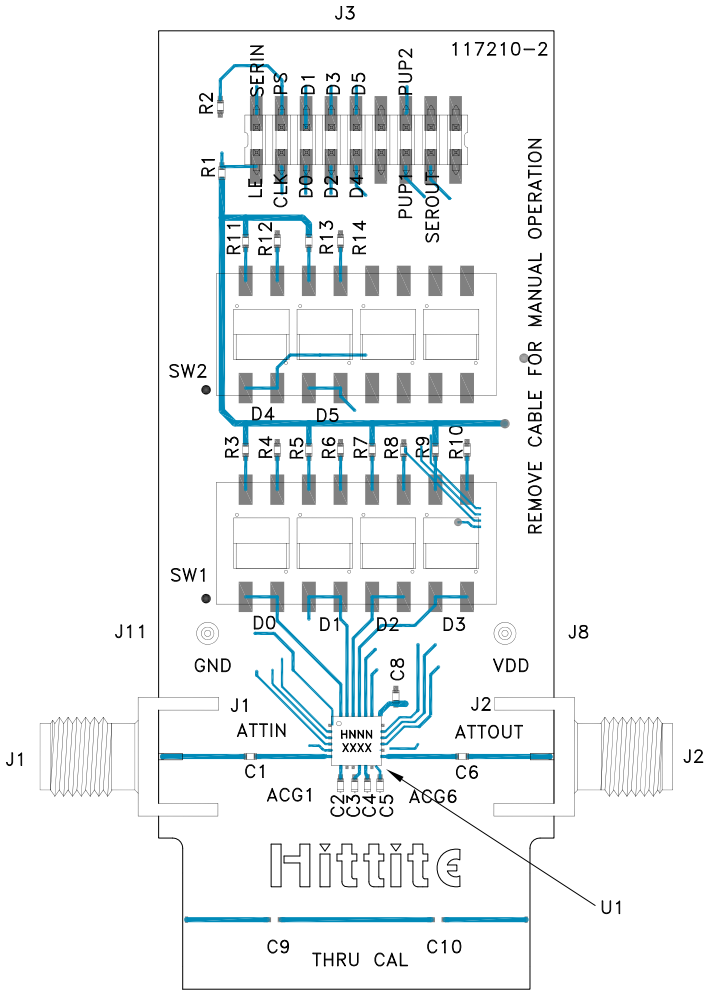
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	P/S	See truth table, control voltage table and timing diagram.	
2	CLK		
3	SERIN		
4	LE		
5, 14	GND	These pins and package bottom must be connected to RF/DC ground.	
6, 13	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
7 - 12	ACG1 - ACG6	External capacitors to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
15	SEROUT	Serial input data delayed by 6 clock cycles.	
16, 17 19 - 24	PUP2, PUP1 D5, D4, D3, D2, D1, D0	See truth table, control voltage table and timing diagram.	
18	Vdd	Supply voltage	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 117212 [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3	18 Pin DC Connector
J8, J11	DC Pin
C1, C6	330 pF Capacitor, 0402 Pkg.
C7, C8	1000 pF Capacitor, 0402 Pkg.
R1 - R14	100 kOhm Resistor, 0402 Pkg.
SW1, SW2	SPDT 4 Position DIP Switch
U1	HMC624LP4(E) Digital Attenuator
PCB [2]	117210 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.