HMC1030LP5E

DUAL RMS POWER DETECTOR DC - 3.9 GHz

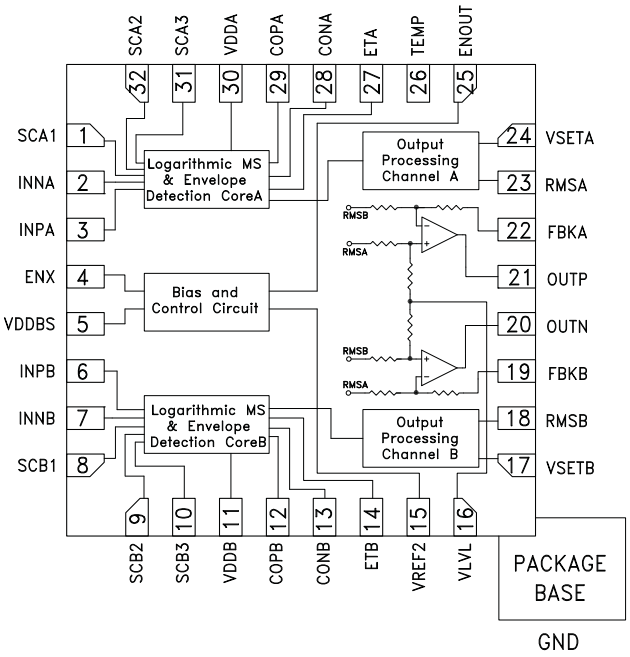
Features

- Crest Factor (Peak-to-Average Power Ratio) Measurement
- Envelope-to-Average Power Ratio Measurement
- Dual channel and channel difference output ports
- Excellent Channel Matching and Channel Isolation
- RF Signal Wave Shape & Crest Factor Independent
- Supports Controller Mode
- ± 1 dB Detection Accuracy to 3.9 GHz
- Input Dynamic Range -55 dBm to +15 dBm
- +5V Operation from -40° C to +85° C
- Excellent Temperature Stability
- Integrated Temperature Sensor
- Power-Down Mode
- 32 Lead 5x5mm SMT Package: 25mm²

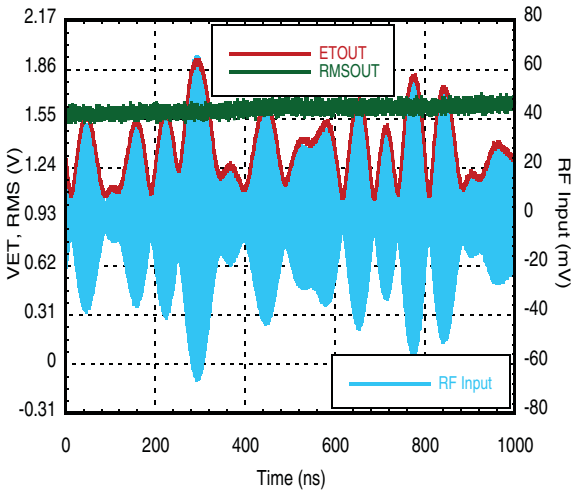
Typical Applications

- Log -> Root - Mean - Square (RMS) Conversion
- Transmitter Power Control
- Receiver Automatic Gain Control
- Antenna VSWR Monitor
- Received Signal Strength Indication (RSSI)
- Transmitter Signal Strength Indication (TSSI)
- Dual Channel wireless infrastructure radio

Functional Diagram



RMS & Envelope Response to WCDMA 4 Carrier with -20dBm RF Input @ 0.9 GHz



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DUAL RMS POWER DETECTOR DC - 3.9 GHz

General Description

The HMC1030LP5E is a dual-channel RMS power detector designed for high accuracy RF power signal measurement and control applications over the 0.1 to 3.9 GHz frequency range. The device can be used with input signals having RMS values from -60 dBm to +10 dBm referenced to 50 Ohm and large crest factors with no accuracy degradation.

Each RMS detection channel is fully specified for operation up to 3.9 GHz, over a wide dynamic range of 70 dB. The HMC1030LP5E operates from a single +5V supply and provides two linear-in-dB detection outputs at the RMSA and RMSB pins with scaled slopes of 37 mV/dB. The RMSA and RMSB channel outputs provide RMS detection performance in terms of dynamic range, logarithmic linearity and temperature stability similar to Hittite's HMC1021LP4E RMS Detector. The RMSA and RMSB outputs provide a read of average input signal power, or true-RMS power. Frequency detection up to 3.9 GHz is possible, with excellent channel matching of less than 1 dB, over a wide range of input frequencies and with low temperature drift.

The HMC1030LP5E also provides "channel difference" output ports via pins OUTP and OUTN, permitting measurements of the input signal power ratio between the two power detection channels. These outputs may be used in single-ended or differential configurations. An input voltage applied to the VLVL input pin is used to set the common mode voltage reference level for OUTP and OUTN. On the Hittite evaluation board, the VLVL pin is shorted to VREF2 output to provide a nominal bias voltage of 2.5V; but any external bias voltage may be used to set VLVL.

The HMC1030LP5E features ETA and ETB pins which provide an accurate voltage output which is linearly proportional to the envelope amplitude of the RF input signal for modulation bandwidths up to 150 MHz. The high bandwidth envelope detection of the HMC1030LP5E makes it ideal for detecting broadband and high crest factor RF signals commonly used in CDMA2000, WCDMA, and LTE systems. Additionally, the instantaneous envelope output can be used to create fast, excessive RF power protection, PA linearization, and efficiency enhancing envelope tracking PA implementations.

The HMC1030LP5E includes a buffered PTAT temperature sensor output with a temperature scaling factor of 2 mV/°C yielding a typical output voltage of 567 mV at 0°C.

The HMC1030LP5E operates over the -40 to +85°C temperature range, and is available in a compact, 32-lead 5x5 mm leadless QFN package.

Electrical Specifications I, T_A = +25°C, VCCA = VCCB = VCCBS = 5V, Sci3 = Sci1 = 0V, Sci2= 5V, Unless Otherwise Noted

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Dynamic Range (± 1 dB measurement error) [1]								
Input Signal Frequency	100	900	1900	2200	2700	3500	3900	MHz
RMSA Output	73	73	71	69	57	48	42	dB
RMSB Output	74	74	72	70	67	50	44	dB
ETA Output		19	20	20	19	19	19	dB
ETB Output		19	20	19	19	19	19	dB
Channel Isolations								
Input Signal Frequency	100	900	1900	2200	2700	3500	3900	MHz
Input A to RMS_B Isolation (PIN_B = -45 dBm, RMS_B = $RMSB_{INB}$ ±1 dB)	> 55	> 55	52	49	49			dB
Input B to RMS_A Isolation (PIN_A = -45 dBm, RMS_A = $RMSA_{INA}$ ±1 dB)	> 55	> 55	50	46	45			dB
Input A to RMS_B Isolation (PIN_B = -40 dBm, RMS_B = $RMSB_{INB}$ ±1 dB)						44	39	dB
Input B to RMS_A Isolation (PIN_A= -40 dBm, RMS_A=$RMSA_{INA}$ ±1 dB)						47	41	dB
Deviation vs Temperature: (Over full temperature range -40°C to 85°C). Deviation is measured from reference, which is the same WCDMA input at 25 °C						1		dB
Channel Mismatch						<1		dB

[1] With WCDMA 4 Carrier (TM1-64 DPCH)

Electrical Specifications II, T_A = +25 °C, VCCA = VCCB = VCCBS = 5V, Sci3= Sci1 = 0V, Sci2 = 5V, Unless Otherwise Noted

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Signal Frequency	100	900	1900	2200	2700	3500	3900	MHz
Modulation Deviation (Output deviation from reference, which is measured with CW input at equivalent input signal power)								
WCDMA 4 Carrier (TM1-64 DPCH) at +25 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	dB
WCDMA 4 Carrier (TM1-64 DPCH) at +85 °C	0.2	0.2	0.2	0.2	0.2	0.2	0.2	dB
WCDMA 4 Carrier (TM1-64 DPCH) at -40 °C	0.2	0.2	0.2	0.2	0.2	0.2	0.2	dB
RMSA Logarithmic Slope and Intercept [1]								
Logarithmic Slope	35.5	38.5	37.3	38.2	40.3	45.8	49.9	mV/dB
Logarithmic Intercept	-66.4	-65.8	-63.4	-62	-58.9	-53	-49.5	dBm
Max. Input Power at ±1 dB Error	10	10	10	10	1	-3	-5	dBm
Min. Input Power at ±1 dB Error	-62	-62	-60	-58	-56	-51	-47	dBm
RMSB Logarithmic Slope and Intercept [1]								
Logarithmic Slope	34.7	34.9	36.2	37	38.8	43.6	47.2	mV/dB
Logarithmic Intercept	-67.5	-67	-65	-63.5	-60.7	-55.2	-51.7	dBm
Max. Input Power at ±1 dB Error	10	10	10	10	9	-3	-5	dBm
Min. Input Power at ±1 dB Error	-64	-64	-62	-61	-58	-53	-49	dBm
ETA Linear Slope and Intercept								
Linear Slope		14.3	12.3	11.8	10.5	9.1	8.4	V/V
Linear Intercept		-65.5	-75.8	-79	-88.2	-102.6	-111.32	mV
Max. Input Power at ±1 dB Error		-12	-10	-9	-9	-8	-8	dBm
Min. Input Power at ±1 dB Error		-31	-30	-29	-28	-27	-27	dBm
ETB Linear Slope and Intercept								
Linear Slope		14.5	12.6	12.2	11.1	9.7	8.9	V/V
Linear Intercept		-64.1	-73.7	-76.1	-82.9	-95.1	-103.7	mV
Max. Input Power at ±1 dB Error		-12	-10	-10	-9	-8	-8	dBm
Min. Input Power at ±1 dB Error		-31	-30	-29	-28	-27	-27	dBm

[1] With WCDMA 4 Carrier (TM1-64 DPCH)

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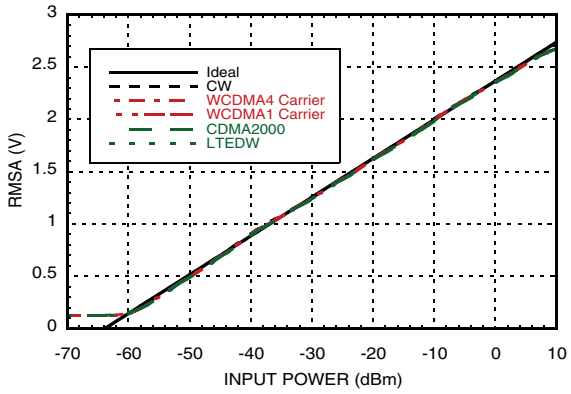
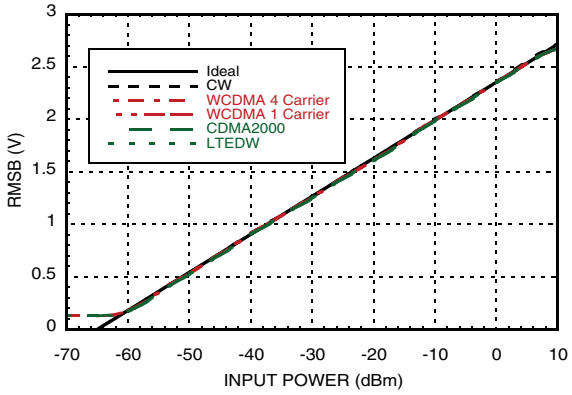
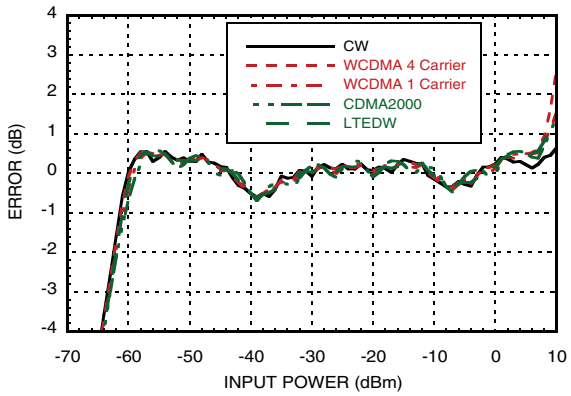
RMSA vs. Pin with Different Modulations @ 1900 MHz[1]



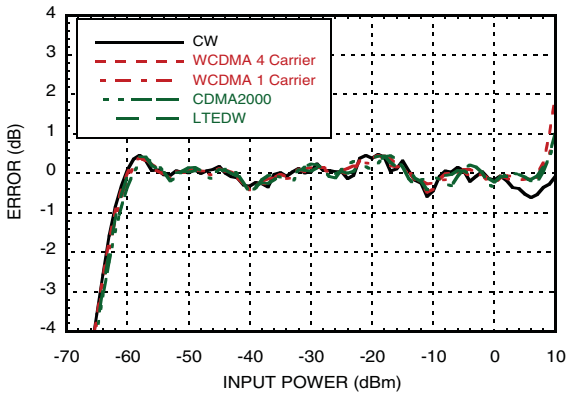
RMSB vs. Pin with Different Modulations @ 1900 MHz[1]



RMSA Error vs. Pin with Different Modulations @ 1900 MHz[1]



RMSB Error vs. Pin with Different Modulations @ 1900 MHz[1]



Electrical Specifications III,

T_A = +25 °C, VCCA = VCCB = VCCBS = 5V, Sci3 = Sci1 = 0V, Sci2 = 5V, Unless Otherwise Noted

Parameter	Conditions	Min.	Typ.	Max.	Units
Single-Ended Input Configuration					
Input Network Return Loss	up to 4 GHz		> 15		dB
Input Resistance between INP_A and INN_A	Between pins 2 and 3		110		Ohm
Input Resistance between INP_B and INN_B	Between pins 6 and 7		110		Ohm
Input Voltage Range	$V_{DIFFINA} = V_{INPA} - V_{INNA}$ and $V_{DIFFINB} = V_{INPB}-V_{INNB}$			2.25	V
RMS [A,B] Output					
Output Voltage Range			0.1 to 3		V
Open-loop Output Voltage Range	RMS-VSET disconnected for control applications		0.4 to Vcc-1		V
Source/Sink Current Compliance	Measured with 0.9GHz input RF signal at -25 dBm power		8/1.98		mA
Output Slew Rate (rise/fall)	Sci3=Sci2=Sci1=0V, Cofs=1nF		33 / 1.5		10^6 V/sec

[1] SCA1=SCA3=SCB1=SCB3=0V, SCA2=SCB2=5V

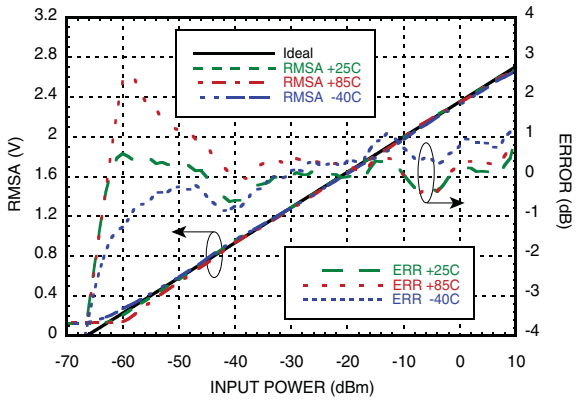
Electrical Specifications III (continued),

T_A = +25 °C, VCCA = VCCB = VCCBS = 5V, Sci3 = Sci1 = 0V, Sci2 = 5V, Unless Otherwise Noted

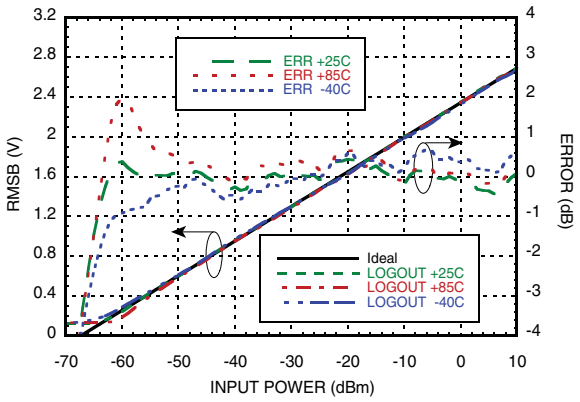
Parameter	Conditions	Min.	Typ.	Max.	Units
ET [A, B] Outputs					
Modulation Bandwidth			100		MHz
Output Voltage Range			1 to 2.1		V
Source/Sink Current Compliance	Measured with 0.9 GHz input RF signal at -18 dBm power		8 / 2.95		mA
Output Slew Rate (rise/fall)			83.3 / 250		10^6 V/sec
V_{SET} [A,B] Outputs					
Input Voltage Range [1]	For control applications with nominal slope/intercept settings		0.13 to 2.7		V
Input Resistance			1		kOhm
OUTP and OUTN Outputs					
Output Voltage Range	R_L=1k Ohm, C_L=4.7pF [1]		1 to 3.9		V
Open-loop Output Voltage Range	OUTP-FBKA and OUTN-FBKB disconnected for control applications		0.1 to Vcc-0.9		V
Source/Sink Current Compliance	Measured with 0.9 GHz input RF signal at -30 dBm power		8 / 2.2		mA
V_{LVL}, Common Mode Reference Level for OUT[P,N]					
Voltage Range	OUT[P,N]=FBK[A,B]	0		5	V
Input Resistance			6		kOhm
V_{REF2}, Voltage Reference Output					
Output Voltage			2.43		V
Temperature Sensitivity			0.15		mV/°C
Source/Sink Current Compliance			5.5 / 2.6		mA
TEMP, Temperature Sensor Output					
Output Voltage	measured at 0°C		0.6		V
Temperature Sensitivity			2.2		mV/°C
Source/Sink Current Compliance			1.7 / 0.5		mA
SCI1-3 Inputs, ENX Logic Input, Power Down Control					
Input High Voltage		$0.7xV_{CC}$			V
Input Low Voltage				$0.3xV_{CC}$	V
Input Capacitance			0.5		pF
Power Supply					
Supply Voltage		4.5	5	5.5	V
Supply Current with no input power	120.6 mA nominal at -40°C; 159.5 mA nominal at 85°C		143		mA
Supply Current with 0 dBm at one channel	128 mA nominal at -40°C; 168.2 mA nominal at 85°C		151.7		mA
Supply Current with 0 dBm at both channels			160		mA
Standby Mode Supply Current			13		mA

[1] For nominal slope/intercept setting, please see application section to change this range

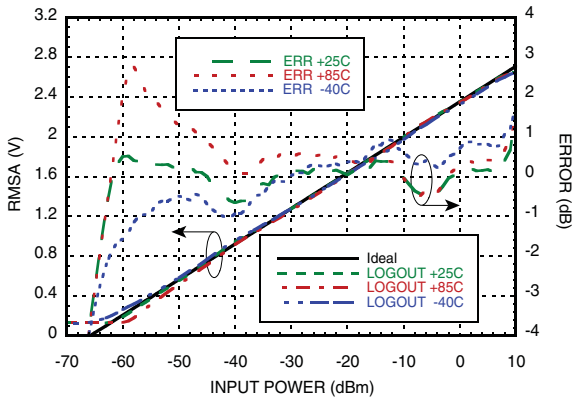
RMSA & Error vs. Pin @ 100 MHz [1]



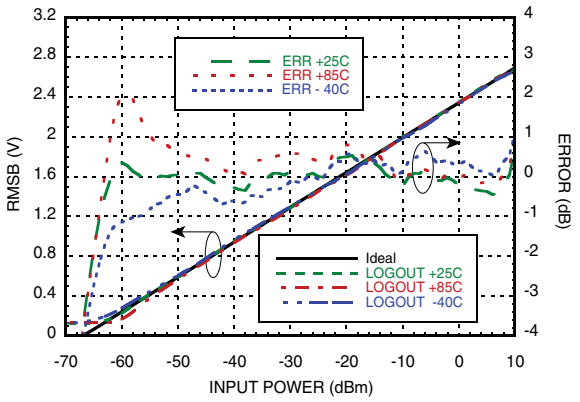
RMSB & Error vs. Pin @ 100 MHz [1]



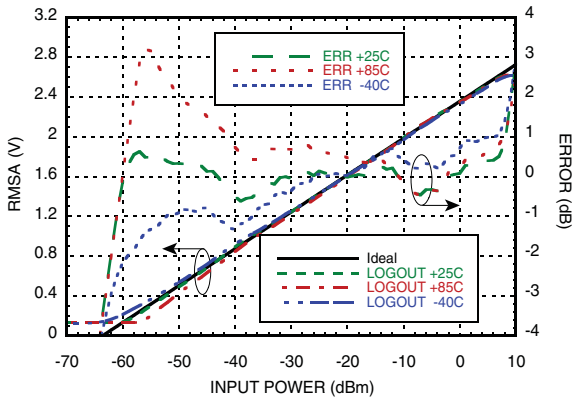
RMSA & Error vs. Pin @ 900 MHz [1]



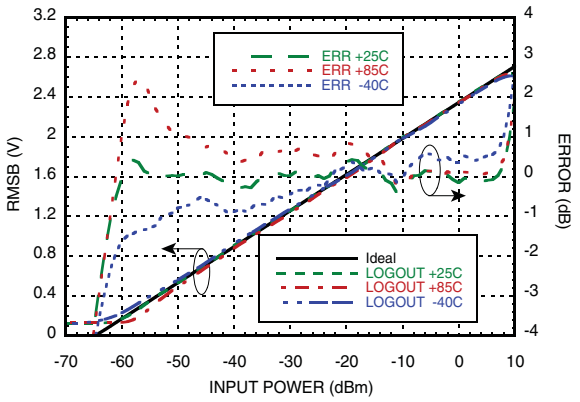
RMSB & Error vs. Pin @ 900 MHz [1]



RMSA & Error vs. Pin @ 1900 MHz [1]

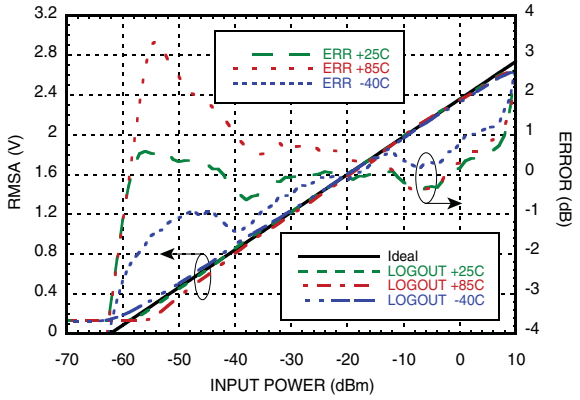


RMSB & Error vs. Pin @ 1900 MHz [1]

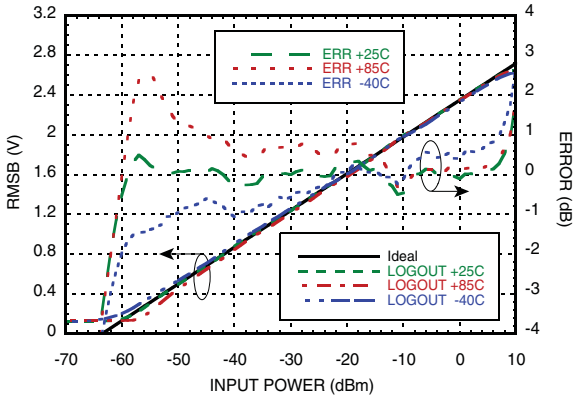


[1] WCDMA Input Waveform

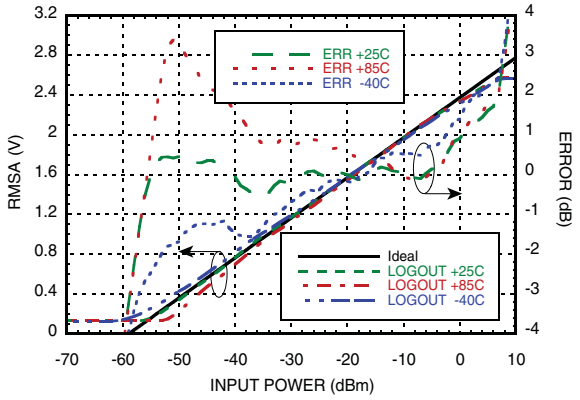
RMSA & Error vs. Pin @ 2200 MHz [1]



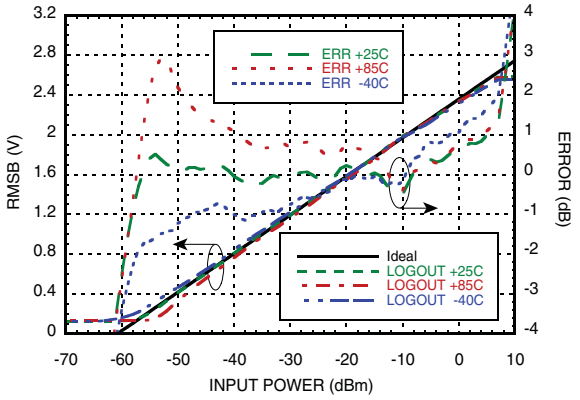
RMSB & Error vs. Pin @ 2200 MHz [1]



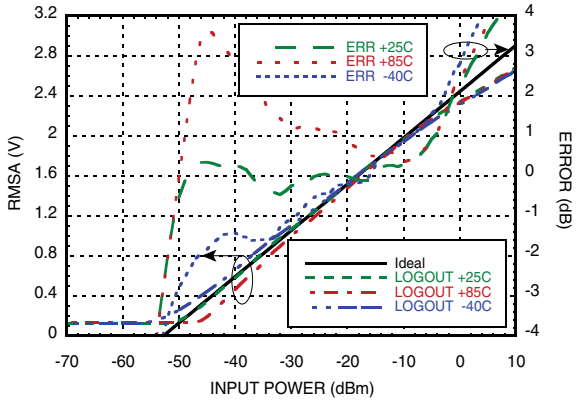
RMSA & Error vs. Pin @ 2700 MHz [1]



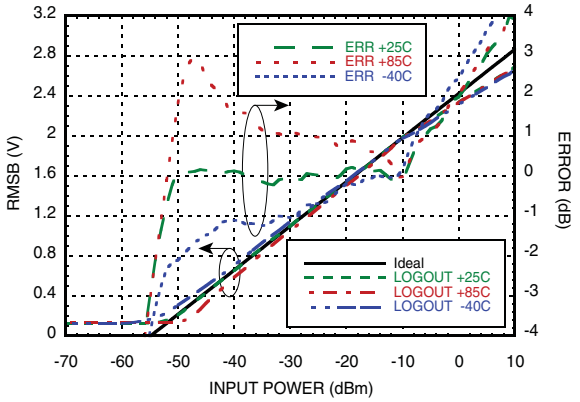
RMSB & Error vs. Pin @ 2700 MHz [1]



RMSA & Error vs. Pin @ 3500 MHz [1]



RMSB & Error vs. Pin @ 3500 MHz [1]



[1] WCDMA Input Waveform

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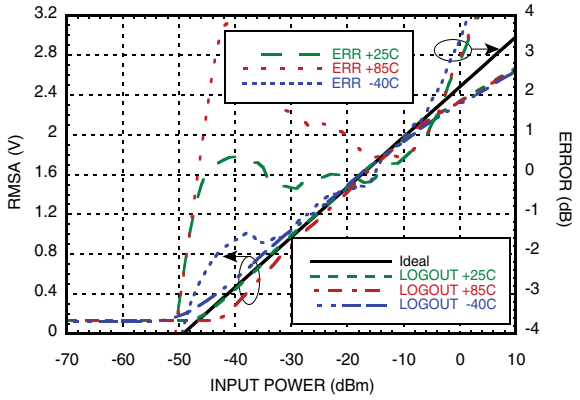
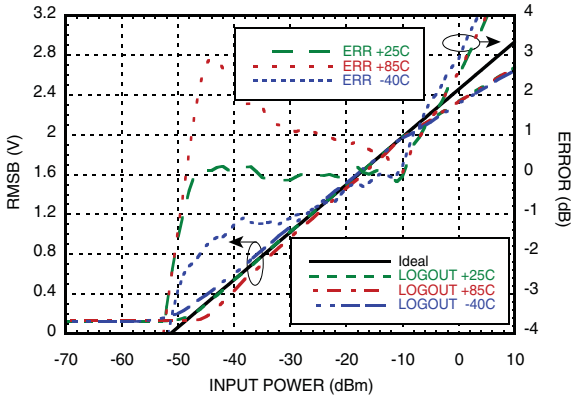
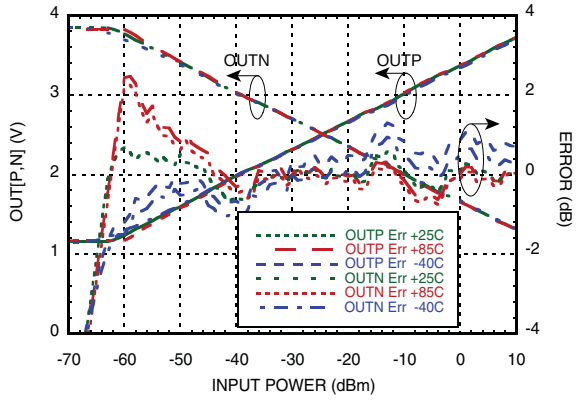
RMSA & Error vs. Pin @ 3900 MHz [1]



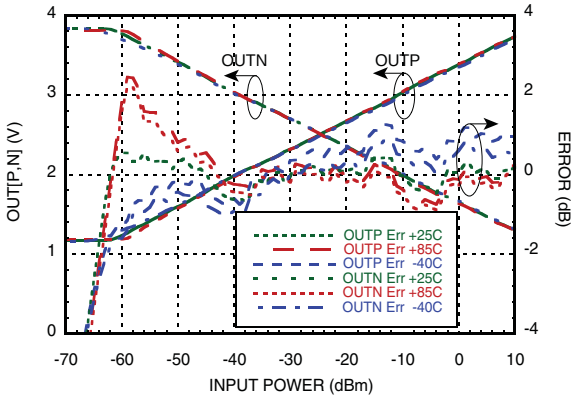
RMSB & Error vs. Pin @ 3900 MHz [1]



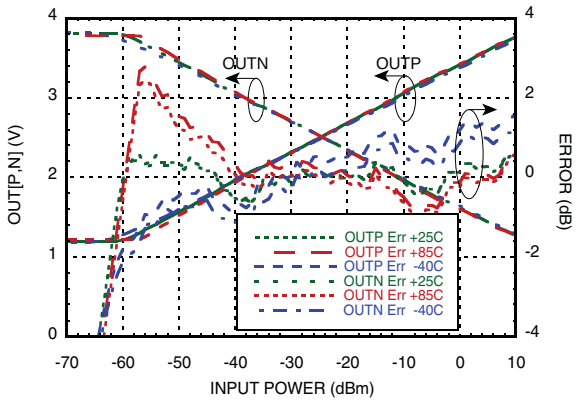
OUT [P,N] & Error vs. Pin @ 100 MHz [1] [2]



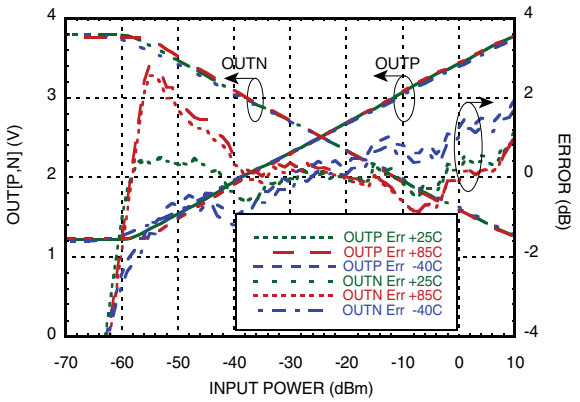
OUT [P,N] & Error vs. Pin @ 900 MHz [1] [2]



OUT [P,N] & Error vs. Pin @ 1900 MHz [1][2]



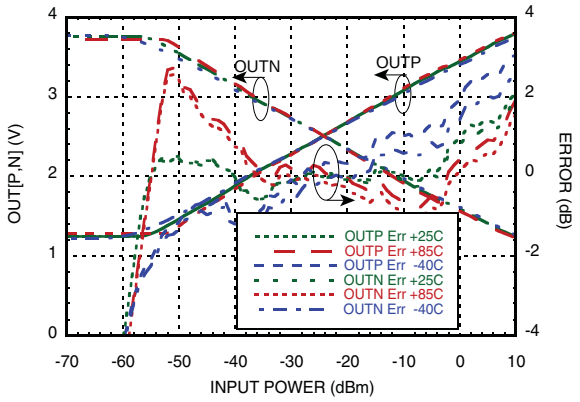
OUT [P,N] & Error vs. Pin @ 2200 MHz [1][2]



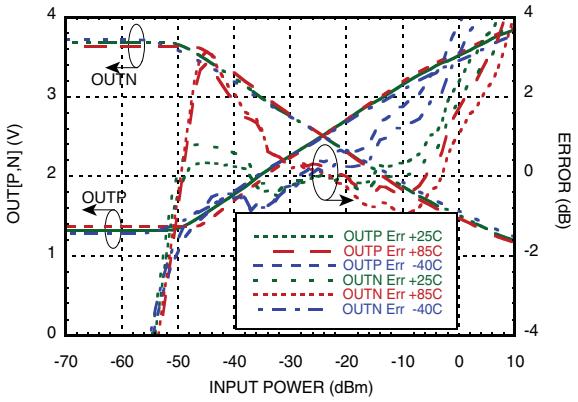
[1] WCDMA Input Waveform

[2] INPA Power Swept, INPB Fixed Power @ -25 dBm

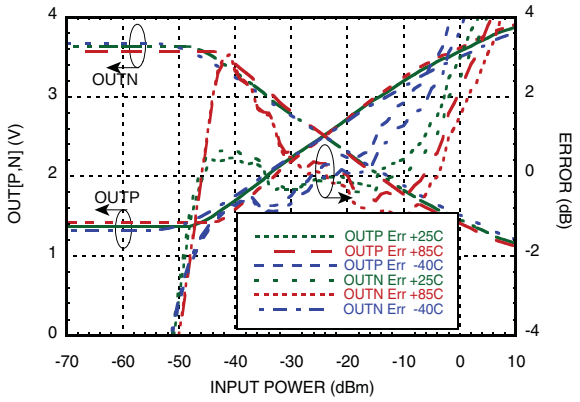
OUT [P,N] & Error vs. Pin @ 2700 MHz [1][2]



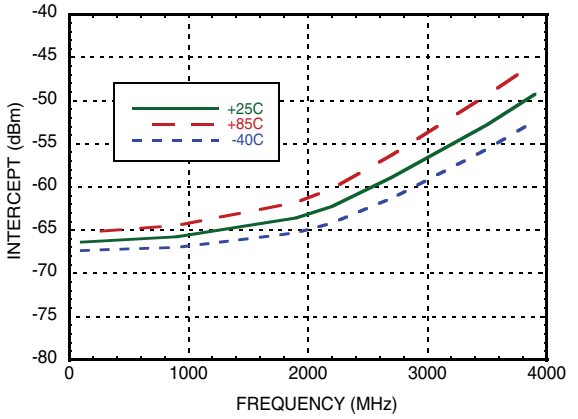
OUT [P,N] & Error vs. Pin @ 3500 MHz[1][2]



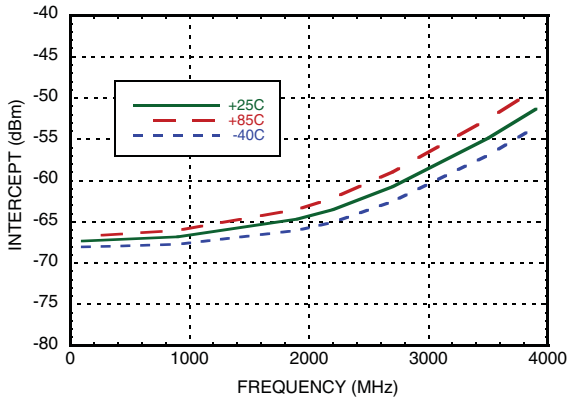
OUT [P,N] & Error vs. Pin @ 3900 MHz [1][2]



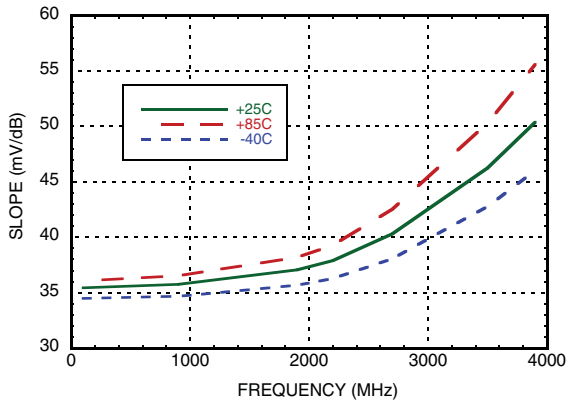
RMSA Intercept vs. Frequency [1]



RMSB Intercept vs. Frequency [1]



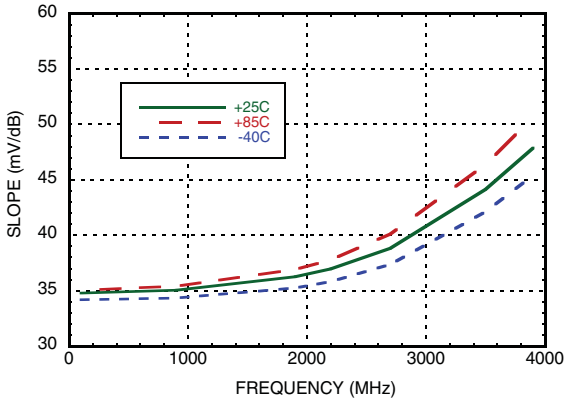
RMSA Slope vs. Frequency [1]



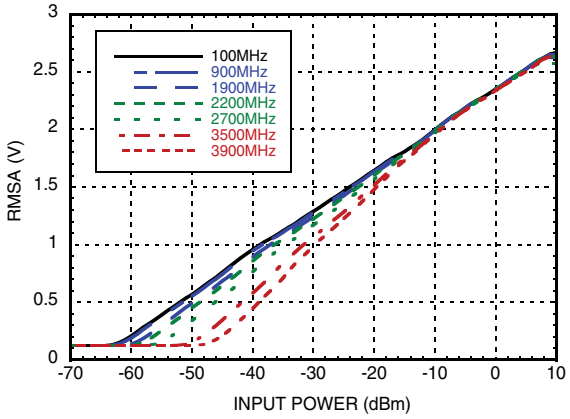
[1] WCDMA Input Waveform

[2] INPA Power Swept, INPB Fixed Power @ -25 dBm

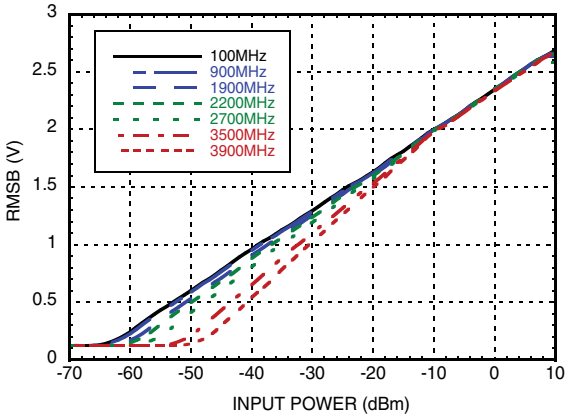
RMSB Slope vs. Frequency [1]



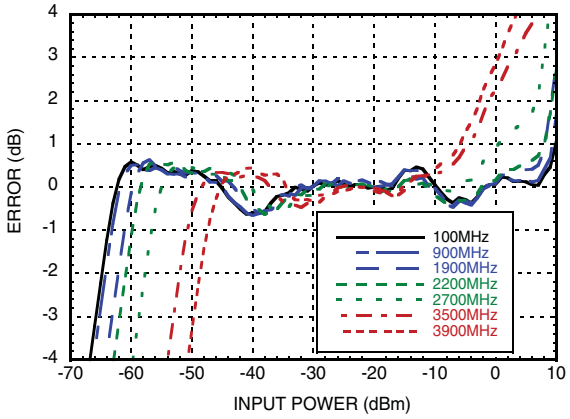
RMSA vs. Pin with WCDMA 4 Carrier @ +25°C [1] [2]



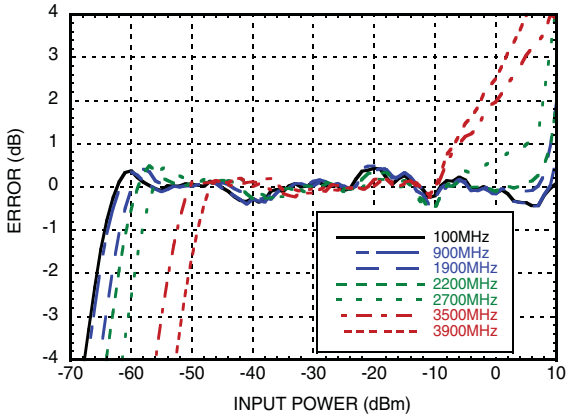
RMSB vs. Pin with WCDMA 4 Carrier @ +25°C [1] [2]



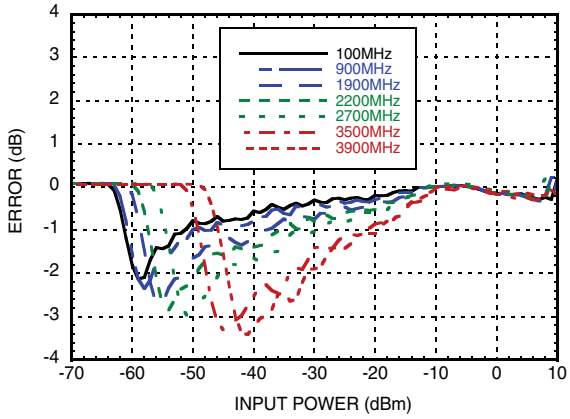
RMSA Error vs. Pin with WCDMA 4 Carrier @ +25°C [1] [2]



RMSB Error vs. Pin with WCDMA 4 Carrier @ +25°C [1] [2]



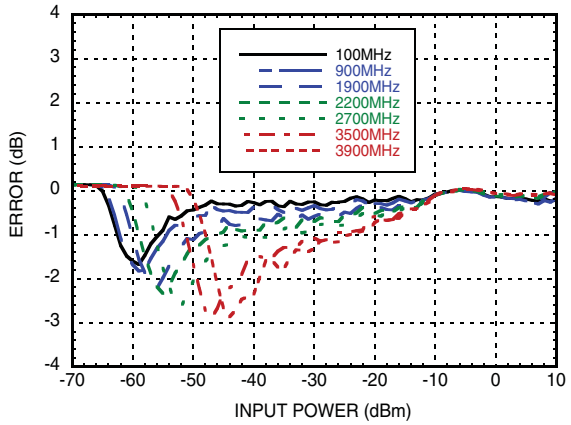
RMSA Error vs. Pin with WCDMA 4 Carrier @ +85°C wrt +25°C Response [1] [2]



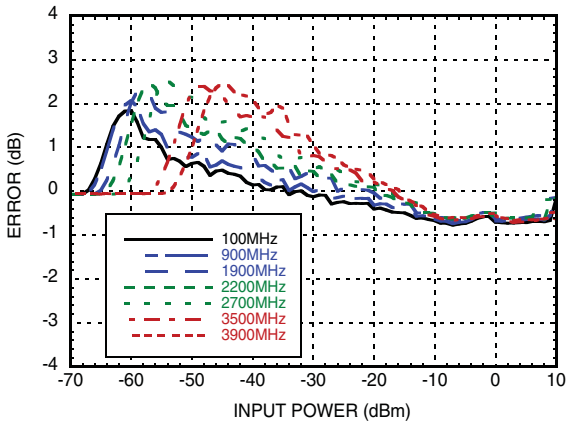
[1] WCDMA Input Waveform

[2] SCA1=SCA3=SCB1=SCB3=0V, SCA2=SCB2=5V

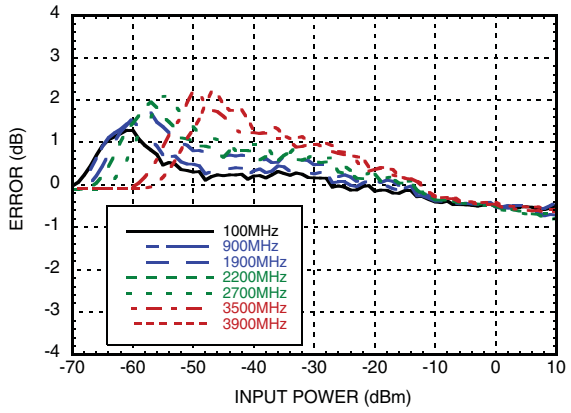
RMSB Error vs. Pin with WCDMA 4 Carrier @ +85°C wrt +25°C Response [1] [2]



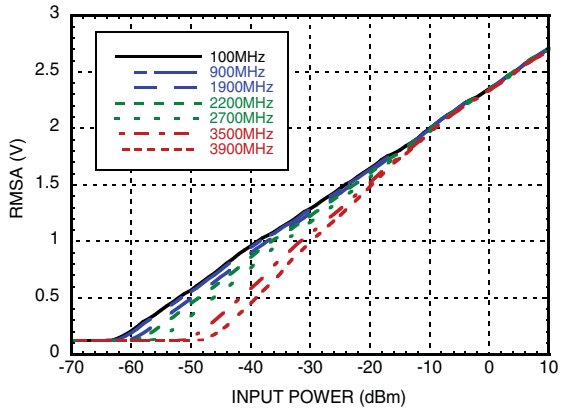
RMSA Error vs. Pin with WCDMA 4 Carrier @ -40°C wrt +25°C Response [1] [2]



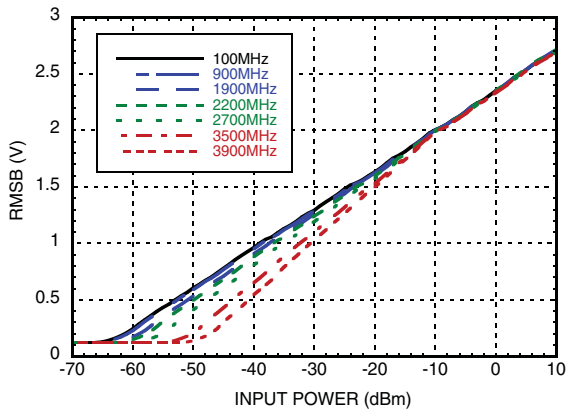
RMSB Error vs. Pin with WCDMA 4 Carrier @ -40°C wrt +25°C Response [1] [2]



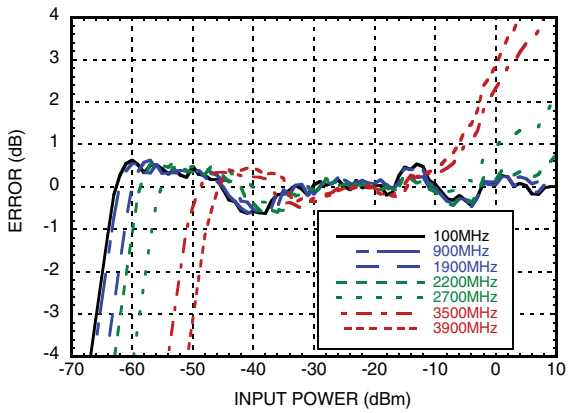
RMSA vs. Pin with CW @ +25°C [1] [2]



RMSB vs. Pin with CW @ +25°C [1] [2]



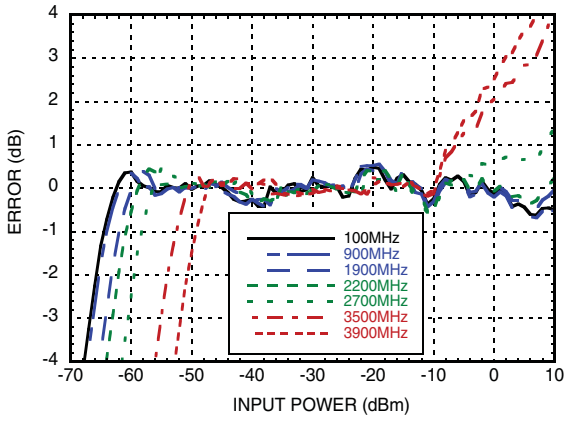
RMSA Error vs. Pin with CW @ +25°C [1] [2]



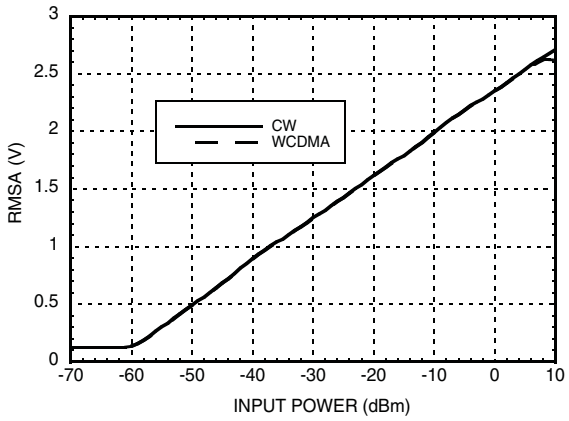
[1] WCDMA Input Waveform

[2] SCA1=SCA3=SCB1=SCB3=0V, SCA2=SCB2=5V

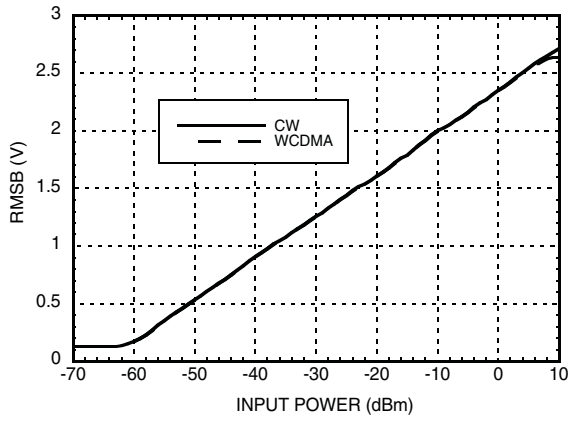
RMSB Error vs. Pin with CW @ +25°C [1] [2]



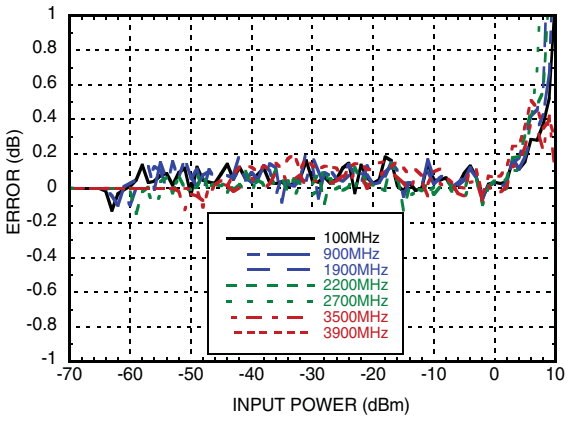
RMSA vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & +25°C [1] [2]



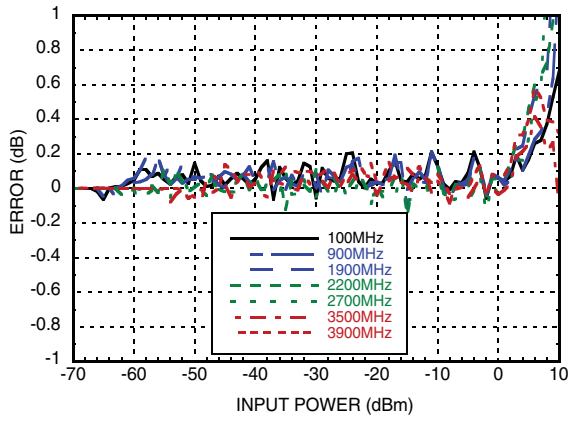
RMSB vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & +25°C [1] [2]



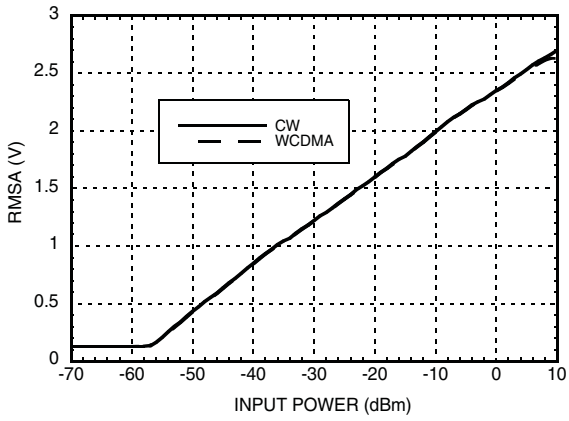
RMSA Reading Error for WCDMA wrt CW Response @ +25°C [1] [2]



RMSB Reading Error for WCDMA wrt CW Response @ +25°C [1] [2]



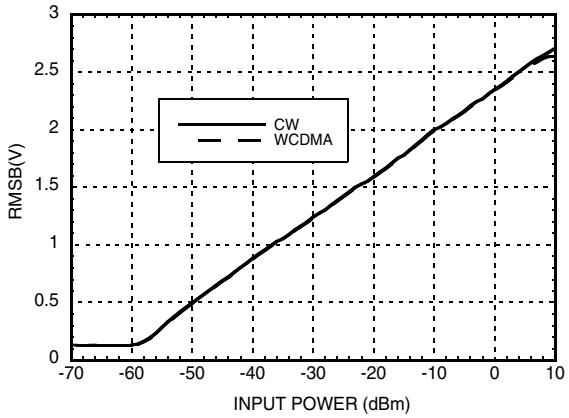
RMSA vs. Pin w/ CW & WCDMA 4 Carrier @ 1900MHz & +85°C [1] [2]



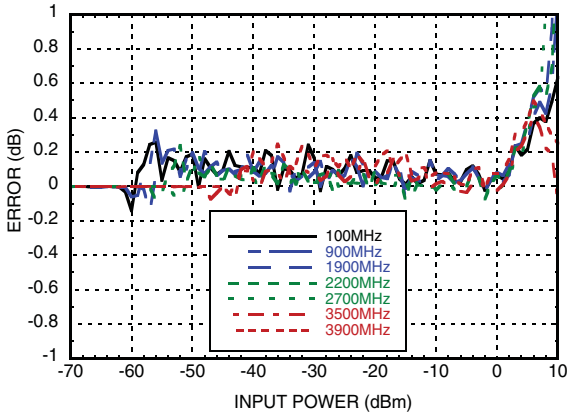
[1] WCDMA Input Waveform

[2] SCA1=SCA3=SCB1=SCB3=0V, SCA2=SCB2=5V

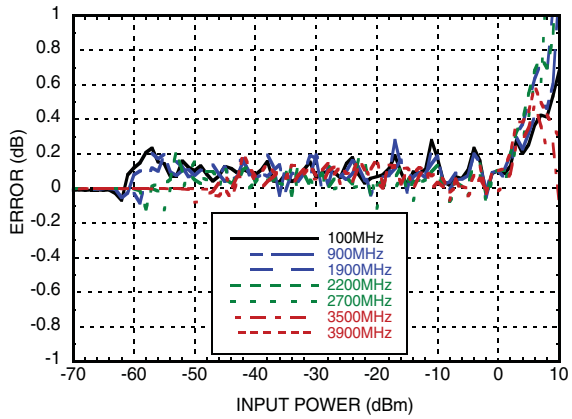
RMSB vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & +85°C [1] [2]



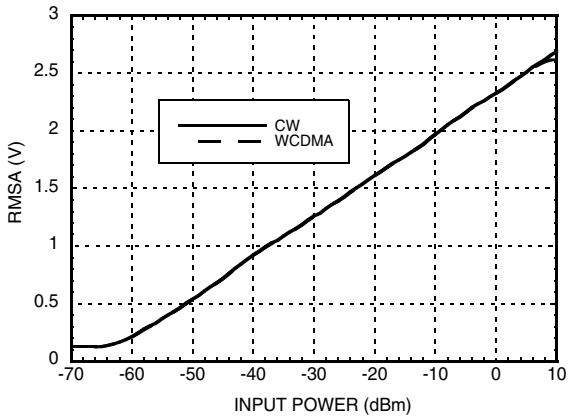
RMSA Reading Error for WCDMA wrt CW Response @ +85°C [1] [2]



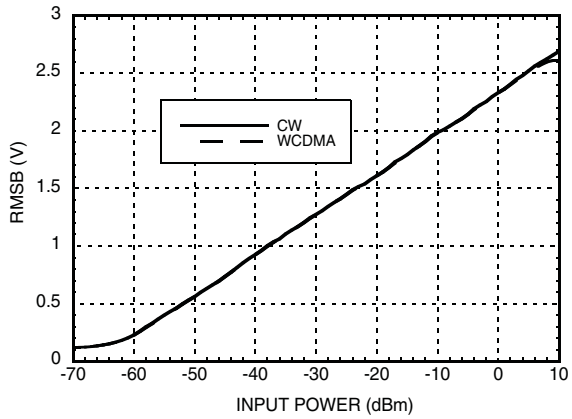
RMSB Reading Error for WCDMA wrt CW Response @ +85°C [1] [2]



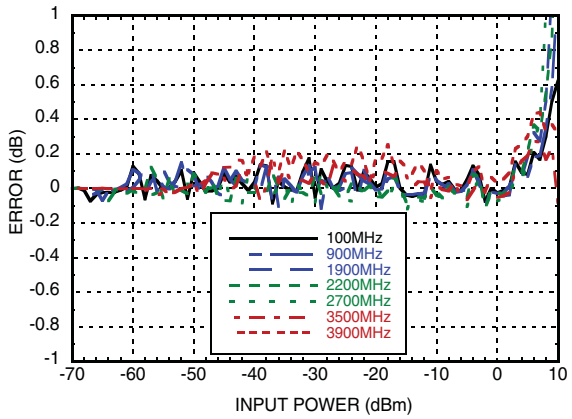
RMSA vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & -40°C [1] [2]



RMSB vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & -40°C [1] [2]



RMSA Reading Error for WCDMA wrt CW Response @ -40°C [1] [2]



[1] WCDMA Input Waveform

[2] SCA1=SCA3=SCB1=SCB3=0V, SCA2=SCB2=5V

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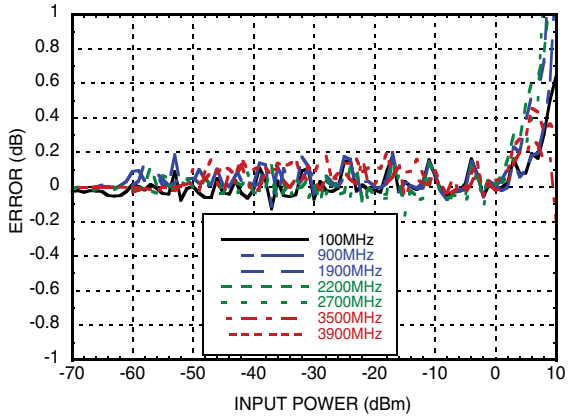
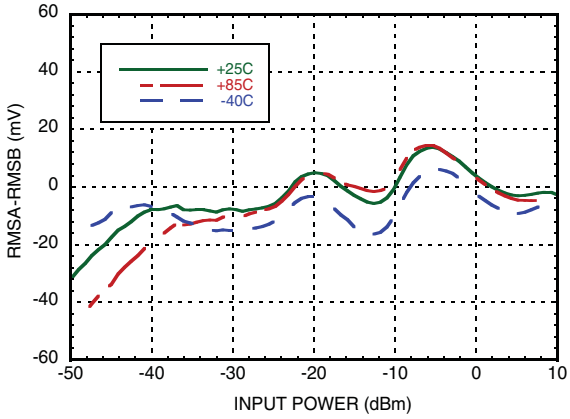
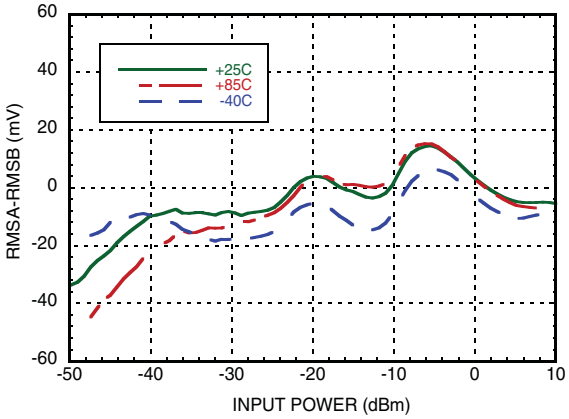
RMSB Reading Error for WCDMA wrt CW Response @ -40°C [1] [2]



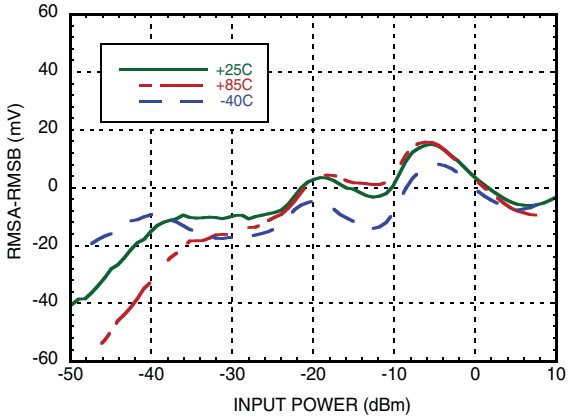
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 100 MHz [2] [3]



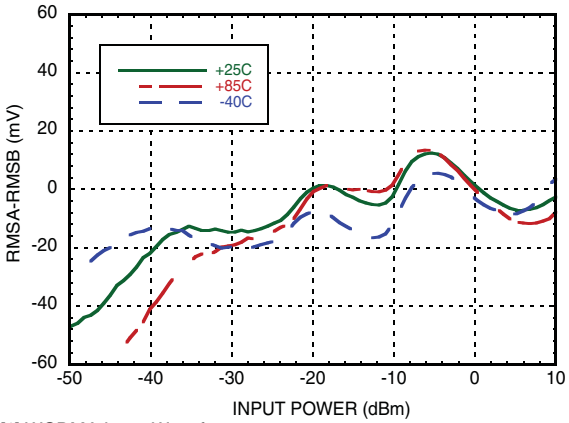
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 900 MHz [2] [3]



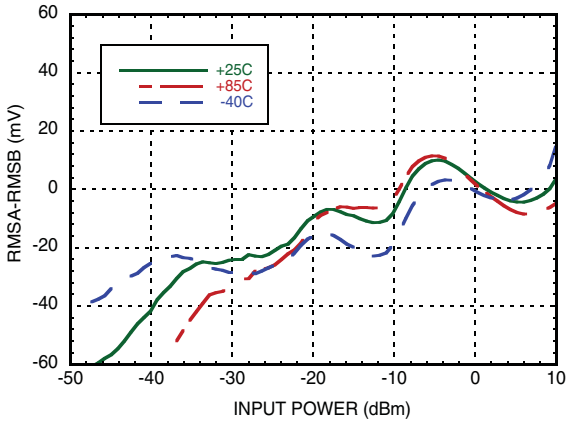
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 1900 MHz [2] [3]



RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 2200 MHz [2] [3]



RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 2700 MHz [2] [3]

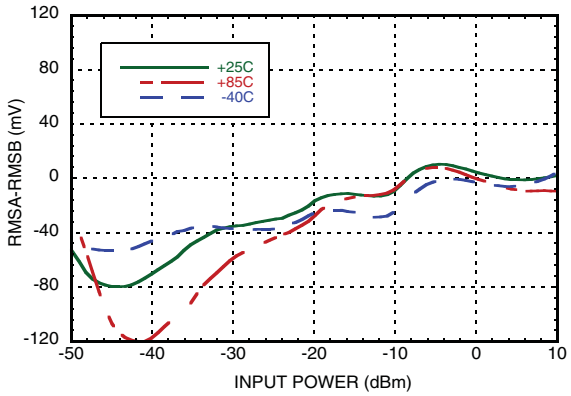


[1] WCDMA Input Waveform

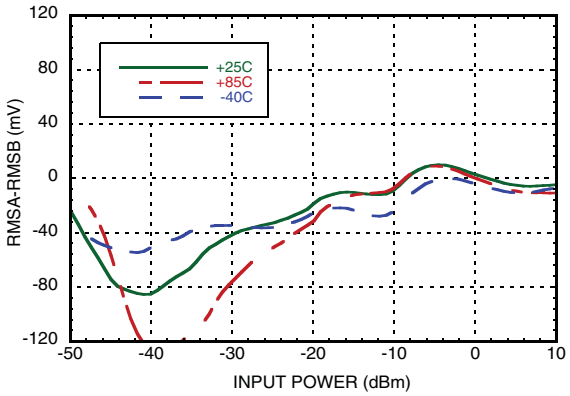
[2] SCA1=SCA3=SCB1=SCB3=0V, SCA2=SCB2=5V

[3] CW Input Waveform, RMSA Referenced

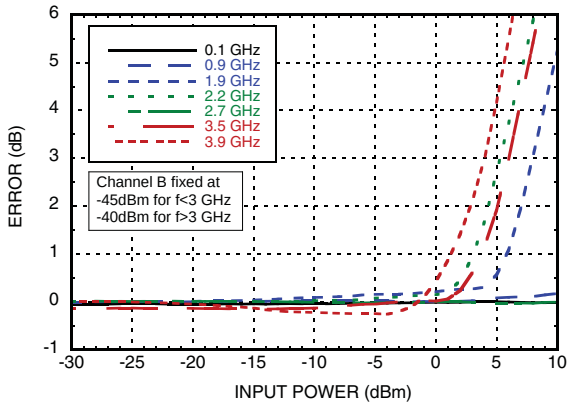
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 3500 MHz [1] [2]



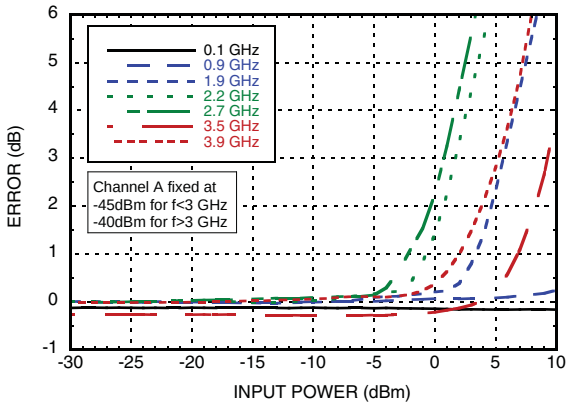
RMSA-RMSB, Channel Matching vs. Pin over Temperature @ 3900 MHz [1] [2]



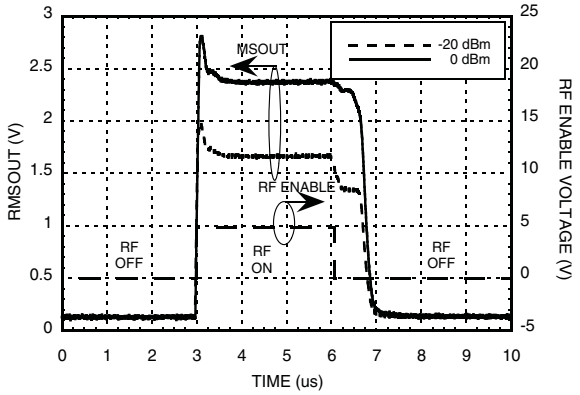
Interference to an Input Signal (INB Power Fixed) with Interfering Signal on the other Channel (INA Power Swept) [1]



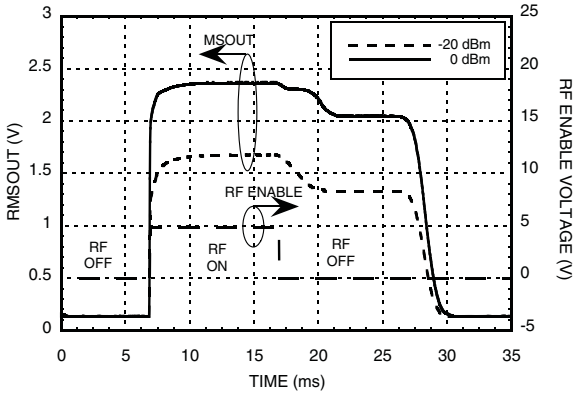
Interference to an Input Signal (INA Power Fixed) with Interfering Signal on the other Channel (INB Power Swept) [1]



RMS [A, B] Output Response with SCI = 000 @ 1900 MHz



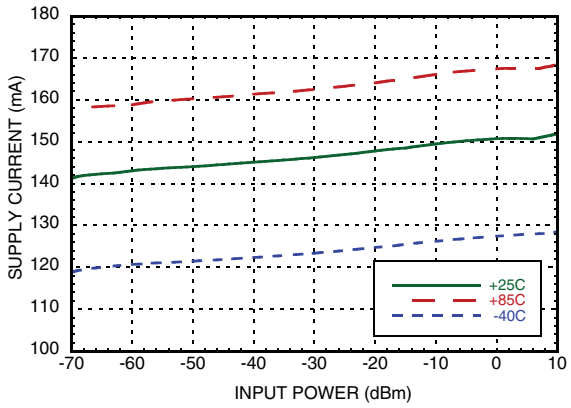
RMS [A, B] Output Response with SCI = 111 @ 1900 MHz



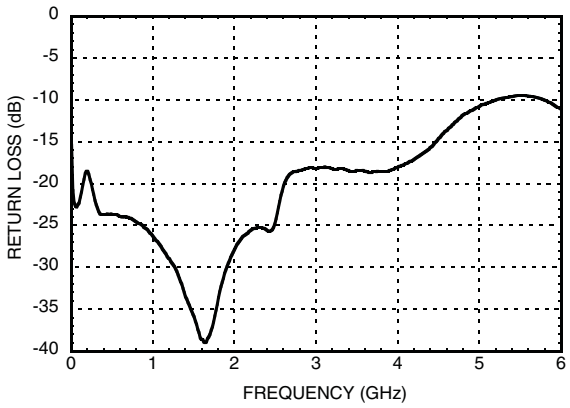
[1] CW Input Waveform

[2] RMSA referenced

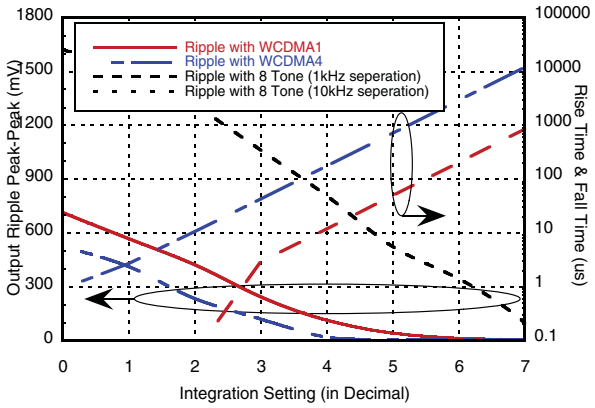
Typical Supply Current vs. Pin, Vcc=5V [1]



Input Return Loss vs. Frequency

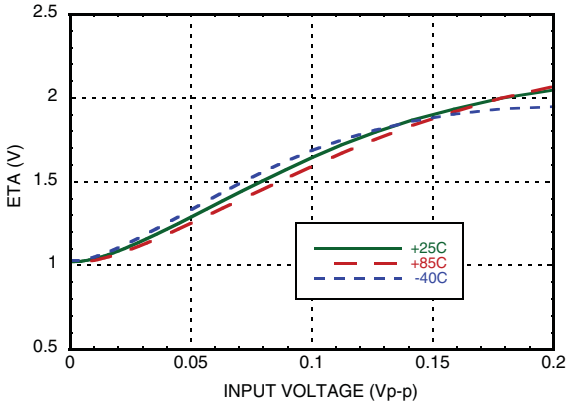


Output Ripple & Rise/Fall Time vs. Integration Setting[Sci4,Sci3,Sci2,Sci1] in Decimal

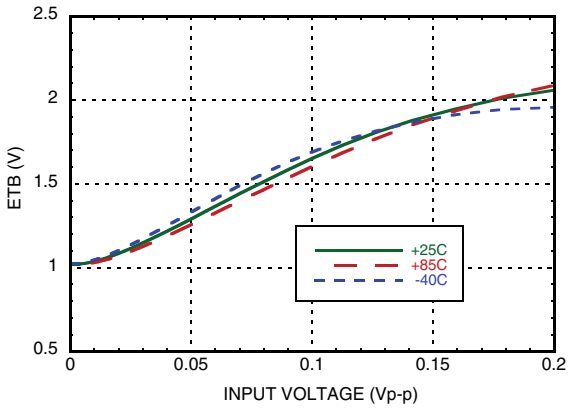


[1] CW Input Waveform

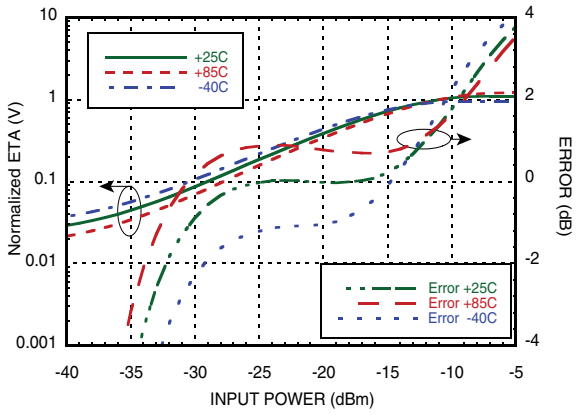
ETA vs. Pin with CW @ 900 MHz



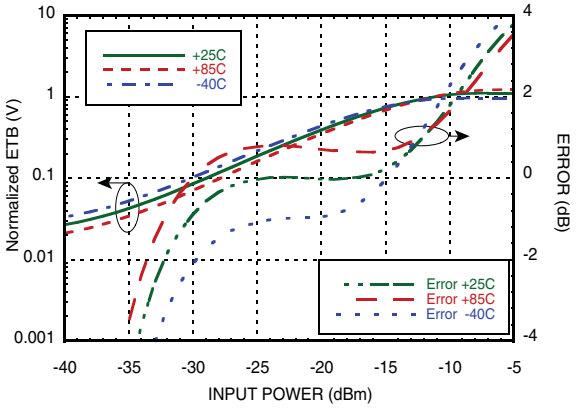
ETB vs. Pin with CW @ 900 MHz



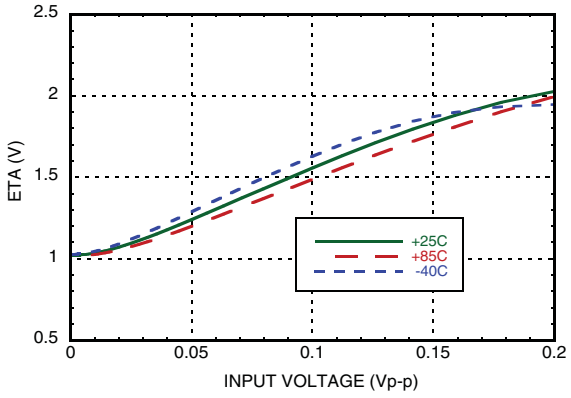
ETA & ETA Error vs. Pin with CW @ 900 MHz



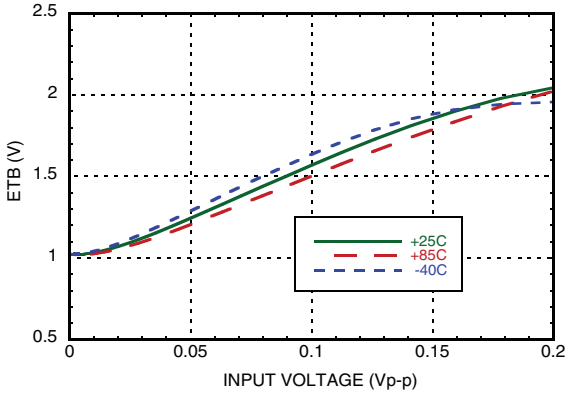
ETB & ETB Error vs. Pin with CW @ 900 MHz



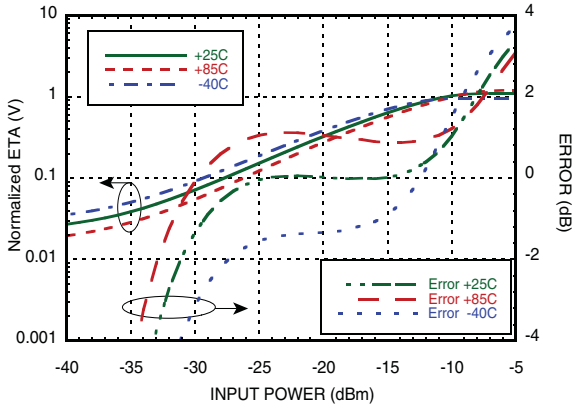
ETA vs. Pin with CW @ 1900 MHz



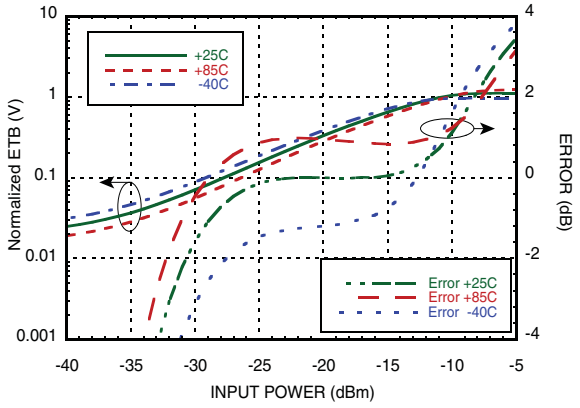
ETB vs. Pin with CW @ 1900 MHz



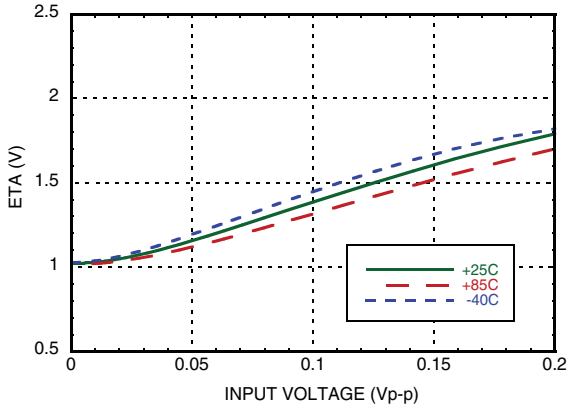
ETA & ETA Error vs. Pin with CW @ 1900 MHz



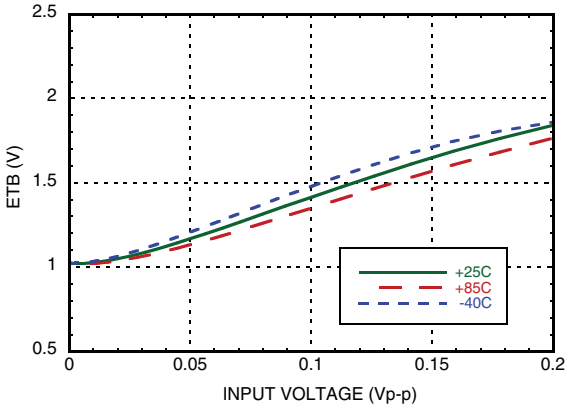
ETB & ETB Error vs. Pin with CW @ 1900 MHz



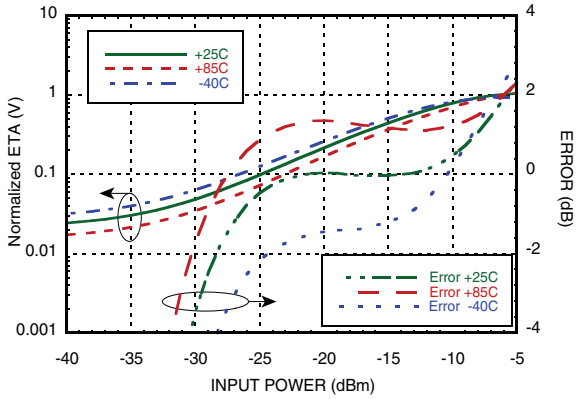
ETA vs. Pin with CW @ 3500 MHz



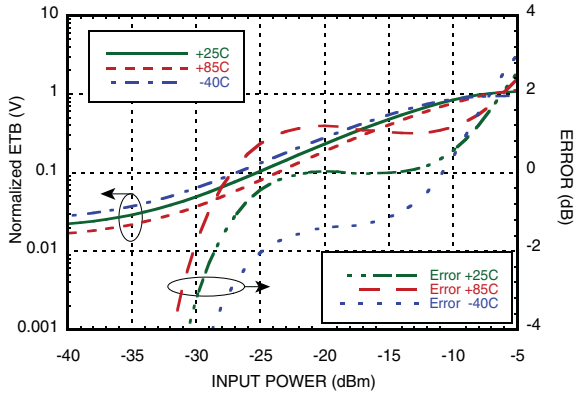
ETB vs. Pin with CW @ 3500 MHz



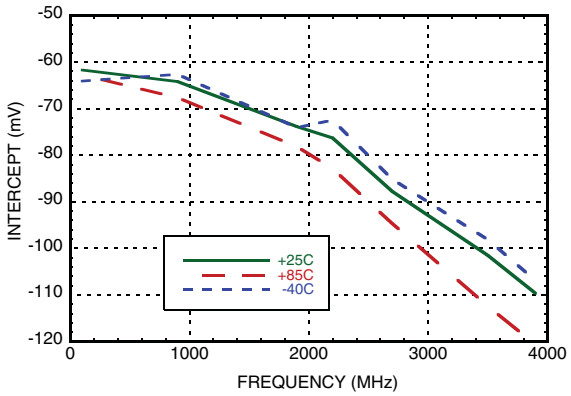
ETA & ETA Error vs. Pin with CW @ 3500 MHz



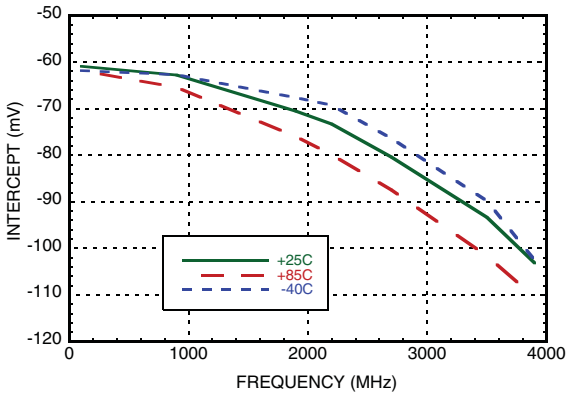
ETB & ETB Error vs. Pin with CW @ 3500 MHz



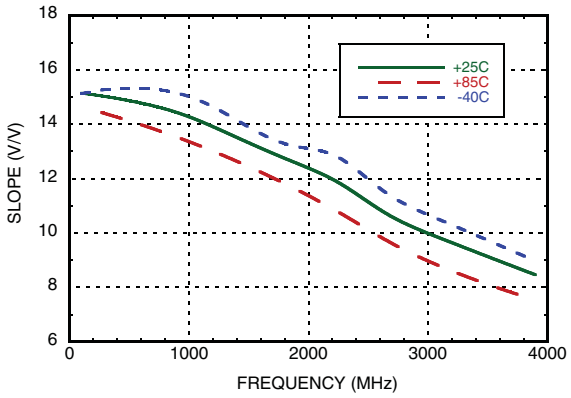
ETA Intercept vs. Frequency with CW



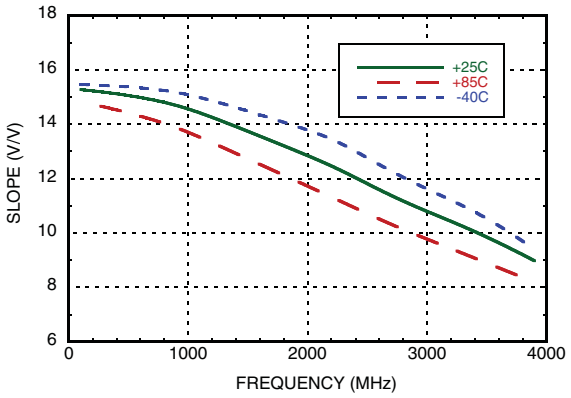
ETB Intercept vs. Frequency with CW



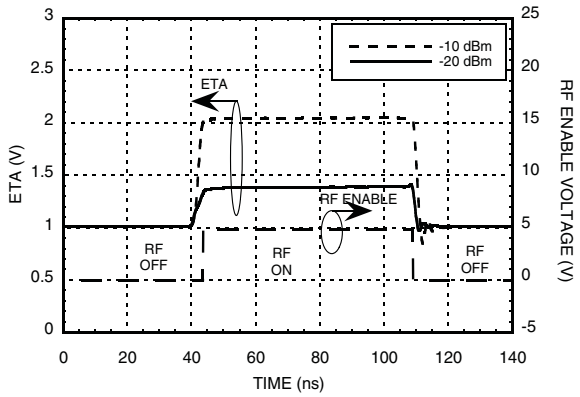
ETA Slope vs. Frequency with CW



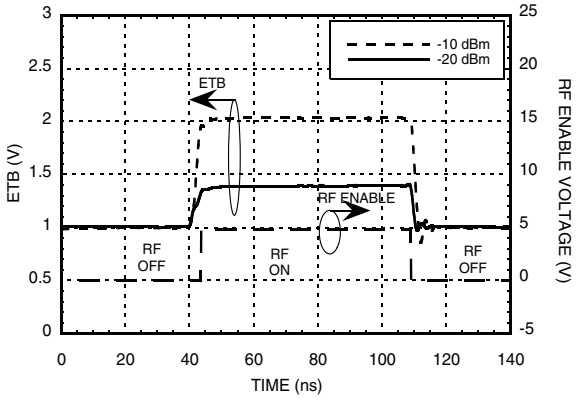
ETB Slope vs. Frequency with CW



ETA Output Response @ 1900 MHz



ETB Output Response @ 1900 MHz



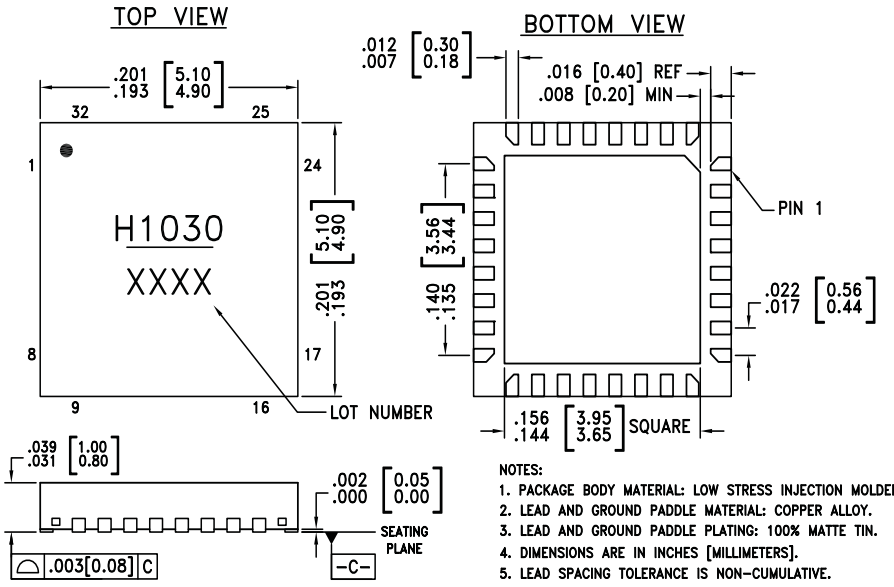
For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

Absolute Maximum Ratings

Supply Voltage	5.6V
Single-Ended RF Input Power	10 dBm
Input Voltage	VCC ± 0.6V
Channel / Junction Temperature	125°C
Continuous Pdiss (T = 85°C) (Derate 55.29 mW/°C above 85°C)	2.21 Watts
Thermal Resistance (R_{th}) (junction to ground paddle)	18.09 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



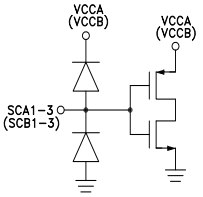
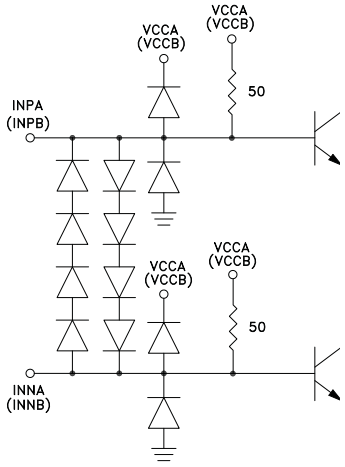
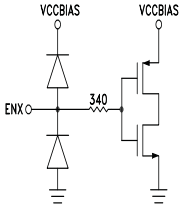
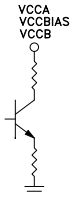
NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

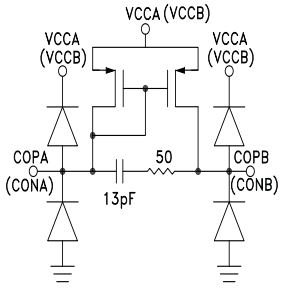
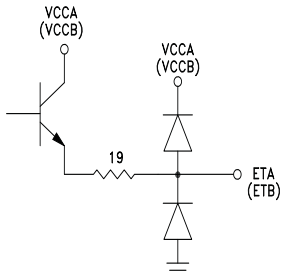
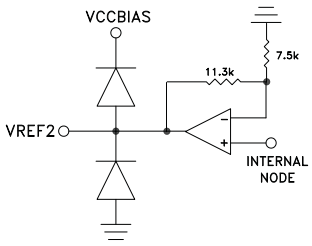
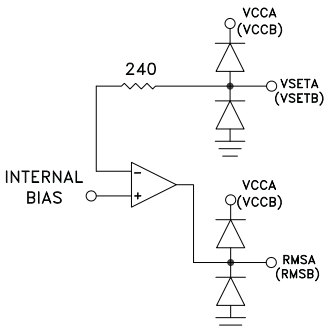
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC1030LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H1030 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

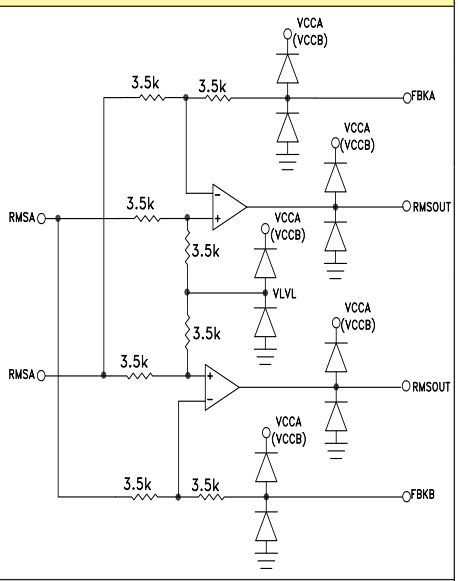
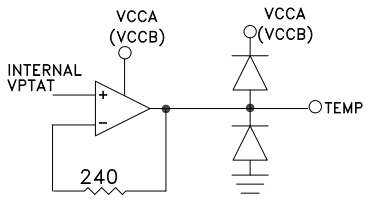
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 8, 9, 10, 31,32	SCA1, SCB1, SCB2, SCB3, SCA3, SCA2	Digital input pins that control the internal integration time constant for mean square calculation. SCA(B)3 is the most significant bit. Set V>0.2xVcc to disable. Shortest integration time is for SCA(B)=000, longest integration time is for SCA(B)=111. Each step changes the integration time by 1 octave.	
2, 3 6, 7	INNA, INPA INPB, INNB	RF Input Pins.	
4, 25	ENX, ENOUT	The ENX input is the active low enable pin of the whole device. The ENOUT input is the active high enable pin of the integrated OpAmps driving OUTA & OUTB, ETA & ETB. For normal operation, ENX should be connected to GND and ENOUT should be connected to Vcc.	
5, 11, 30	VCCBS, VCCB, VCCA	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	

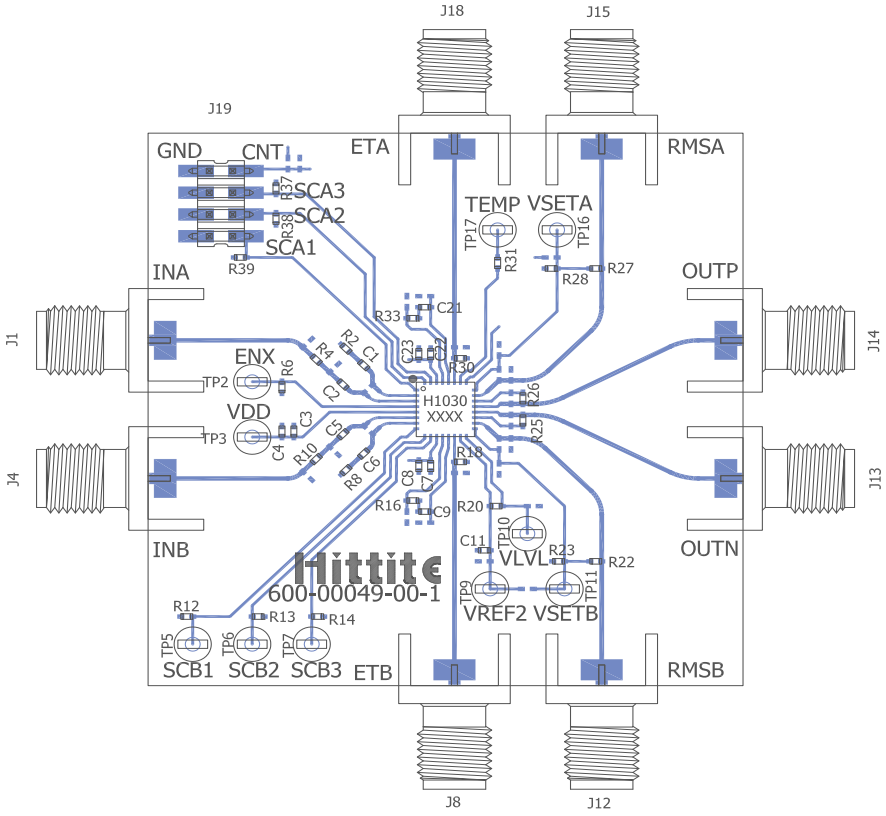
Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
12, 13, 28, 29	COPB, CONB, CONA, COPA	Input high pass filter capacitor. Connect a capacitor between COPA(CONA) and COPB(CONB) to determine 3 dB point of input signal high-pass filter.	
14, 27	ETB, ETA	Linear output that provides an indication of envelope of the input signal.	
15	VREF2	2.5V Reference voltage output.	
16	VLVL	Reference level input for OUTP and OUTN. Connect to VREF for normal operation.	
17, 24	VSETB, VSETA	VSET inputs. Set point inputs for controller mode.	
18, 23	RMSB, RMSA	Logarithmic outputs that convert the input power to a DC level for channel A and channel B.	

Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
19	FBKB	Feedback through 3.5k Ohm to the negative terminal of the integrated Op Amp driving OUTN	
20	OUTN	Output providing the difference of RMS outputs using an Op Amp. For normal operation, connected to FBKB to provide the function: OUTN = RMSB - RMSA + VLVL	
21	OUTP	Output providing the difference of RMS outputs using an Op Amp. For normal operation, connected to FBKA to provide the function: OUTP = RMSA - RMSB + VLVL	
22	FBKA	Feedback through 3.5K Ohms to the negative terminal of the integrated Op Amp driving OUTP	
26	TEMP	Temperature sensor output. See Application Note section.	
	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	

Evaluation PCB - Wideband Single-Ended



List of Materials for Evaluation PCB EVAL01-HMC1030LP5E[1]

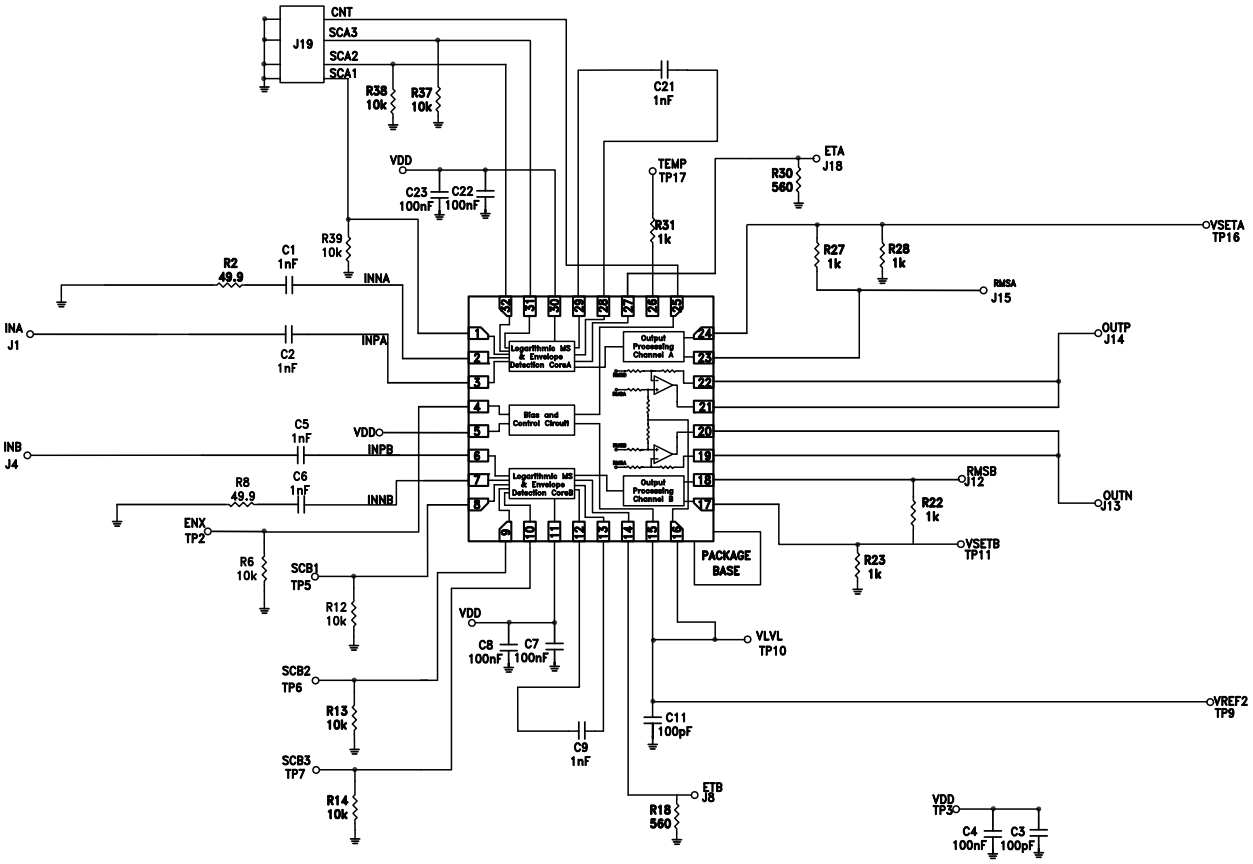
Item	Description
J1, J4, J8, J12, J13, J14, J15, J18	SMA Connector
J19, TP2, TP3, TP5, TP6, TP7, TP9, TP10, TP11, TP16, TP17	DC Pin
C1, C2, C5, C6, C9, C21	1 nF Capacitor, 0402 Pkg.
C3,C7, C11, C22	100 pF Capacitor, 0402 Pkg.
C4,C8,C23	100 nF Capacitor, 0402 Pkg.
R2, R8	49.9 Ohm Resistor, 0402 Pkg.
R18, R30	560 Ohm Resistor, 0402 Pkg.
R22, R23, R27, R28, R31	1K Ohm Resistor, 0402 Pkg.
R6, R12-14,R37-39	10K Ohm Resistor, 0402 Pkg.
R4, R10,R16, R20,R25-26, R33	0 Ohm Resistor, 0402 Pkg.
U1	HMC1030LP5E Single-Ended Dual RMS Power Detector
PCB [2]	600-00049-00-1 Evaluation PCB

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

[1] Reference this number when ordering complete evaluation PCB

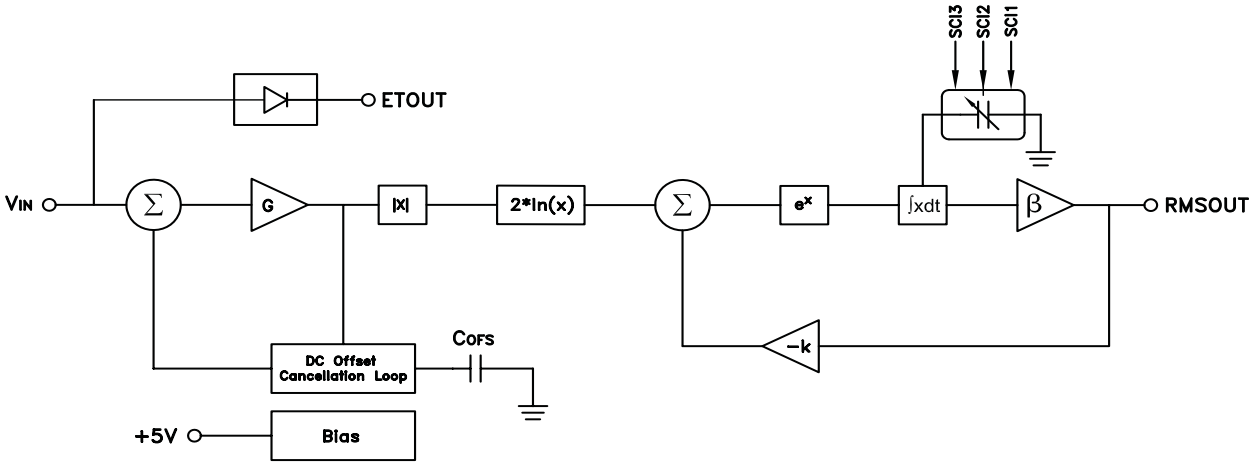
[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

Application Circuit - Wideband Single-Ended



Application Information

Principle of Operation



The HMC1030LP5E is a dual-channel RMS and Envelope detector in a single package. The HMC1030LP5E's RMS detector core is designed to measure the actual RMS power of the input signal, independent of the modulated signal waveform complexity or the modulation scheme. The RMS detector core architecture of HMC1030LP5E is composed of a full-wave rectifier, log/antilog circuit, and an integrator as shown above. The RMS output signal is directly proportional to the logarithm of the time-average of V_{IN}^2. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signal levels can be measured accurately.

The HMC1030LP5E supports controller mode operation. For more information regarding controller mode operation, please contact Hittite application support.

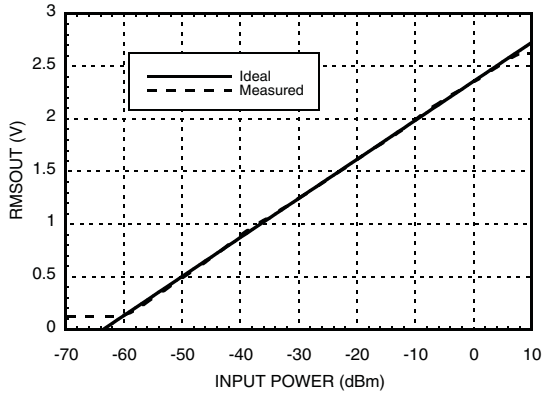
The HMC1030LP5E achieves exceptional RF power measurement accuracy independent of the modulation of the carrier with this system architecture. The relation between the HMC1030LP5E's RMSOUT output and the RF input power is given below

$$V_{RMSOUT} = \frac{1}{k} \ln(\beta k G^2 \int V_{IN}^2 dt)$$

Where ß is op-amp gain set via resistors on the V_{set} pin.

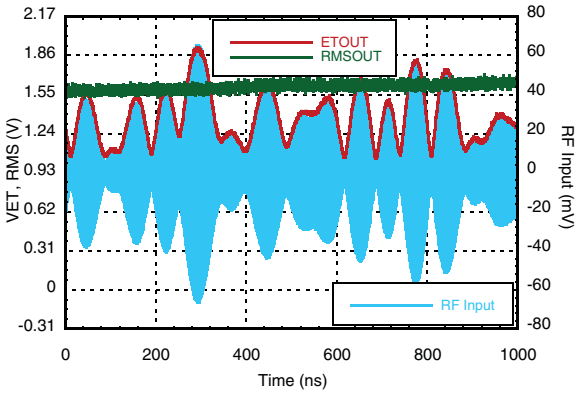
P_{in} = V_{RMS}/[log-slope]+[log-intercept], dBm

VRMSA vs. P_{IN} with WCDMA 4 Carrier @ 1900 MHz



HMC1030LP5E's envelope detector core is capable of extracting the envelope information of the modulated RF signal with modulation bandwidths in excess of 100 MHz. The extracted envelope information is independent of the average power and the crest factor of the RF signal. The RMS detector core provides a linear-in-dB output of the average RF power, whereas the envelope detector core provides a linear representation of the instantaneous envelope waveform. The envelope detection feature may be used in ultra-fast excessive RF power protection systems, PA linearization techniques and in efficiency enhancing Envelope-Tracking PA implementations.

VRMSA & VETA & WCDMA 4 Carrier with -20dBm RF Input vs. Time @ 900 MHz



Measuring the ETOUT and RMS output voltage signals simultaneously provides a very informative picture of the RF input signal such as, peak power, average power, peak-to-average power, and RF wave-shape. Simultaneous measurement of instantaneous signal power and average power is essential for taking full advantage of a receive signal chain's available dynamic range, while avoiding saturation, or to maximize transmitter efficiency.

Configuration for the Typical Application

The HMC1030LP5E requires a single 5V supply with an adequate power supply decoupling as recommended in the application schematic.

Inputs of the HMC1030LP5E are broadband matched to 50 Ohm single-ended with details included in the subsequent "Broadband Single-Ended Input Interface" section.

The RMSA & RMSB outputs are typically connected to VSETA & VSETB inputs through a resistive network, resulting in a Pin VRMS transfer characteristic with a slope of 37 mV/dBm (at 1900 MHz) for both channels. However, the RMS outputs can be re-scaled to "magnify" a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS outputs. Refer to the section under the "Log-Slope and Intercept" section for details.

The OUTP & OUTN outputs provide the input signal power ratio between the two power detection channels. The OUTP & OUTN outputs are typically connected to FBKA & FBKB. An input voltage applied to the VLVL input pin is used to set the common mode voltage reference level for the OUTP & OUTN. The VLVL pin is typically connected to VREF2 output to provide a nominal bias voltage of 2.5V. Optionally, external bias voltage may be applied to VLVL. Refer to the section under the "Channel Difference Outputs" for details.

The ETA & ETB outputs provide linearly scaled replica of the instantaneous envelope of the modulated RF signal with modulation bandwidths up to 150 MHz for both channels. For optimum performance, the ET outputs of the HMC1030LP5E should be terminated to ground with a 560 Ohm load resistor. Refer to the section under the "Envelope Detector Output" for details.

The SCA1-3 & SCB1-3 inputs are configured digitally to set the integration bandwidth of the RMS detectors for both channels. Refer to the section under the “RMS Output Interface and Transient Response” section for details.

The COFAP-N & COFBP-N inputs determine the 3dB bandwidth of the input high pass filter for both channels. Typically 1nF external high pass filter capacitors are connected between COFAP & COFAN and between COFBP & COFBN for a banwdith of 62 kHz.

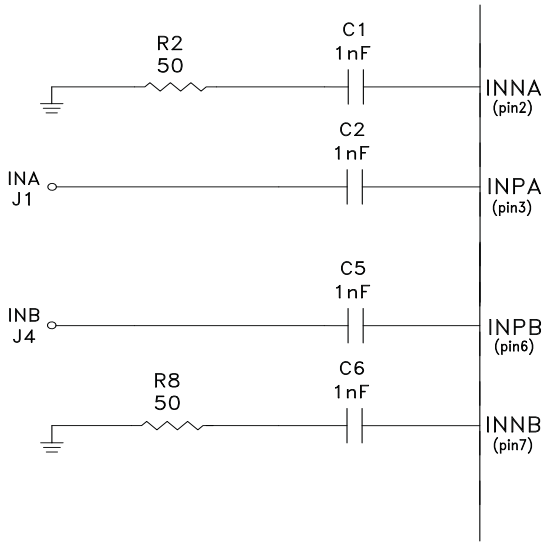
The ENX input is the active low enable pin of the whole device. The ENOUT input is the active high enable pin of the integrated OpAmps driving OUTA & OUTB, ETA & ETB. For normal operation, ENX should be connected to GND and ENOUT should be connected to Vcc.

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements: refer to the “System Calibration” section for more details.

Broadband Single-Ended Input Interface

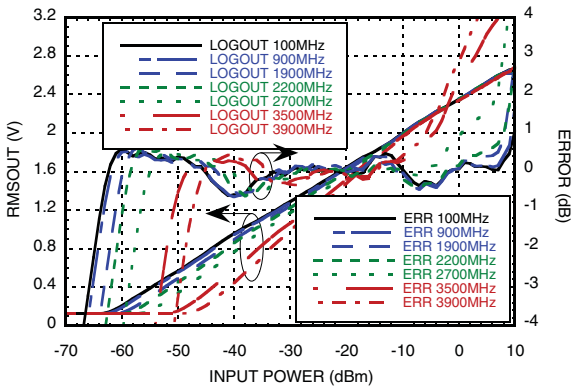
The HMC1030LP5E inputs are broadband matched to single-ended 50 Ohm with the configuration shown below. The interface and requires only two external DC blocking capacitors and an external 50 Ohm resistor over the entire frequency band of operation.

The integrated broadband single-ended input interface of HMC1030LP5E eliminates the requirement for an external balun transformer or matching network and provides a compact, broadband solution.



Note that the provided single-ended input interface covers the whole operating spectrum of the HMC1030LP5E and does not require matching tuning for different frequencies. The performance of the HMC1030LP5E at different frequencies is shown below:

VRMSA & Error vs. Pin



Dual RMS Detection Channels

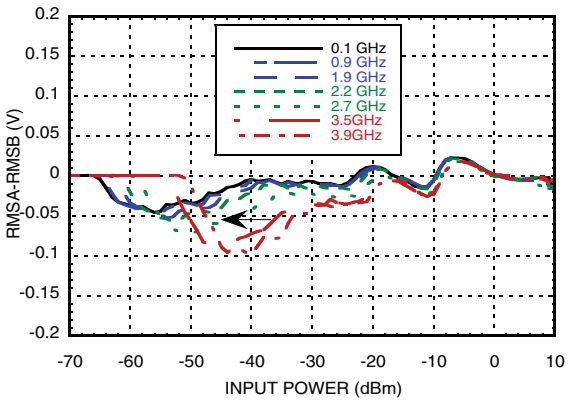
The HMC1030LP5E integrates two HMC1021LP4E RMS detection channels with shared bias and control circuitry. Proprietary design techniques enable extremely good matching between channels over a wide range of input frequencies with low temperature drift.

Channel Matching

Part-to-part variations for single channel RMS detectors complicate simultaneous power readings. Simultaneous signal power measurements are particularly useful for automatic gain/level control and VSWR measurements. When separate power detectors are used, the lack of an accurate match between the power detectors result in measurement errors. Calibration and compensation methods are required to counteract the differences between the separate power detectors. The HMC1030LP5 dual RMS detector greatly simplifies that activity, and will reliably produce more accurate measurements.

The HMC1030LP5E provides industry leading channel matching performance with the use of proprietary techniques. The channel mismatch is typically less than 100 mV over the specified temperature and frequency range with the integrated broadband single-ended input interface.

Channel Matching (RMSA-RMSB)



Channel Isolation/Interference

Off-chip interference between channels should be minimized with good RF board design practices and the quality of the soldered connections.

On-chip inter-channel interference, manifests itself as the variation on one detector output due to a relatively strong signal present at the other detector input. Quantitatively, the input-output channel isolation is defined as the difference between the input power levels at both channels when the interfering (higher power level) channel causes a 1 dB measurement error in the victim channel. Worst case channel interference occurs when victim channel has an input signal level just over its detection threshold.

Input-Output Channel isolation for HMC1030LP5E is:

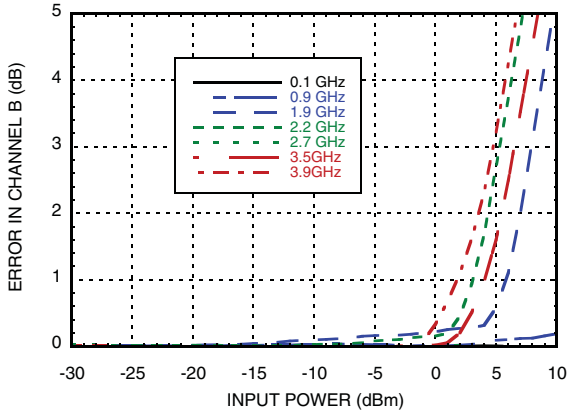
55 dB input-output isolation at 0.9 GHz
49 dB input-output isolation up to 2.2 GHz
40 dB input-output isolation up to 3.9 GHz.

For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

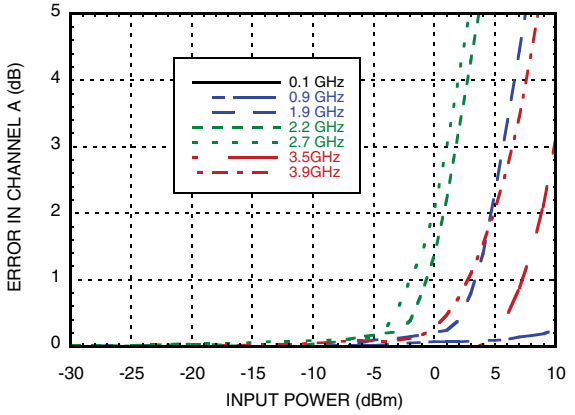
If the same input signal frequency is applied to both channels, the interference will occur as a phase delay.

A slight offset in signal frequency between the two channels can be seen as a ripple at the output of the channel with the lower power level applied at its input. Peaks in the output ripple correspond to the worst-case phase shift for input-output interference. The frequency of the output ripple will be equal to the "beat" frequency between the two channels. The magnitude of the output ripple will depend on the SCI (integration) settings and offset capacitors connected to COFA & COFB pins, respectively. The output ripple is reduced by increasing the value of the SCI setting, thereby decreasing the integrator bandwidth. The data was collected using a 1 kHz offset between the channels.

Interference to an Input Signal (INB Power Fixed) with Interfering Signal on the other Channel (INA Power Swept)



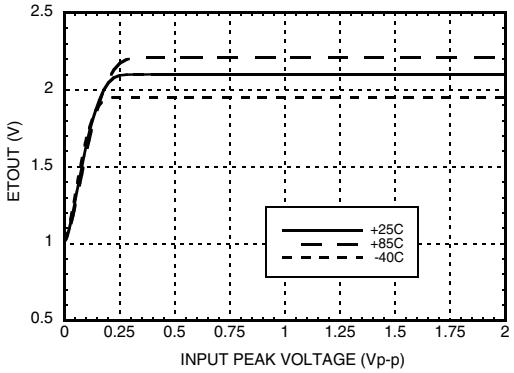
Interference to an Input Signal (INA Power Fixed) with Interfering Signal on the other Channel (INB Power Swept)



Envelope Detector Outputs

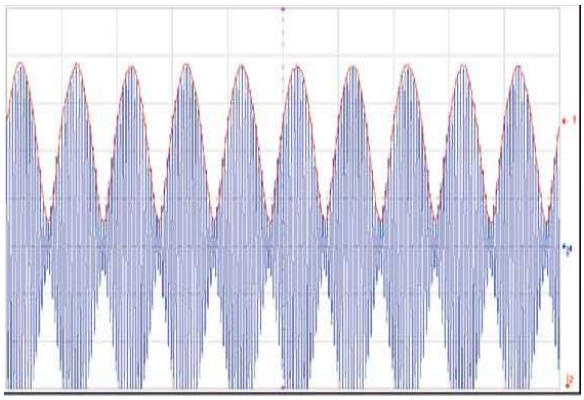
The HMC1030LP5E features envelope detection for both channels. The ETA & ETB outputs provide a linearly scaled replica of the instantaneous envelope of the modulated RF signal for modulation bandwidths up to 150 MHz at for both channels. For optimum performance, the ETA & ETB pins of the HMC1030LP5E should be terminated with a 560 Ohm load resistor to GND. Note that any capacitive loading on the ETA & ETB pins would reduce the modulation bandwidth of the envelope detection. The envelope outputs have a conversion gain of 15V/V with an output voltage ranging from 1.0V to 2.1V.

ETA vs. Input Peak Voltage @ 900 MHz



The waveform below shows the HMC1030LP5E's envelope detector response to an RF input signal with a 100 MHz modulation bandwidth.

ETOUT Response to an RF Input Signal with 100 MHz Modulation Bandwidth



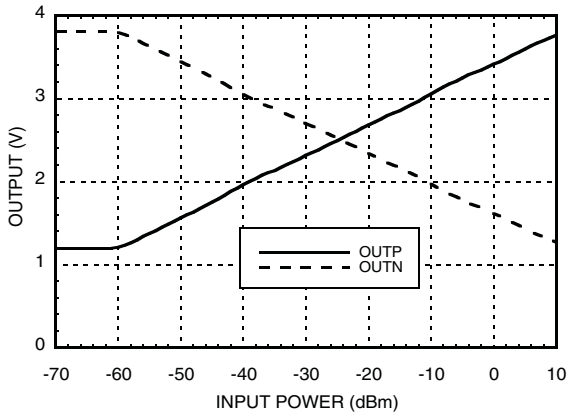
Channel Difference Outputs

HMC1030LP5E features OUTP and OUTN "channel difference" outputs that can be used differentially or single-ended. The OUTP and OUTN outputs provide direct read of input signal power ratio between the two channels. The OUTP and OUTN are connected to FBKA and FBKB pins respectively. The OUTP and OUTN are defined with the following equations:

OUTP = RMSA - RMSB + VLVL
OUTN = RMSB - RMSA + VLVL

Where, the VLVL is the common mode reference level applied at the VLVL pin. The VLVL pin can be connected to VREF2 output to provide a nominal base voltage of 2.5V. Optionally; external bias voltage can be applied to VLVL.

Channel Difference Outputs @ 1900 MHz, Channel A Power Swept, Channel B @ -25 dBm, VLVL=2.5V



With the channels of HMC1030LP5E having very low mismatch, and located on the same die, the channel outputs RMSA and RMSB track very closely over temperature. The difference operation also allows the OUTP and OUTN to reject common-mode changes in channels A and B.

RMS Output Interface and Transient Response

The HMC1030LP5E features digital input pins (SCI1-SCI3) that control the internal integration time of the RMS detector. The RMS output transient response is determined by the digital integration controls, and output load conditions.

The SCI3 is the most significant bit, and the longest integration time is for SCI=111.

Using larger values of SCI will narrow the operating bandwidth of the integrator, resulting in a longer averaging time interval and a more filtered output signal. It will also slow the power detector's transient response. A larger SCI value favors output accuracy over speed. For the fastest possible transient settling time,s set SCI to 000. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. For most applications an SCI setting may be selected to maintain a balance between speed and accuracy. Furthermore, error performance over modulation bandwidth is dependent on the SCI setting. For example modulations with relatively low frequency components and high crest factors may require higher SCI (integration) settings.

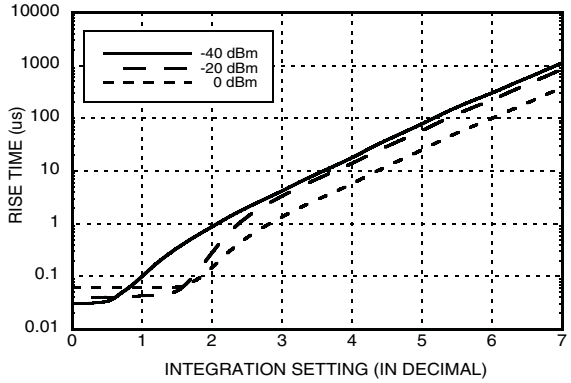
Excessive loading at the RMS output impacts the transient response. It is recommended to keep load resistance above 500 Ohm.

For increased load drive capability, consider a buffer amplifier on the RMS output. Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering when operating HMC1030LP5E with a lower SCI value.

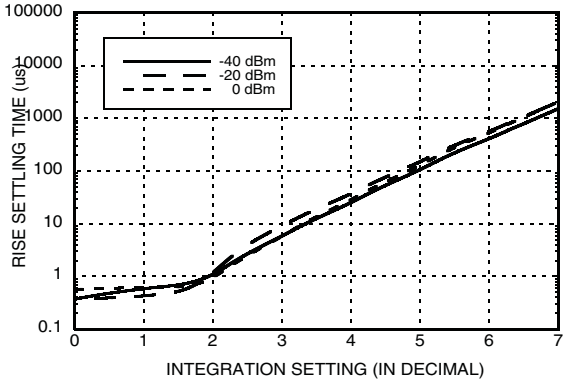
Table 1: Transient Response vs. SCI Setting:

	RMSOUT Rise-Time 10% -> 90% (µs) [3]			RMSOUT Rise Settling Time (µs) [2]			RMSOUT Fall-time 100% -> 10% (µs) [4]		
SCI3,2,1	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm
000	0.06	0.04	0.03	0.06	0.04	0.04	0.9	0.9	0.8
001	0.06	0.04	0.06	0.06	0.04	0.06	2.7	2.7	2.54
010	0.06	0.06	0.74	0.06	2.30	0.78	10.7	10.7	10
011	1.18	2.94	3.57	4.69	8	5	43.7	43	41.4
100	4.82	11.9	15	23.9	32	21.5	178	176	169
101	21.3	50	67.2	107	130	91.3	727	718	667
110	90.5	205	278	486	520	378	3000	2950	2730
111	381	851	1120	2047	2042	1515	12240	12066	11770

Rise Time[1] vs. SCI Setting over Input Power

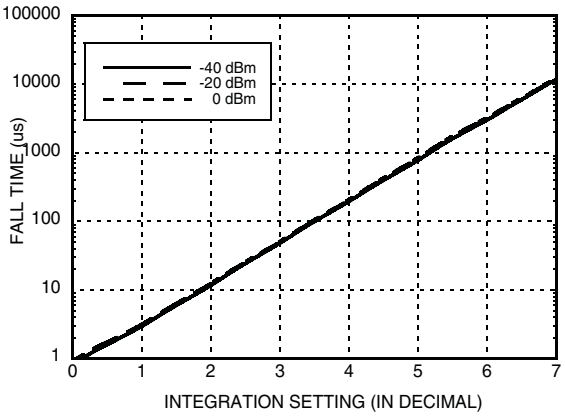


Rise Settling Time[2] vs. SCI Setting over Input Power

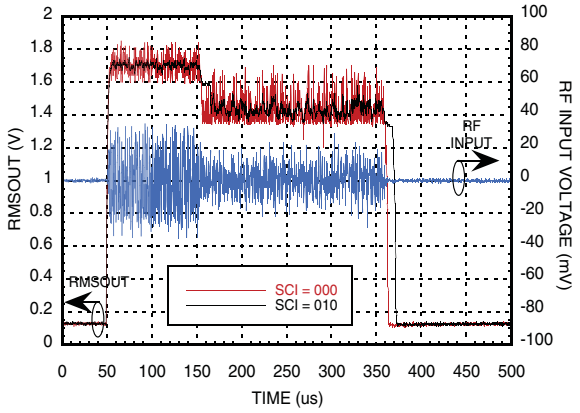


[1] Measured from 10% to 90% [2] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.

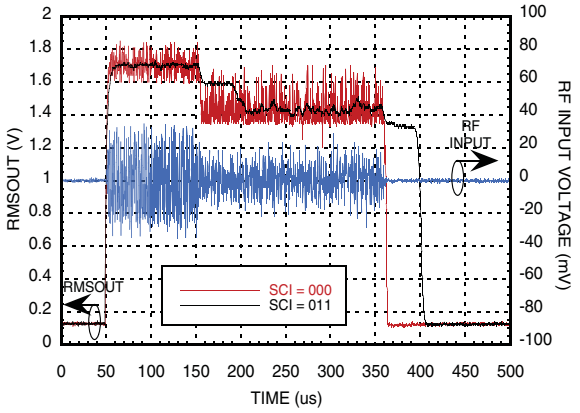
Fall Time [1] vs. SCI Setting over Input Power



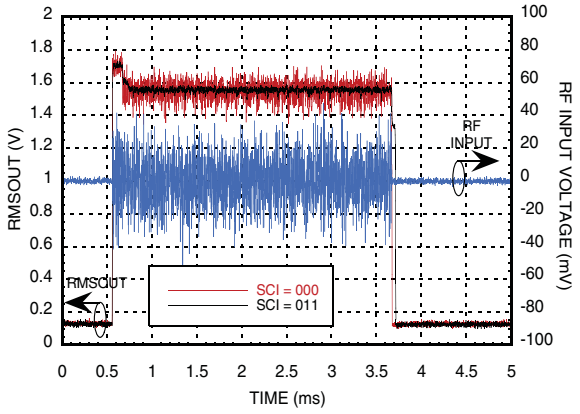
Residual Ripple for 0.9 GHz OFDM Advanced 802.16 @ SCI = 010



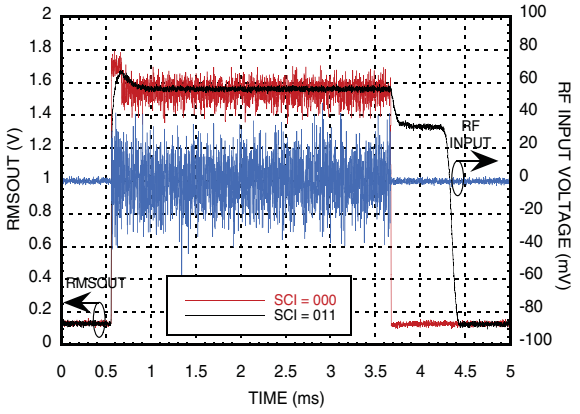
Residual Ripple for 0.9 GHz WiMAX OFDM Advanced 802.16 @ SCI = 011



Residual Ripple for 0.9 GHz WIBRO @ SCI = 011

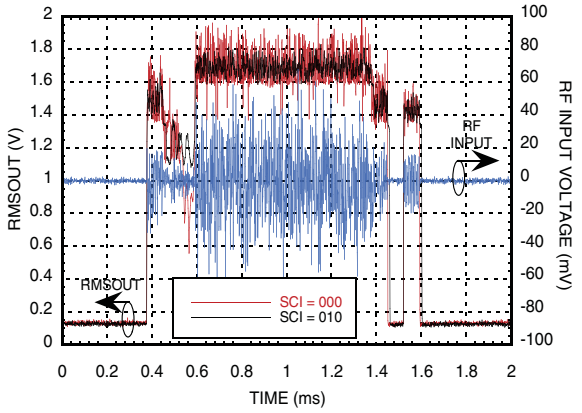


Residual Ripple for 0.9 GHz WIBRO @ SCI = 101

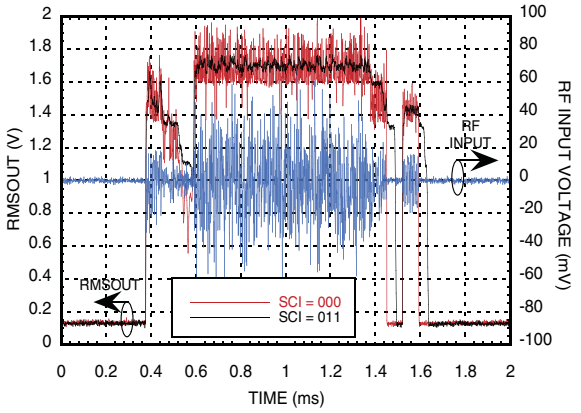


[1] Measured from 100% to 10%

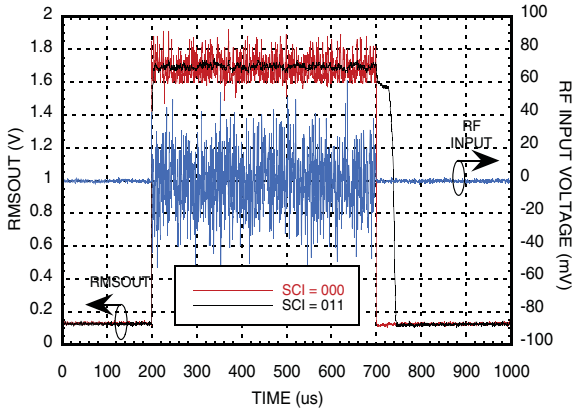
Residual Ripple for 0.9 GHz LTE Downlink @ SCI = 010



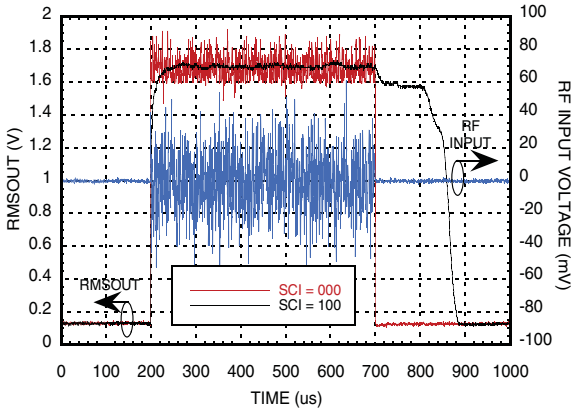
Residual Ripple for 0.9 GHz LTE Downlink @ SCI = 011



Residual Ripple for 0.9 GHz WCDMA-4TM @ SCI = 011



Residual Ripple for 0.9 GHz WCDMA-4TM @ SCI = 100

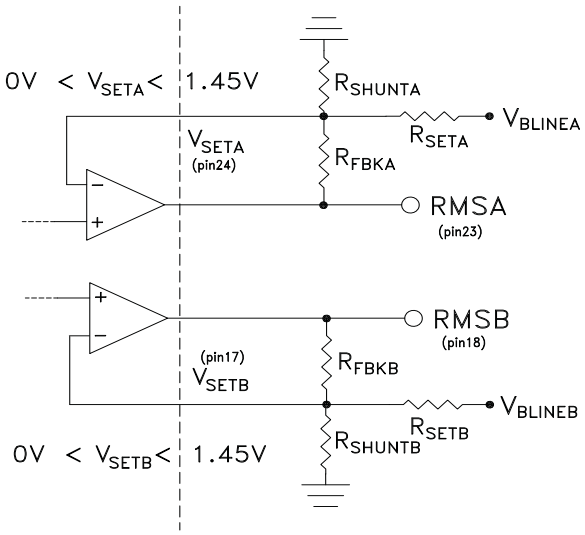


LOG-Slope and Intercept

The HMC1030LP5E provides for an adjustment of output scale with the use of integrated operational amplifiers for both channels. Log-slope and intercept can be adjusted to “magnify” a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS outputs.

A log-slope of 37 mV/dB (@1900 MHz) is set by connecting RMS Output to VSET through a resistor network for B=1 (see application schematic). The log-slope is adjusted by using the appropriate resistors RFBKA, RFBKB, RSHUNTA, RSHUNTB on the RMSA/RMSB and VSETA/VSETB pins. Log-intercept is adjusted by applying DC voltage to the VBLINEA and /VBLINEB.

Due to the 15k Ohm input resistance at the VSETA/VSETB pins, moderately low resistance values should be used to minimize the scaling errors. Very low resistor values will reduce the load driving capabilities of RMSA/RMSB outputs while larger values will result in scaling errors and increase of the temperature errors because of the mismatch of the on-chip and external resistor temperature coefficients.



Optimized slope = B * log-slope

Optimized intercept = log-intercept – (RFBK /RSET) * VBLINE

$$\beta = (1/2)\frac{R_{FBK}}{R_{FBK} // R_{SHUNT} // R_{SET}}$$

When R_{FBK}=0 to set VRMS=VSET, then B=1/2.

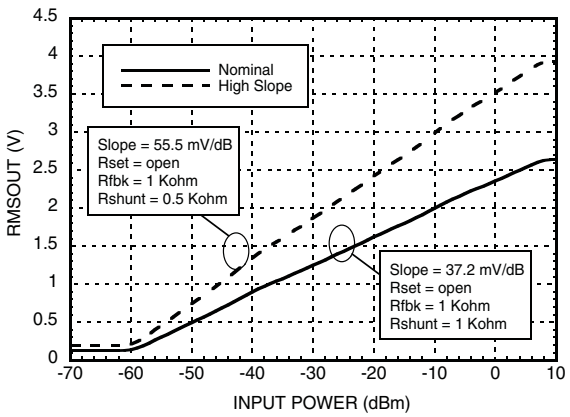
If R_{SET} is not populated, then B =1/2 * (R_{FBK}/ (R_{FBK} // R_{SHUNT})) and intercept is at nominal value.

Note: Avoid excessive loading of the RMS output; keep C_{LOAD} < 35 pF, and R_{LOAD} > 375 Ohm

Example: The logarithmic slope can be simply increased by choosing appropriate R_{FBK} and R_{SHUNT} values while not populating the R_{SET} resistor on the evaluation board to keep the intercept at nominal value.
Setting RFBK =1k Ohm and R_{SHUNT} = 0.5k Ohm results in an optimized slope of:

Optimized Slope = B * log_slope = 1.5* 37 mV / dB
Optimized Slope = 55.5 mV / dB

Slope Adjustment



Example: The logarithmic intercept can also be adjusted by choosing appropriate R_{FBK}, R_{SHUNT}, and R_{SET} values.

Setting R_{FBK} = 1k Ohm, R_{SHUNT} =0.5k Ohm, and R_{SET} = 4.7k Ohm results in an optimized slope of:

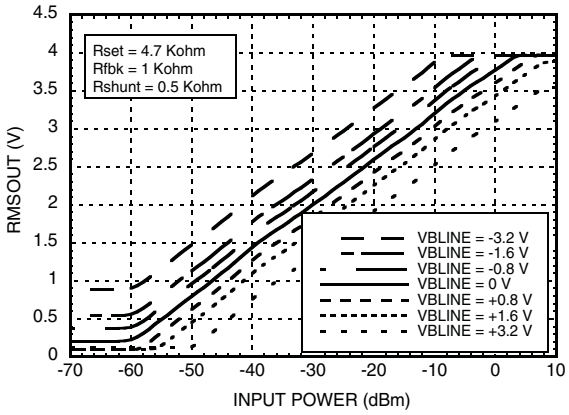
Optimized Slope = B * log_slope = 1.6 * 37 mV / dB

Optimized Slope = 59.2 mV / dB

Optimized Intercept = log_intercept –(R_{FBK}/R_{SET})*VBLINE

Optimized Intercept = log_intercept - 0.213 * VBLINE

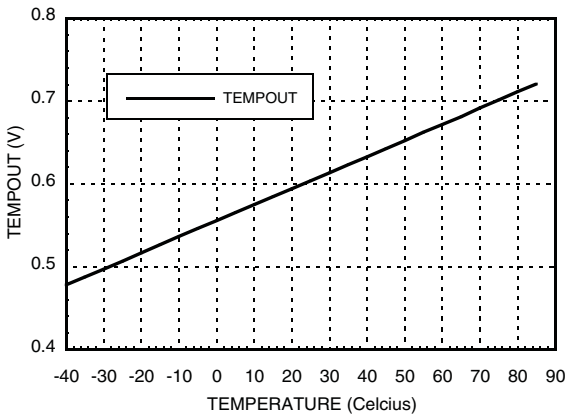
Intercept Adjustment



Temperature Sensor Interface

The HMC1030LP5E provides a buffered PTAT temperature sensor output that provides a temperature scaling factor of 2 mV/°C with a typical output voltage of 567 mV at 0°C. The output is capable of sourcing 1.5 mA.

TEMP Output



DC Offset Compensation Loop

Internal DC offsets, which are input signal dependant, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitances (COFS) connected between COFPA&COFNA pins and between COFPB&COFNB pins. The COFS capacitors sets the loop bandwidth of the DC offset compensations. Higher COFS values are required for measuring lower RF frequencies. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

$$\text{DC Offset Cancellation Loop} \approx \frac{1}{\pi(500)(C_{OFS} + 20 \times 10^{12})} \quad \text{Bandwidth , Hz}$$

For example: loop bandwidth for DC cancellation with C_{OFS} = 1nF, bandwidth is ~62 kHz

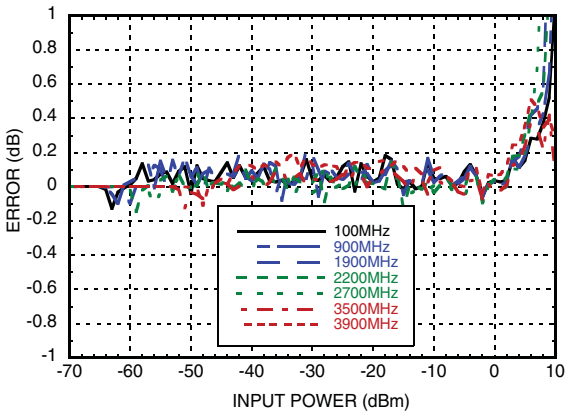
Standby Mode

The ENX pin can be used to force the power detector into a low-power standby mode. As ENX is deactivated, power is restored to all of the circuits. There is no memory of previous conditions. Coming out of stand by, internal integration and COFS capacitors will require recharging, so if large SCI values or large COFS capacitor values have been chosen, the wake-up time will be lengthened.

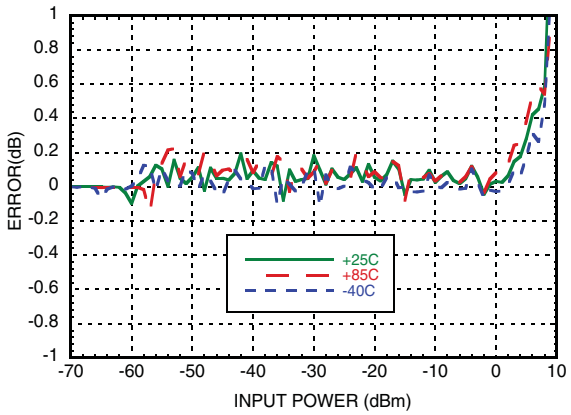
Modulation Performance – Crest factor performance

The HMC1030LP5E is able to detect the average power of RF signals with complex modulation schemes with exceptional accuracy. The proprietary RMS detection core is optimized to accurately detect the RMS power of the modulated RF signals with very high crest factors. This crest factor immune detection architecture of HMC1030LP5E results in detection accuracy of better than 0.2 dB over the entire operating frequency and temperature range, compared with the CW response under actual WCDMA4TM test signals shown below:

Reading Error for WCDMA 4 Carrier wrt CW Response @ +25°C



Reading Error for WCDMA 4 Carrier wrt CW Response @ 1900 MHz



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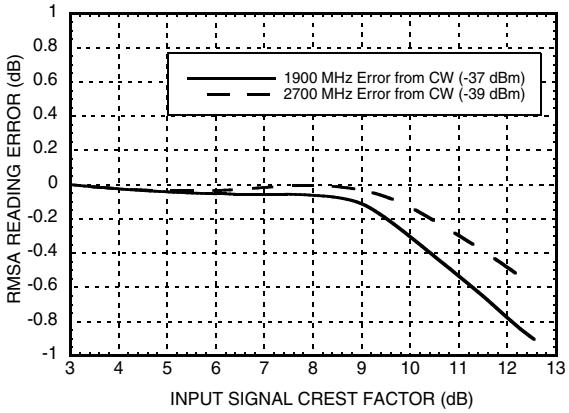
**RMSA Error vs.
Crest Factor over Frequency**



System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, choose at least two test points: near the top-end and bottom-end of the measurement range. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. Derive the log-slope and log-intercept, and store them in non-volatile memory.

For example if the following two calibration points were measured at 2.35 GHz:

With Vrms = 2.34V at Pin = -7 dBm,	Now performing a power measurement:
and Vrms=1.84V at Pin = -16 dBm	Vrms measures 2.13V
Slope Calibration Constant = SCC	[Measured Pin] = [Measured Vrms]*SCC + ICC
SCC = (-16+7)/(1.84-2.34) = 18 dB/V	[Measured Pin] = 2.13*18.0 – 49.12 = -10.78 dBm
Intercept Calibration Constant = ICC	An error of only 0.22 dB
ICC = Pin – SCC*Vrms = -7 – 18.0 * 2.34 = -49.12 dBm	

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector will operate over a wide range of frequencies, choose a central frequency for calibration.

Layout Considerations

- Mount RF input coupling capacitors close to the IN+ and IN- pins.
- Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.
- Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

Definitions:

- Log-slope: slope of P_{IN} –> V_{RMS} transfer characteristic. In units of mV/dB
- Log-intercept: x-axis intercept of P_{IN} –> V_{RMS} transfer characteristic. In units of dBm.
- RMS Output Error: The difference between the measured P_{IN} and actual P_{IN} using a line of best fit.

  [measured_P_{IN}] = [measured_V_{RMS}] / [best-fit-slope] + [best-fit-intercept], dBm
- Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with “RMS Output Error” falling within a specific error tolerance.
- Crest Factor: Peak power to average power ratio for time-varying signals.