Stepping Motor Driver Series

Standard 36V Stepping Motor Drivers

BD63801EFV

No.12009EAT07

●Description

BD63801EFV is rated 24V system maximum input voltage / 0.8A maximum output current and employs a constant-current PWM control scheme for low power consumption.
Serial (CLK-IN) drive mode allows for simple interfacing and operation, while allowing for full and half excitation modes. The single-power supply configuration allows for easy design and layout in the application.

●Feature

1) Power supply: one system drive (19V～28V)
2) Low ON resistance DMOS output
3) Serial (CLK-IN) drive mode
4) PWM constant current control (self oscillation)
5) Built-in spike noise cancel function (external noise filter is unnecessary)
6) FULL STEP applicable to HALF STEP
7) Normal / Reverse rotation switching function
8) Power save function*
9) Built-in logic input pull-down resistor
10) Power-on reset function
11) Thermal shutdown circuit (TSD)
12) Over current protection circuit (OCP)
13) Under voltage lock out circuit (UVLO)
14) Over voltage lock out circuit (OVLO)
15) Malfunction prevention at the time of no applied power supply (Ghost Supply Prevention)
16) Electrostatic discharge: 4kV (HBM specification)
17) Microminiature, ultra-slim and high heat-radiation (exposed metal type) HTSSOP package
18) Function pin compatible with constant current 2ch 36V Simple Stepping Motor Driver Series

●Application

PPC, Laser beam printer, Scanner, Photo printer, FAX, Ink jet printer, Mini printer, Sewing machine, Toy, and Robot etc.

●**Absolute maximum ratings(Ta=25℃)**

Item	Symbol	BD63801EFV	Unit
Supply voltage	$V_{CC1,2}$	-0.2～+36.0	V
Power dissipation	Pd	1.1※1	W
		4.0※2	
Input voltage for control pin	V_{IN}	-0.2～+5.5	V
RNF maximum voltage	V_{RNF}	0.5	V
Maximum output current	I_{OUT}	0.8※3	A/phase
Operating temperature range	T_{opr}	-25～+85	℃
Storage temperature range	T_{stg}	-55～+150	℃
Junction temperature	T_{jmax}	+150	℃

※1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 8.8mW/℃ for operating above Ta=25℃.
※2 4-layer recommended board. Derating in done at 32.0mW/℃ for operating above Ta=25℃.
※3 Do not, however exceed Pd, ASO and Tjmax=150℃.

●**Operating conditions(Ta= -25～+85℃)**

Item	Symbol	BD63801EFV	Unit
Supply voltage	$V_{CC1,2}$	19～28	V
Output current (DC)	I_{OUT}	0.5※4	A/phase

※4 Do not however exceed Pd, ASO.

●**Electrical characteristics**

Applicable to all the series (Unless otherwise specified Ta=25℃, $V_{cc1,2}$=24V)

Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Whole						
Circuit current at standby	I_{CCST}	-	0.6	2.0	mA	PS=L
Circuit current	I_{CC}	-	2.7	7.0	mA	PS=H, VREF=0.4V
Control input (CLK, FR, MODE, EN, PS)						
H level input voltage	V_{INH}	2.0	-	-	V	
L level input voltage	V_{INL}	-	-	0.8	V	
H level input current	I_{INH}	-	33	50	μA	V_{IN}=3.3V
Output (OUT1A, OUT1B, OUT2A, OUT2B)						
Output ON resistance	R_{ON}	-	2.8	3.6	Ω	I_{OUT} =0.3A Sum of upper and lower
Output leak current	I_{LEAK}	-	-	10	μA	
Current control						
RNFX input current	I_{RNFX}	-40	-20	-	μA	RNFX=0V
VREFX input current	I_{VREF}	-2.0	-0.1	-	μA	VREFX=0V
VREFX input voltage range	V_{REF}	0	-	0.4	V	
Comparator offset	V_{COFS}	-20	0	20	mV	VREFX=0.4V
Minimum on time	T_{ONMIN}	0.3	0.7	1.2	μs	R=39kΩ, C=1000pF

●Terminal function ・Block diagram・Application circuit diagram

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	PGND	Ground terminal	13	CLK	Clock input terminal (for advancing electrical angle)
2	EN	Output enable terminal	14	PGND	Ground terminal
3	VREF2	Output current value setting terminal	15	VCC1	Power supply terminal
4	CR2	Connection terminal of CR for setting PWM frequency	16	OUT1A	H bridge output terminal
5	NC	Non connection	17	RNF1	Connection terminal of resistor for output current detection
6	TEST	Terminal for testing (used by connecting with GND)	18	OUT1B	H bridge output terminal
7	GND	Ground terminal	19	OUT2B	H bridge output terminal
8	PS	Power save terminal	20	RNF2	Connection terminal of resistor for output current detection
9	CR1	Connection terminal of CR for setting PWM frequency	21	OUT2A	H bridge output terminal
10	VREF1	Output current value setting terminal	22	VCC2	Power supply terminal
11	MODE	Motor excitation mode setting terminal	23	NC	Non connection
12	NC	Non connection	24	FR	Motor rotating direction setting terminal

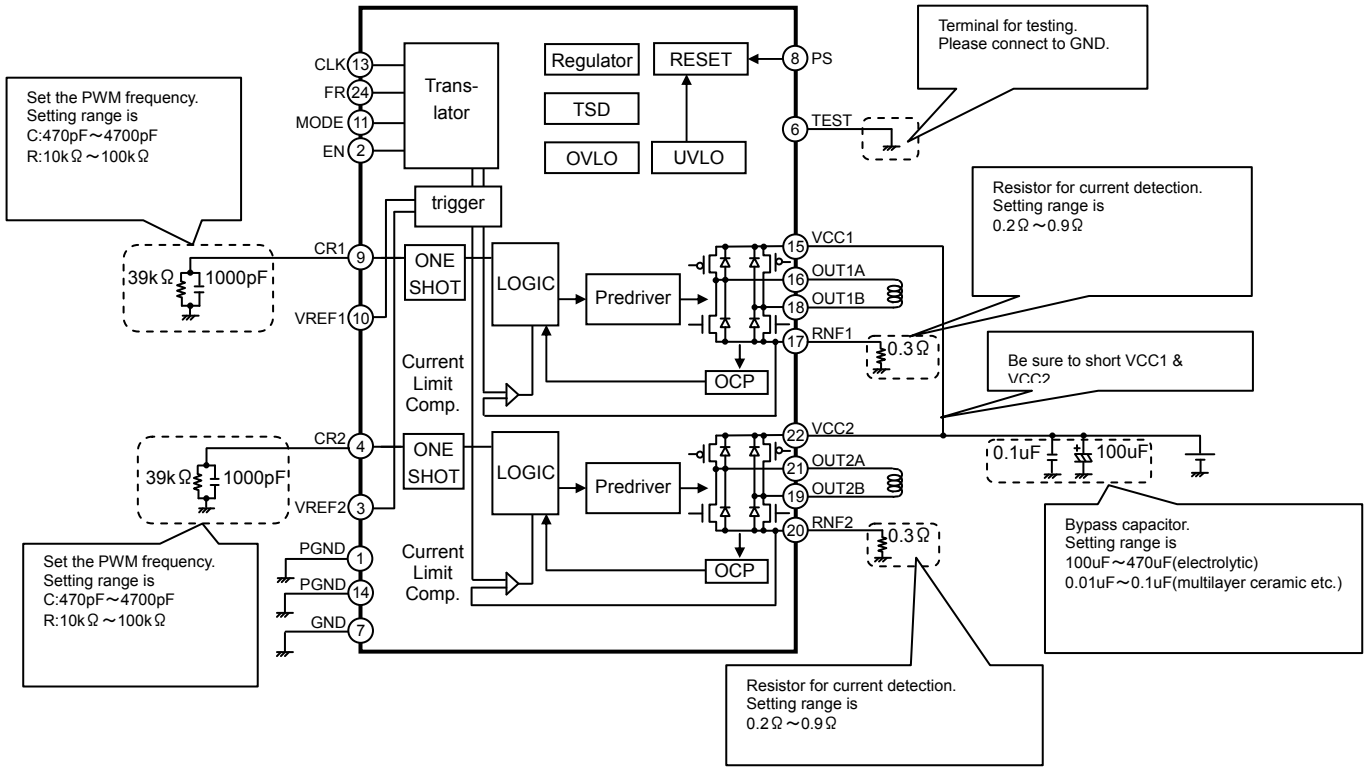


Fig.1 Block diagram & Application circuit diagram

●Points to notice for terminal description

○CLK(pin13)／Clock input terminal for advancing the electrical angle

CLK is reflected at rising edge. The Electrical angle advances by one for each CLK input.
Motor's misstep will occur if noise is picked up at the CLK terminal, so please design the pattern in such a way that there is no noise plunging.

○MODE(pin11)／Motor excitation mode setting terminal

Set the motor excitation mode.

MODE	Excitation mode
L	FULL STEP
H	HALF STEP A

○FR(pin24)／Motor rotating direction setting terminal

Set the motor's rotating direction. Change in setting is reflected at the CLK's rising edge immediately after the change in setting

CW_CCW	Rotating direction
L	Clockwise (CH2's current is outputted with a phase lag of 90° in regard to CH1's current)
H	Counter Clockwise(CH2's current is outputted with a phase lead of 90° in regard to CH1's current)

○ENABLE(pin2)／Output enable terminal

Turn off forcibly all the output transistors (motor output is open).
At the time of ENABLE=L, electrical angle or operating mode is maintained even if CLK is inputted.
Please be careful because the electrical angle at the time of ENABLE being released (ENABLE=L→H) is different from the released occasion at the section of CLK=H and from the released occasion at the section of CLK＝L .

ENABLE	Motor output
L	OPEN (electrical angle maintained)
H	ACTIVE

○PS(pin8)／Power save terminal

PS can make circuit standby state and make motor output OPEN. In standby state, translator circuit is reset (initialized) and electrical angle is initialized.
Please be careful because there is a delay of 40μs(Max.) before it is returned from standby state to normal state and the motor output becomes ACTIVE.

PS	State
L	Standby state (RESET)
H	ACTIVE

The electrical angle (initial electrical angle) of each excitation mode immediately after RESET is as follows Please be careful because the initial state at the time of FULL STEP is different from HALF STEP.

Excitation mode	Initial electrical angle
FULL STEP	45°
HALFSTEP A	0°

●Protection Circuits

○Thermal shutdown (TSD)

This IC features an integrated thermal shutdown for protection against thermal destruction. When the IC's chip temperature rises above 175°C (Typ.), the motor output is forced open. When the temperature returns to 150°C or less (Typ.), the IC automatically resumes normal operation. However, even if TSD has engaged, the IC may become damaged if heat continues to be absorbed from an external source.

○Over-current protection (OCP)

This IC features an integrated over-current protection circuit to protect against destruction if the motor outputs are shorted to one another, if VCC is shorted to the motor output, or if the motor output is shorted to GND. The circuit latches the motor output open if current flows above the maximum threshold for 4 μS (Typ.), and is disengaged when the IC is power-cycled or if the PS terminal is reset. The OCP circuitry is designed only to protect the IC from irregular conditions (such as motor output shorts) and is not designed to be used as an active security device for the application. Therefore, applications should not be designed under the assumption that this circuitry will engage. After OCP has engaged, if irregular conditions continue after a power cycle or PS pin reset, OCP may engage repeatedly, causing the IC to generate heat or otherwise suffer damage. If the inductance of the IC's input/output wiring is large (e.g., due to long trace length), overload current may flow into the wiring before OCP engages, causing a jump in voltage on the input/output pin that may exceed the IC's absolute maximum rating and damage the IC. Additionally, if the IC conducts a current through the output that is larger than the specified output current rating but lower than the OCP threshold, the IC may heat up beyond its maximum rating (Tjmax = 150°C) and destroy itself. Therefore, ensure that the set output current does not exceeds the IC's maximum output rating.

○Under-voltage lockout (UVLO)

This IC features an integrated under-voltage lockout function to prevent against output when powered by an insufficient supply voltage. If the supply voltage connected to the VCC terminal drops below 15 V (Typ.), the motor output is forced open. This switching voltage threshold has a hysteresis of 1 V (Typ.) to prevent malfunction due to noise on the input. This circuit does not function in power-save mode. Also, when driving the IC in serial (CLK-in) mode, the output angle is reinitialized to the default angle upon release of the UVLO circuitry.

○Over-voltage lockout (OVLO)

This IC features an integrated over-voltage lockout function to prevent against output when powered by a supply voltage exceeding the rated input voltage range. If the supply voltage connected to the VCC terminal reaches 32 V (Typ.), the motor output is forced open. This switching voltage threshold has a hysteresis of 1 V (Typ.) and a noise-masking period of 4 µs (Typ.) to prevent malfunction due to noise on the input. Although the IC features this integrated protection device, it may still be destroyed if the input voltage exceeds the IC's absolute maximum ratings. This circuit does not operate in power-save mode.

○Ghost supply prevention

This IC features integrated ghost supply protection circuitry, which prevents the IC from being powered by a logic input when the power supply is disconnected or grounded. This circuitry prevents current from flowing through the integrated ESD protection diodes (located between logic input pins and the VCC pin), ensuring that the IC itself or any other peripherals connected to the VCC pin cannot be powered by an input signal on any logic terminals. Therefore, the circuit will not malfunction if a logic signal is input to the IC while the power supply is disconnected or grounded.

● Power dissipation

○ HTSSOP-B24 package

The HTSSOP-B24 package features a heat-radiating metal slag mounted on the backside of the IC. Ensure that the PCB design incorporates large areas of copper to facilitate heat dissipation as much as possible. As the heat slag is shorted with the substrate of the IC die, ensure that the slag is connected to GND. Connecting the slag to a potential other than GND will cause the chip to malfunction. Also ensure that the backside of the chip is completely and firmly soldered onto the PCB. The ratings specified in this sheet assume the IC has been properly mounted and soldered, and that the PCB has been adequately designed to facilitate heat dissipation.

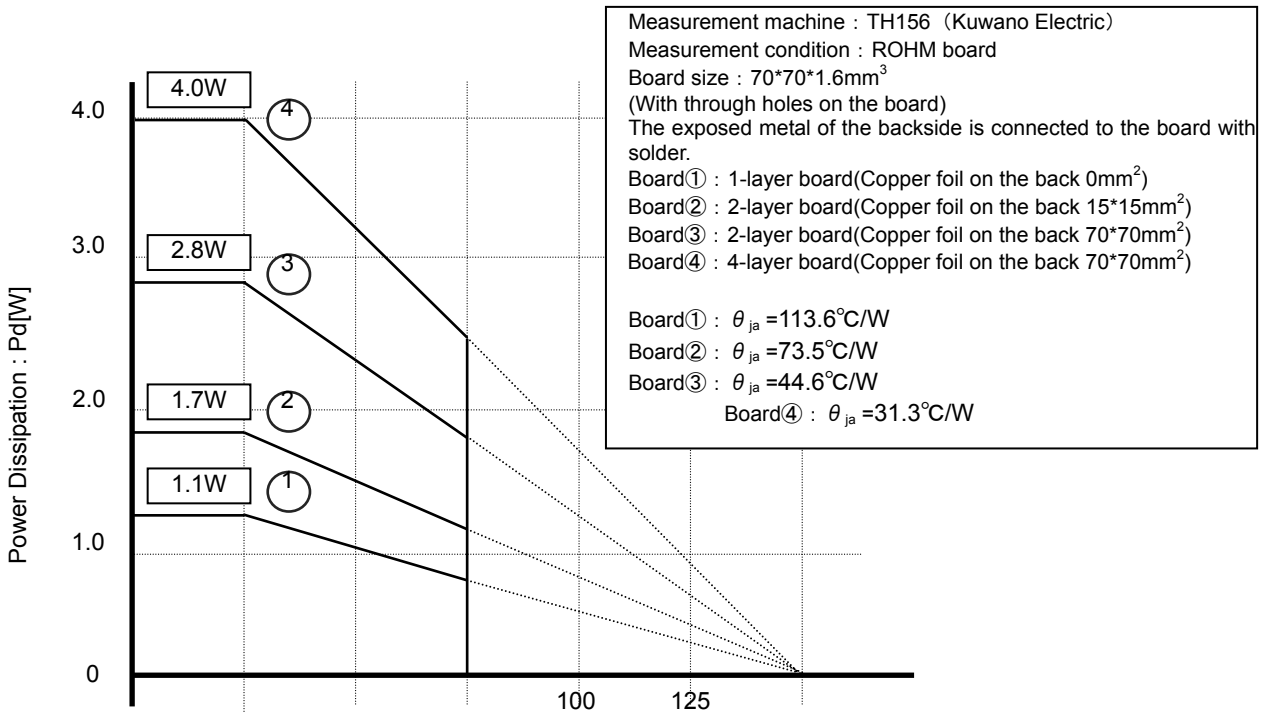


Fig.2 HTSSOP-B24 Derating curve

●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

(2) Power supply polarity

Connecting the power supply with a reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external diode can be connected to the input for extra protection.

(3) Power supply lines

PCB design should allow for low-impedance GND and supply lines. To minimize noise on these lines, the GND section and supply lines of the digital and analog blocks should be routed separately on the PCB. Furthermore, for all power IC supply terminals, a capacitor should be connected between the power supply and GND terminal. If using electrolytic capacitors, note that their capacitance values may be reduced at lower temperatures.

(4) GND potential

The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.

(5) Backside heat slag

The metal heat slag integrated on the backside of the IC is connected internally with the backside of the IC die. Therefore, it should always be connected to GND. Connecting to any other potential may cause malfunction or destruction of the IC.

(6) Thermal design

Use a thermal design that allows for a sufficient margin for the package's rated power dissipation (Pd) under actual operating conditions. Keep in mind that the packaging of this IC series has been designed with an exposed heat slag on the backside of the package, and that this heat slag should be soldered completely to as broad a GND pattern as possible (on both the base fin of the slag as well as the entire backside) to improve heat dissipation.

(7) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.

(8) Operation in strong electromagnetic fields

Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

(9) ASO – Area of safe operation

When using the IC, ensure that operating conditions do not exceed absolute maximum ratings or ASO of the output transistors.

(10) Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit, which is designed to force the motor output open if the IC's internal temperature exceeds Tjmax = 150°C. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

TSD on temperature [°C] (Typ.)	Hysteresis Temperature [°C] (Typ.)
175	25

(11) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(12) Input terminal of IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

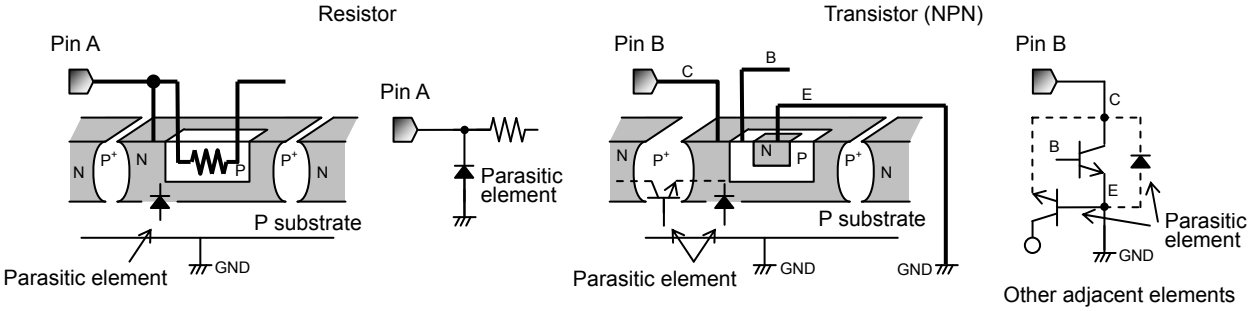


Fig.3 Example of Monolithic IC Structure

(13) Ground wiring patterns

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

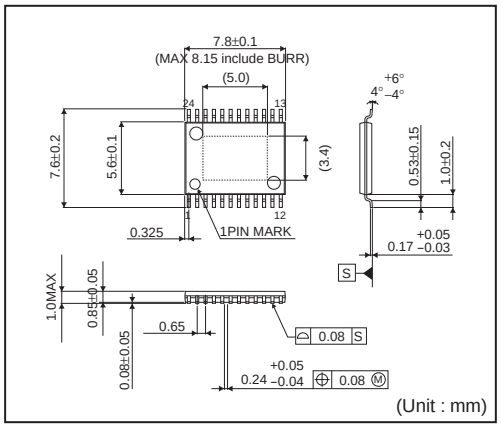
(14) TEST Terminal

Connect the TEST pin to GND during operation.

●Ordering part number

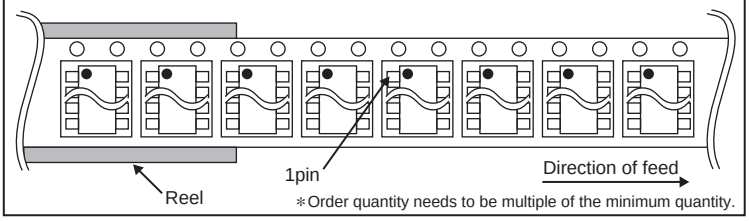
B D 6 3 8 0 1 E F V	-	E 2
形名	パッケージ EFV=HTSSOP-B24	包装、フォーミング仕様 E2: リール状エンボステーピング

HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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