System Power Supply ICs for TVs

Built-in FET Synchronous Rectification Type DC/DC converters H^{3}Reg^{TM} Type

BD95830MUV

No.11034EBT08

●Description

BD95830MUV is a 2ch switching regulator that can generate low output voltages (0.8V to 5.5V) at the large input voltage range (7.5 to 15V). Space-saving and high efficient switching regulator can be achieved due to built-in N-MOSFET power transistor. The IC also incorporates a new technology called H^{3}Reg^{TM}, a Rohm proprietary control method which facilitates ultra-high transient response against changes in load. For protection and ease of use, the IC also incorporates soft start, and short circuit protection with timer latch functions. This switching regulator is designed for power supplies for Digital AV Equipments.

●Features

1) 2ch H^{3}Reg^{TM} DC/DC converter synchronous controller
2) Built-in N-MOSFET (High side:75mΩ, Low side:50mΩ)
3) Built-in Thermal Shut Down (TSD), Under-Voltage Lock-Out (UVLO), Adjustable Over Current Protection (OCP) : detected Low side FET Ron, Over Voltage Protection (OVP), Short Circuit Protection (SCP)
4) Soft start function to minimize rush current during startup
5) VQFN032V5050 package
6) Built-in 5V power supply for FET drive
7) Integrated bootstrap diode
8) Switching frequency : 400kHz～800kHz（depend on input-output condition）

●Applications

LCD-TV, PDP-TV, Set Top Box, Game Consoles, Desktop PCs

●**Maximum Absolute Ratings** (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Input Voltage	VIN1, VIN2, VINS	15.1 *1*2	V
BOOT Voltage	BOOT1,BOOT2	21.1 *1*2	V
BOOT-SW Voltage	BOOT1-SW1, BOOT2-SW2	7 *1*2	V
Output Voltage	VOUT1, VOUT2	7 *1*2	V
Output Feedback Voltage	FB1, FB2	VREG	V
VREG Voltage	VREG	7 *1*2	V
VCC Voltage	VCC	VREG	V
Logic Input Voltage	EN1, EN2	15.1 *1*2	V
Power Dissipation 1	Pd1	0.38 *3	W
Power Dissipation 2	Pd2	0.88 *4	W
Power Dissipation 3	Pd3	3.26 *5	W
Power Dissipation 4	Pd4	4.56 *6	W
Operating Temperature Range	Topr	-20～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 3.04mW/℃ for each increase in Ta of 1℃ over 25℃ (when don't mounted on a heat radiation board)
*4 Reduced by 7.04mW/℃ for increase in Ta of 1℃ over 25℃.
(when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB(1 layer), copper foil area : 20.2mm^2)
*5 Reduced by 26.11mW/℃ for increase in Ta of 1℃ over 25℃.
(when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB(4 layer), copper foil area: 20.2mm^2, 2-3layer: 5505mm^2)
*6 Reduced by 36.5mW/℃ for increase in Ta of 1℃ over 25℃.
(when mounted on a board 74.2mm × 74.2mm × 1.6mm Glass-epoxy PCB(4 layer), copper foil area: 5505mm^2)

●**Operating Conditions** (Ta=25℃)

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Input Voltage	VIN1, VIN2, VINS	7.5	15	V
BOOT Voltage	BOOT1, BOOT2	4.5	21	V
SW Voltage	SW1, SW2	-0.7	15	V
BOOT-SW Voltage	BOOT1-SW1, BOOT2-SW2	4.5	5.5	V
Logic Input Voltage	EN1, EN2	0	15	V
Output Voltage	VOUT1, VOUT2	0.8	5.5	V
MIN ON TIME	tonmin	-	100	ns

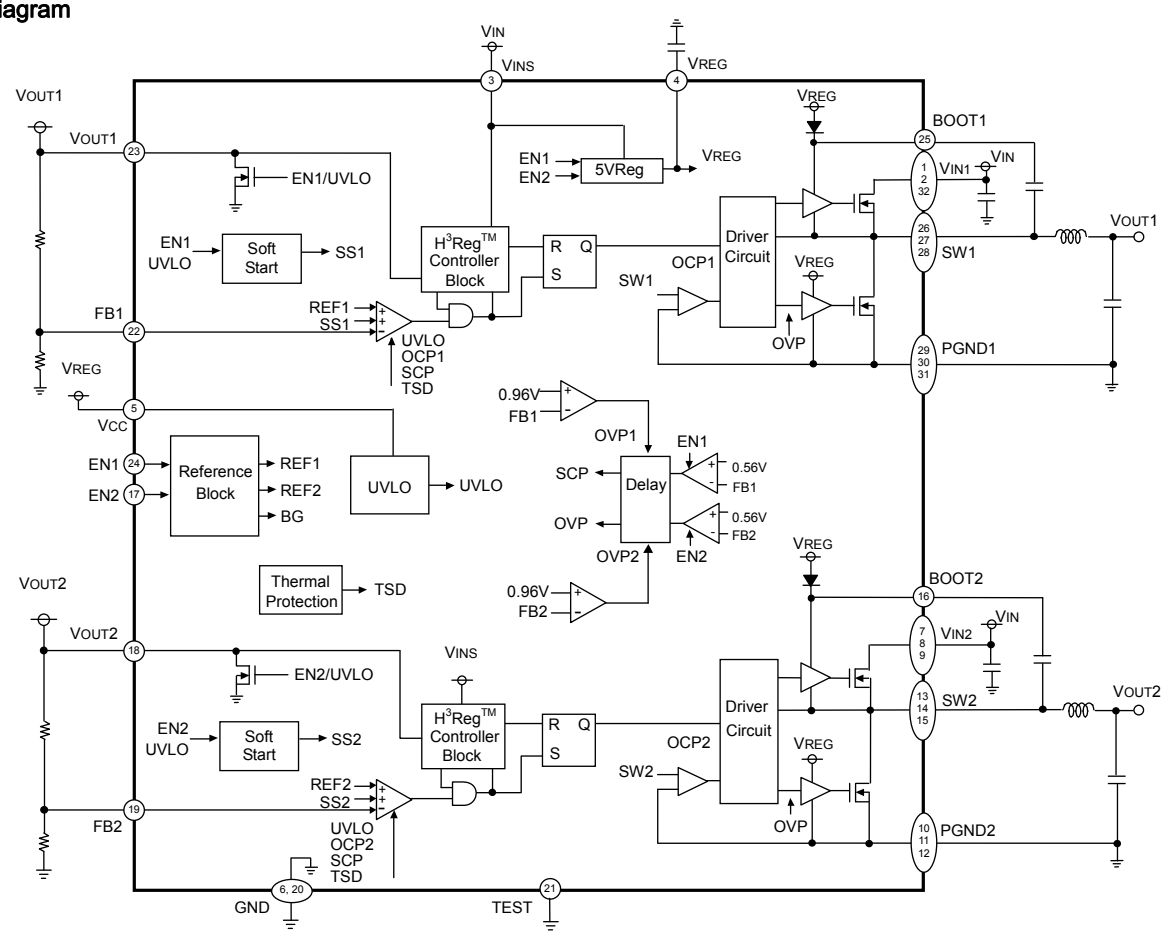
☆This product should not be used in a radioactive environment.

●Electrical Characteristics

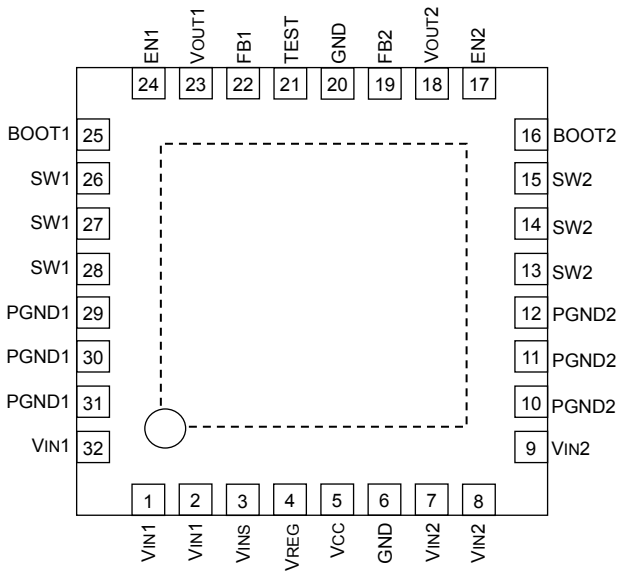
(Unless otherwise noted, Ta=25℃ V_{CC}=V_{REG}, V_{IN}1=V_{IN}2=V_{INS}=12V, V_{EN}1=V_{EN}2=3V, V_{OUT}1=V_{OUT}2=1.8V)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
[Whole Device]						
VIN Bias Current	I_{IN}	-	1.7	2.2	mA	
VIN Standby Current	I_{IN_stb}	-	0	10	μA	V_{EN}1=V_{EN}2=0V
EN Low Voltage 1,2	$V_{EN\_low1,2}$	GND	-	0.3	V	
EN High Voltage 1,2	$V_{EN\_high1,2}$	2.2	-	15	V	
EN Pull-down resistance1,2	$R_{EN1,2}$	28	48	68	kΩ	
[5V Regulator]						
V_{REG} Standby Voltage	V_{REG_stb}	-	-	0.1	V	V_{EN}1=V_{EN}2=0V
V_{REG} Output Voltage	V_{REG}	4.8	5.0	5.2	V	V_{INS}=7.5V to 15V I_{REG}=10mA
Maximum Current	I_{REG}	10	-	-	mA	
[Under-Voltage Lock-Out]						
UVLO Threshold Voltage	V_{CC_UVLO}	4.0	4.3	4.6	V	V_{REG}:Sweep up
UVLO Hysteresis Voltage	DV_{CC_UVLO}	100	160	220	mV	V_{REG}:Sweep down
[OVP Block]						
OVP Threshold Voltage 1,2	V_{OVP}	0.86	0.96	1.06	V	
OVP delay time	t_{OVP}	-	1.4	-	ms	
[H^3Reg^{TM} Control Block]						
ON Time1,2	t_{on1}	200	255	310	ns	
MIN OFF Time 1,2	$t_{offmin1}$	300	550	-	ns	
[FET Driver Block]						
High side FET ON Resistance 1,2	$R_{ON\_high1,2}$	-	75	120	mΩ	
Low side FET ON Resistance 1,2	$R_{ON\_low1,2}$	-	50	75	mΩ	
[Over Current Protection Block]						
Current Limit 1,2	$I_{lim1,2}$	3	4	5	A	
[Output Voltage Detection Block]						
FB threshold Voltage1,2	$V_{FB1,2}$	0.788	0.8	0.812	V	
Soft Start Time1,2	T_{SOFT1}	-	1.3	-	ms	
FB Input Current 1,2	$I_{FB1,2}$	-1	-	1	μA	
VOUT Discharge Current 1,2	$I_{VOUT1,2}$	5	10	-	mA	V_{OUT}=1V, V_{EN}=0V V_{CC}=5V
[SCP Block]						
SCP Threshold Voltage 1,2	$V_{thscp1,2}$	0.48	0.56	0.64	V	
SCP delay time	t_{SVP}	-	1.4	-	ms	

●Block Diagram



●Pin Configuration



●Pin Function

PIN No.	PIN Name	PIN Function
1,2,32	VIN1	Power Supply Voltage Input Pin for 1ch.
3	VINS	Power Supply Voltage Sense Pin. Input Pin for VREG.
4	VREG	Reference Voltage Inside IC.
5	VCC	5V Power Supply Input Pin.
6,20	GND	Sense GND.
7-9	VIN2	Power Supply Voltage Input Pin for 2ch.
10-12	PGND2	Power GND for 2ch.
13-15	SW2	High side FET Source Pin 2.
16	BOOT2	High side FET Gate Driver Power Supply Pin 2.
17	EN2	Enable Input Pin 2. (0～0.3V:OFF, 2.2～15V:ON).
18	VOUT2	Output Voltage Sense / Discharge Pin 2.
19	FB2	Output Voltage Feedback Pin 2.
21	TEST	Pin for TEST. Connect to GND.
22	FB1	Output Voltage Feedback Pin 1.
23	VOUT1	Output Voltage Sense / Discharge Pin 1.
24	EN1	Enable Input Pin 1. (0～0.3V:OFF, 2.2～15V:ON).
25	BOOT1	High side FET Gate Driver Power Supply Pin 1.
26-28	SW1	High side FET Source Pin 1.
29-31	PGND1	Power GND for 1ch.
reverse	FIN	Exposed Pad, Connect to GND.

●Pin Descriptions

- EN1 / EN2

  When the input voltage on the EN pin reaches at least 2.2V, the switching regulator becomes active. At voltages less than 0.3 V, the switching regulator becomes inactive, and the input current drops to 10μA or less. Thus the IC can be controlled from 2.5V, 3.3V or 5V power supplies.
- V_{INS}

  The IC determines the duty cycles internally based upon the input voltage on this pin. Therefore, variations in voltage on this pin can lead to highly unstable operation. This pin also acts as the voltage input to the internal switching regulator block, and is sensitive to the impedance of the power supply. Attaching a bypass capacitor or RC filter on this pin as appropriate for the application is recommended.
- V_{REG}

  Reference voltage output pin. If at least 2.2V is supplied to either the EN1 or EN2 pin, the reference output is switched on. This pin supplies 5.0V at up to 10mA. Inserting a 2.2μF capacitor (with a X5R or X7R rating) between the VREG and GND pins is recommended.
- V_{CC}

  This is the power supply pin for all internal circuitry. This pin can be supplied directly by a 5V source, or connect with the V_{REG} pin.
- GND

  This is the ground pin for all internal analog and digital power supplies.
- $V_{OUT}1$ / $V_{OUT}2$

  This is the output voltage sense pin; this pin features an integrated discharge FET used to discharge the output capacitor when status is set to OFF.
- FB1 / FB2

  This is the output feedback pin. FB is compared with REF (Refer to p.8) of IC. Set the output voltage with total about 10kΩ resistances.
- $V_{IN}1$ / $V_{IN}2$

  This is the input voltage pin for Power supply. Connect a input capacitor as appropriate for the ripple current and the load to the pin directly.
- BOOT1 / BOOT2

  This pin supplies voltage used for driving the high-side FET. Inserting a 0.1μF ceramic capacitor between the pin and SW pins is recommended. Maximum absolute ratings are 21V from GND and 5.5V from SW. BOOT voltage swings between (V_{IN} + V_{REG}) and V_{REG} during active operation.
- SW1 / SW2

  This pin is connected to inductor (L). Maximum absolute rating is 15V from GND. SW voltage swings between V_{IN} and PGND.
- PGND1 / PGND2

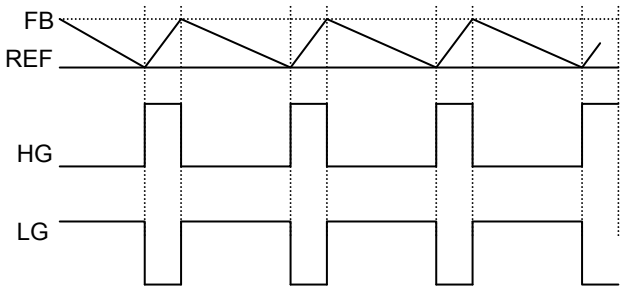
  This pin acts as the ground connection to the source of the low-side FET.
- TEST

  This is the pin for TEST. Connect to GND Pin.

●Explanation of Operation

The BD95830MUV is a 2ch switching regulator controller incorporating ROHM's proprietary H^3Reg^{TM} CONTROLLA control system. When VOUT drops due to a rapid load change, the system quickly restores VOUT by extending the ON time interval.

H^3Reg^{TM} control
(Normal operation)

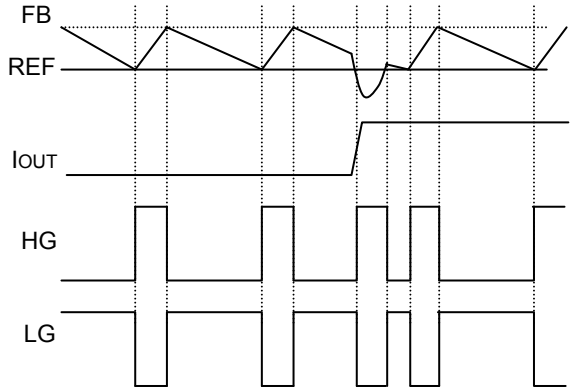


When FB falls below the threshold voltage (REF), a drop is detected, activating the H^3Reg^{TM} CONTROLLA system.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \text{ [sec]} \cdots (1)$$

HG(Gate of High side FET) output is determined by the formula above.
LG(Gate of Low side FET) output operates until FB voltage falls below REF voltage after HG becomes OFF.

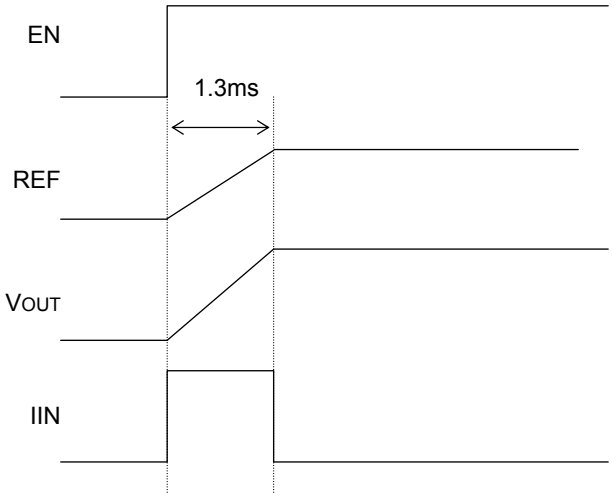
(VOUT drops due to a rapid load change)



When FB (VOUT) drops due to a rapid load change, and the voltage remains below REF after the frequency becomes high, the system quickly restores VOUT by extending the tON time, improving transient response.

●Timing Chart

・Soft Start Function



Soft start is utilized when the EN pin is set high. Current control takes effect at startup, enabling a moderate "ramping start" on the output voltage. Soft start time is 1.3ms (typ). And rush current is determined via formula (2) below.

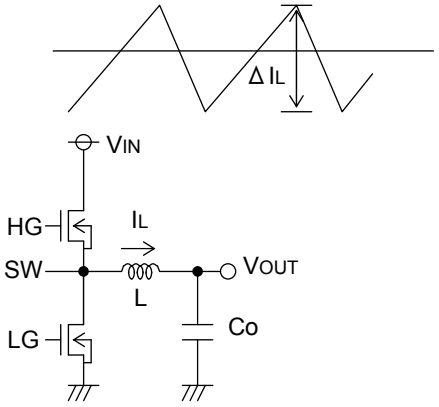
Rush current

$$I_{IN} = \frac{Co \times V_{OUT}}{1.3ms} \text{ [A]} \cdots (2)$$

(Co: All capacitors connected with VOUT)

●External Component Selection

1. Inductor (L) selection



Output Ripple Current

The inductance value has a major influence on output ripple current. As formula (3) below indicates, the greater the inductance or switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f} \quad [A] \cdots (3)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}max. \quad [A] \cdots (4)$$

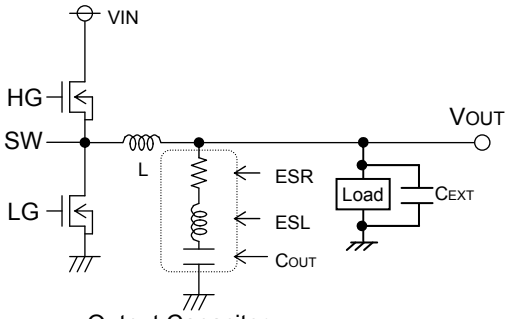
$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [H] \cdots (5)$$

(ΔI_L: output ripple current, f: switching frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. When selecting an inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor's rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2. Output Capacitor (C_{OUT}) Selection



Output Capacitor

Output Capacitor (C_{OUT}) has a considerable influence on output voltage regulation due to a rapid load change and smoothing output ripple voltage. Determine the capacitor by considering the value of capacity, the equivalent series resistance, and equivalent series inductance. Also, make sure the capacitor's voltage rating is high enough for the set output voltage (including ripple).

Output ripple voltage is determined as in formula (6) below.

$$\Delta V_{OUT} = \Delta I_L / (8 \times C_{OUT} \times f) + ESR \times \Delta I_L + ESL \times \Delta I_L / T_{ON} \cdots (6)$$

(ΔI_L: Output ripple current; ESR: Equivalent series resistance, ESL: Equivalent series inductance)

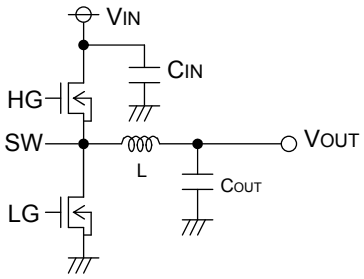
Also, give due consideration to the conditions in formula (7) below for output capacitance, bearing in mind that output rise time must be established within the soft start time frame. As output capacitor capacitance, bypass capacitor will be connected to output load side (C_{EXT}, figure above). Please set the over current detection value with regards to these capacitance.

$$C_{OUT} \leqq \frac{1.3ms \times (Limit - I_{OUT})}{V_{OUT}} \cdots (7)$$

Limit: Over current detection
I_{OUT}: Output current

Note: an improper output capacitor may cause startup malfunctions.

3. Input Capacitor (C_{IN}) Selection



Input Capacitor

In order to prevent transient spikes in voltage, the input capacitor selected must have a low enough ESR resistance to fully support a large ripple current on the output. The formula for ripple current IRMS is given in equation (8) below:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad [A] \cdots (8)$$

Where $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low-ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. Output Voltage Setting

The IC will try to maintain output voltage such that REF≒V_{FB}.

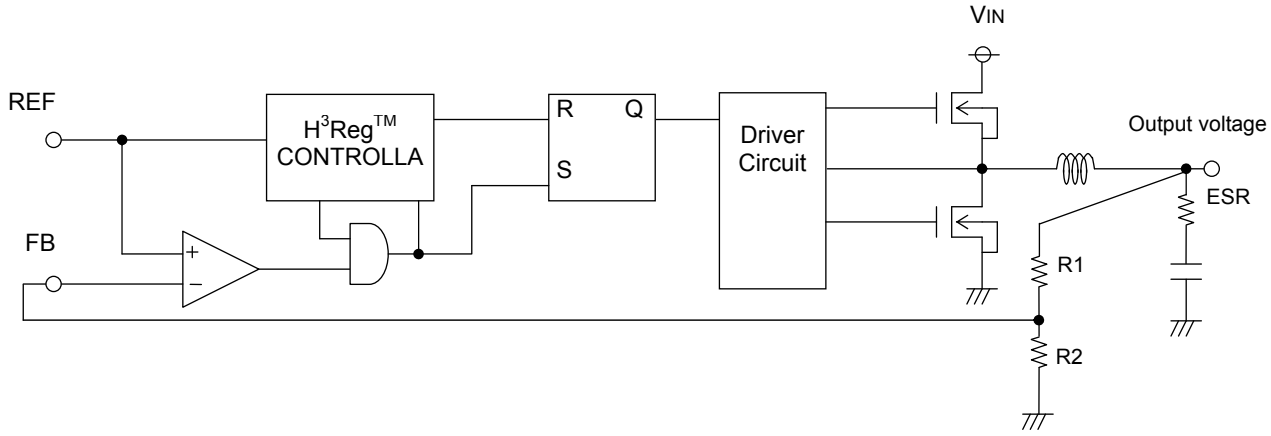
However, the actual output voltage will also reflect the average ripple voltage value.

The output voltage is set via a resistive voltage divider between the output and the FB pin. The formula for output voltage is given in (9) below:

$$\text{Output voltage} = \frac{R1+R2}{R2} \times REF + \Delta V_{OUT} \quad [V] \quad \cdot\cdot\cdot (9)$$

$$REF = 0.8 - (\text{ON duty} \times 0.1) \quad [V] \quad \cdot\cdot\cdot (10)$$

$$\text{ON duty} = \frac{V_{OUT}}{V_{IN}} \quad \cdot\cdot\cdot (11)$$



5. Relationship between output voltage and Ton duration

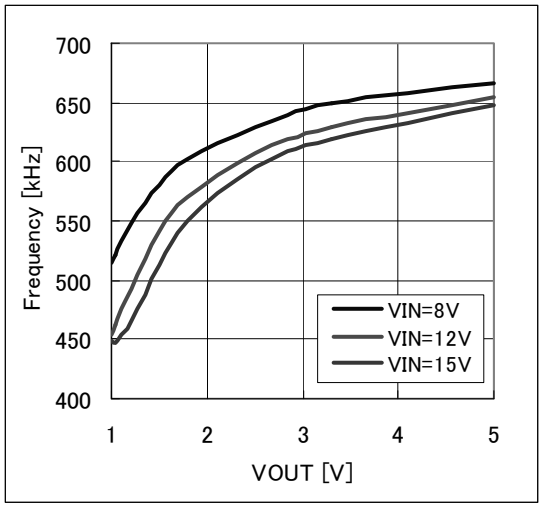
Both 1ch and 2ch of BD95830MUV are synchronous rectification type of switching controllers operated at fixed-frequency. The Ton duration for each channel depends on the output voltage settings, as described by the following formulas.

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 1.34\mu + 70n \text{ [ns]} \cdots (12)$$

Thus from the above Ton duration, the frequency of the applied condition is

$$\text{Frequency} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{T_{ON}} \text{ [kHz]} \cdots (13)$$

However with actual applications, there exists a rising and falling time of the SW and the switching speed, which may vary the above parameters. Thus please also verify those parameters experimentally.



6. Relationship between output current and frequency

BD95830MUV is a fixed-Ton type of switching controller. When the output current increases, the switching loss of the coil and MOSFET also increases and hence the switching frequency speeds up.
The loss of the coil and MOSFET is determined as

① Loss of coil = $I_{OUT}^2 \times DCR$

② Loss of high-side MOSFET = $I_{OUT}^2 \times Ronh \times \frac{V_{OUT}}{V_{IN}}$

③ Loss of low-side MOSFET = $I_{OUT}^2 \times Ronh \times (1 - \frac{V_{OUT}}{V_{IN}})$

(Ronh : On-resistance of high-side MOSFET, Ronn : On resistance of low-side MOSFET,
ESR : C_{OUT} Equivalent series resistance)

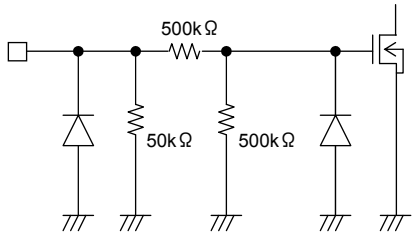
Taking the above losses into the frequency equation, then T (=1/Freq) becomes

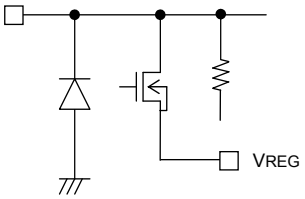
$$T\ (=1/Freq) = \frac{V_{IN} \times I_{OUT} \times T_{ON}}{V_{OUT} \times I_{OUT} + ① + ② + ③} \cdots (14)$$

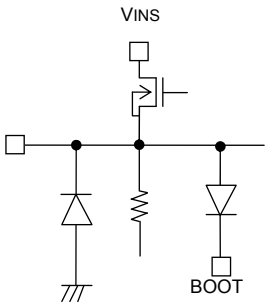
However since the parasitic resistance of the layout pattern exists in actual applications and affects the parameter, please also verify experimentally.

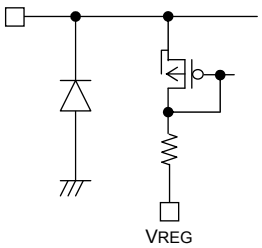
●I/O Equivalent Circuits

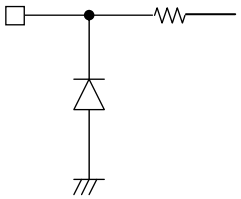
EN1, EN2	VINS	VREG
VCC	FB1, FB2	VOUT1, VOUT2
VIN1, VIN2	BOOT1, BOOT2	SW1, SW2

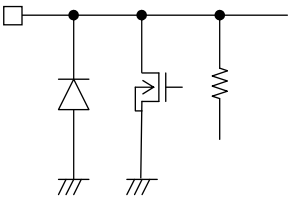


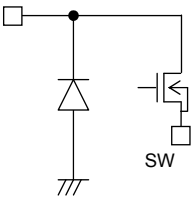


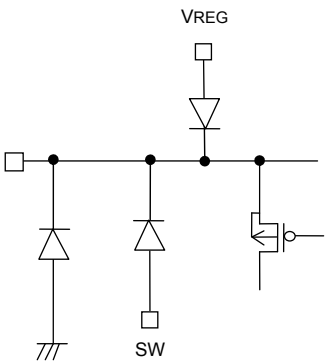


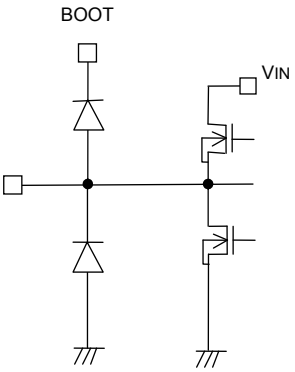












●Notes for use

(1) Absolute Maximum Ratings
Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

(2) Power Supply Polarity
Connecting the power supply in reverse polarity can cause damage to the IC. Take precautions when connecting the power supply lines. An external power diode can be added.

(3) Power Supply Lines
In order to minimize noise, PCB layout should be designed such that separate, low-impedance power lines are routed to the digital and analog blocks. Additionally, a coupling capacitor should be inserted between all power input pins and the ground terminal. If electrolytic capacitors are used, keep in mind that their capacitance characteristics are reduced at low temperatures.

(4) GND voltage
The potential of the GND pin must be the minimum potential in the system in all operating conditions.

(5) Thermal design
Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

(6) Inter-pin Shorts and Mounting Errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

(7) Operation in Strong Electromagnetic Fields
Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

(8) ASO - Area of Safe Operation
When using the IC, ensure that operating conditions do not exceed absolute maximum ratings or ASO of the output transistors.

(9) Thermal shutdown (TSD) circuit
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

	TSD ON Temp. [℃] (typ.)	Hysteresis Temp. [℃] (typ.)
BD95830MUV	175	15

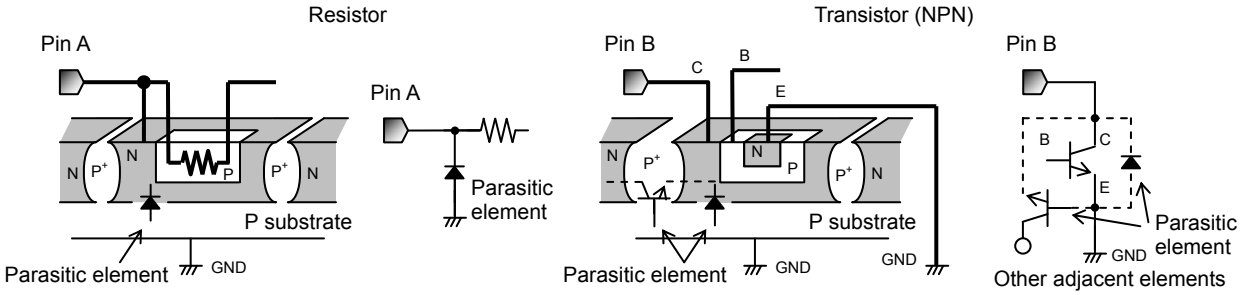
(10) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(11) Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

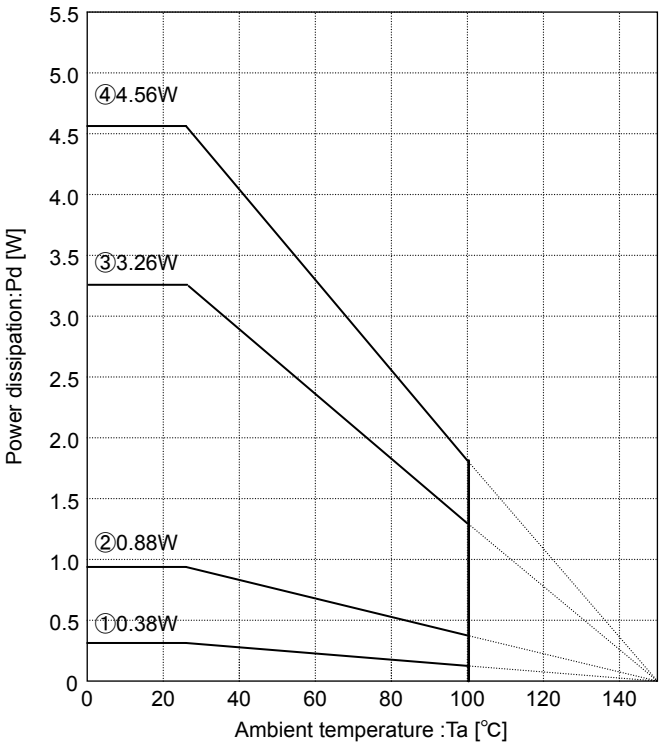


Example of IC structure

(12) Ground Wiring Pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

●Power Dissipation (VQFN032V5050)



① IC Only
θ j-a=328.9℃/W

② IC mounted on 1-layer board (with 20.2 mm^2 copper thermal pad)
θ j-a=142.0℃/W

③ IC mounted on 4-layer board (with 20.2 mm^2 pad on top layer, 5502 mm^2 pad on layers 2,3)
θ j-a=38.3℃/W

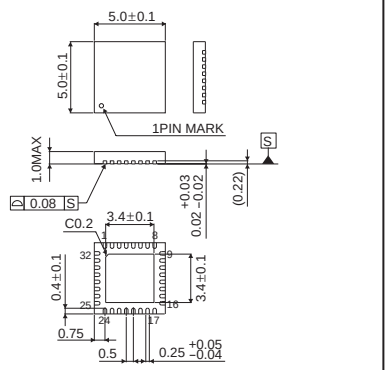
② IC mounted on 4-layer board (with 5505mm^2 pad on all layers)
θ j-a=27.4℃/W

●Type Designations (Selections) for Ordering

B	D	9	5	8	3	0	M	U	V	-	E	2

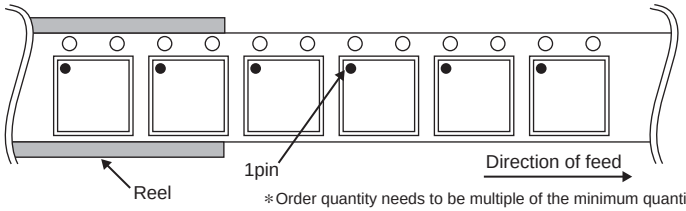
Part No.	Part No.	Package MUV : VQFN032V5050	Packaging and forming specification E2: Embossed tape and reel

VQFN032V5050



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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