

Standard LCD Segment Drivers



BU97950xxx Series MAX 280 segments (SEG35×COM8)

● **Features**

- Integrated RAM for display data (DDRAM):
35 x 8bit (Max 280 Segment)
- LCD drive output:
8 Common output, 35 Segment output
- Integrated Buffer AMP for LCD driving
- Integrated Oscillator circuit
- No external components
- Low power consumption design
- Independent power supply for LCD driving
- Integrated Electrical volume register (EVR) function

● **Key Specifications**

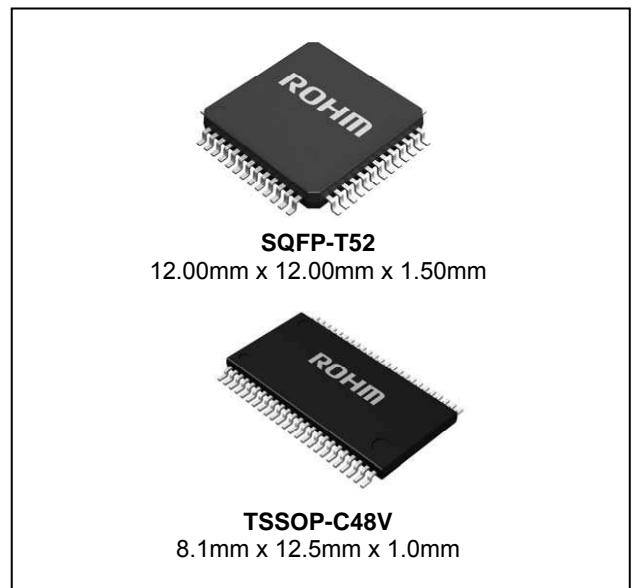
- Supply Voltage Range: +2.5V to +5.5V
- LCD drive power supply Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 280 Segments
- Display Duty: 1/8
- Bias: 1/4
- Interface: 2wire serial interface

● **Applications**

- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment
- etc.

● **Packages**

W (Typ.) x D (Typ.) x H (Max.)



● **Typical Application Circuit**

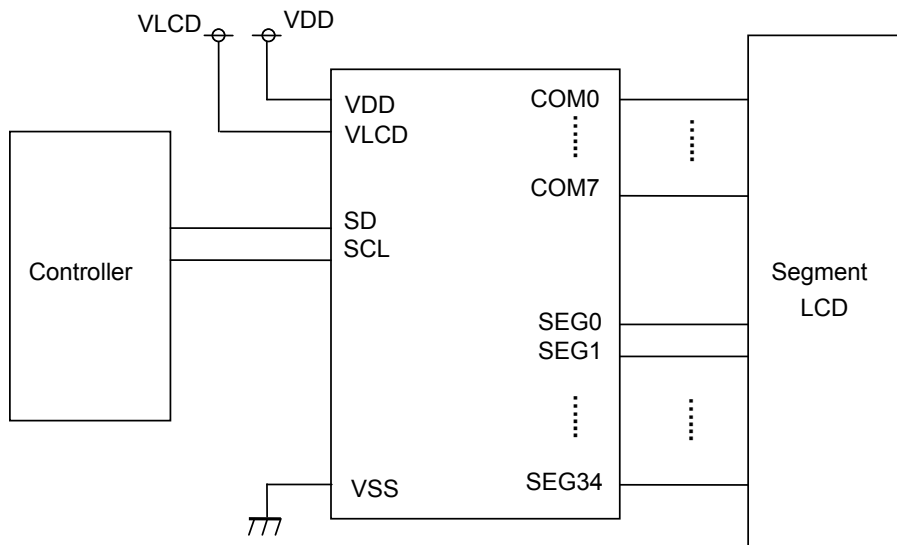


Figure 1. Typical application circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

●Block Diagrams / Pin Configurations / Pin Descriptions

BU97950FUV (TSSOP-C48V)

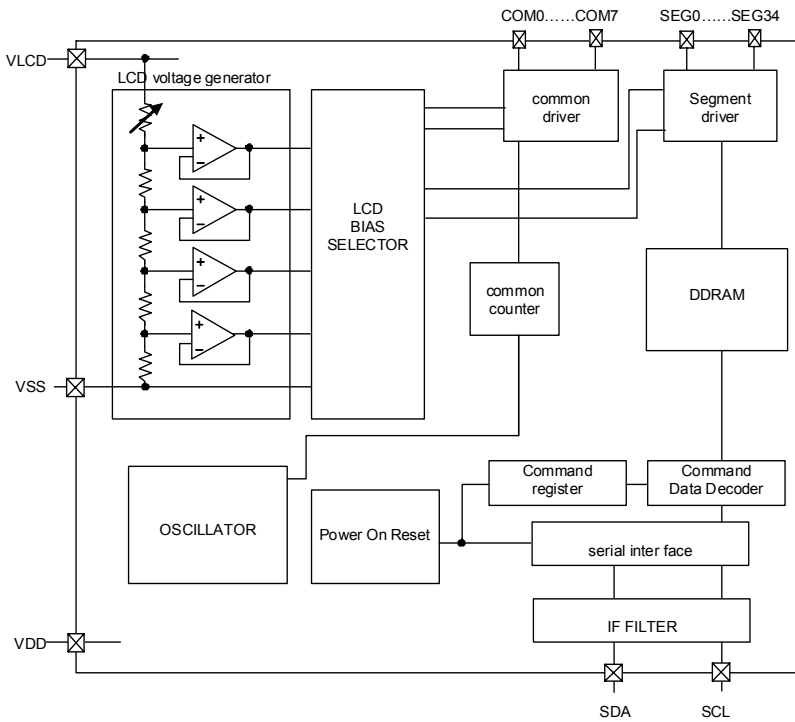


Figure 2. Block Diagram

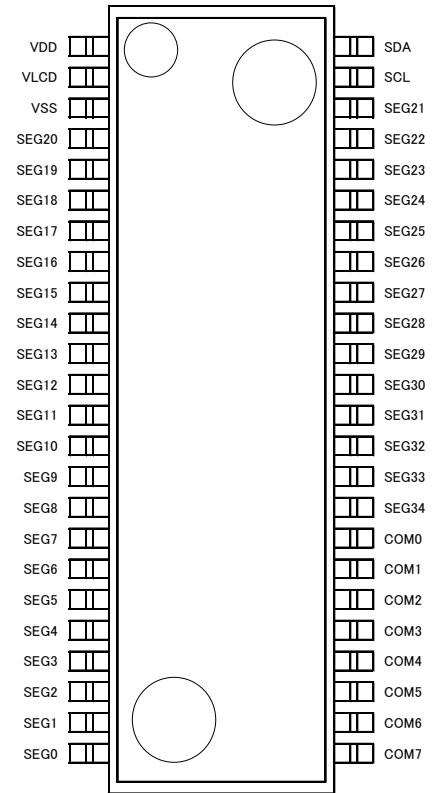


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Terminal	Terminal No.	I/O	Function
SDA	48	I/O	serial data input
SCL	47	I	serial data transfer clock
VSS	3	I	GND
VDD	1	I	Power supply
VLCD	2	I	Power supply for LCD driving
SEG0 to 35	4 to 24 33 to 46	O	SEGMENT output for LCD driving
COM0 to 7	25 to 32	O	COMMON output for LCD driving

●Block Diagrams / Pin Configurations / Pin Descriptions - continued

BU97950KS2 (SQFP-T52)

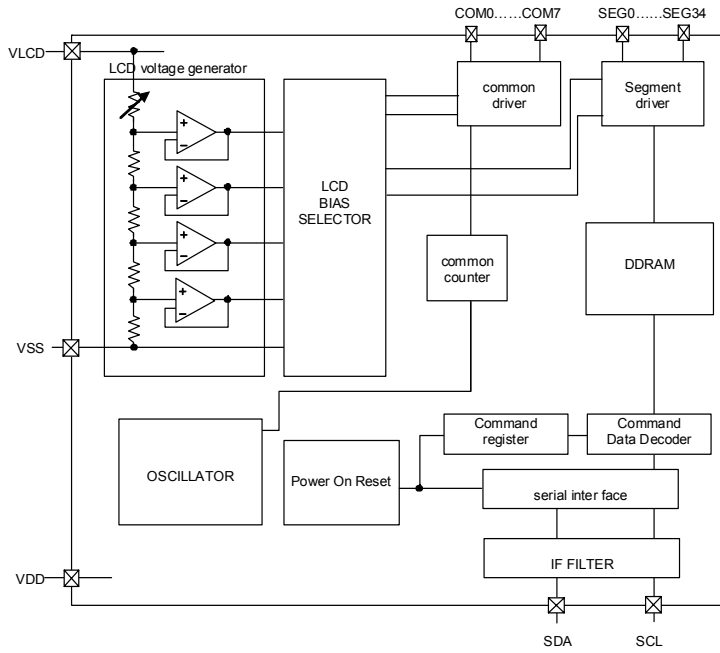


Figure 4. Block Diagram

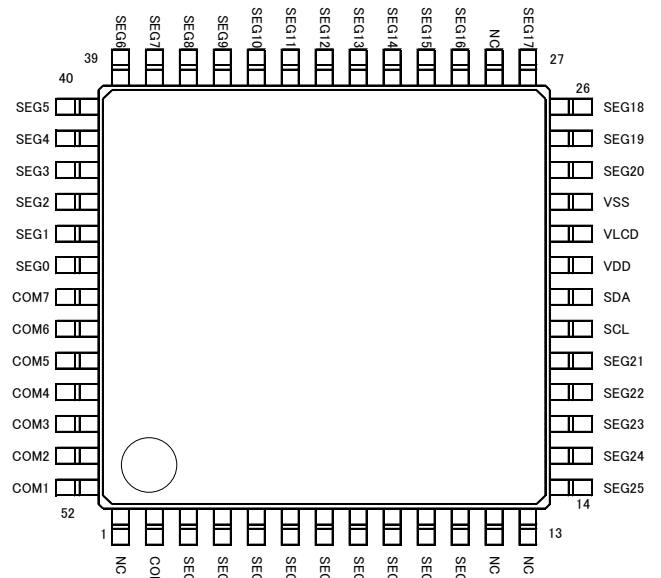


Figure 5. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Terminal	Terminal No.	I/O	Function
SDA	20	I/O	serial data input
SCL	19	I	serial data transfer clock
VSS	23	I	GND
VDD	21	I	Power supply
VLCD	22	I	Power supply for LCD driving
SEG0 to 35	3 to 11 24 to 27 29 to 45	O	SEGMENT output for LCD driving
COM0 to 7	2 46 to 52	O	COMMON output for LCD driving
NC	1,12,13,28	-	No connected

●Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 to +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 to +7.0	V	LCD drive voltage
Allowable loss	Pd	0.64	W	When use more than Ta=25 °C, subtract 6.4mW per degree. (BU97950FUV Package only)
		0.85	W	When use more than Ta=25 °C, subtract 8.5mW per degree. (BU97950KS2 Package only)
Input voltage range	VIN	-0.5 to VDD+0.5	V	
Operational temperature range	Topr	-40 to +85	°C	
Storage temperature range	Tstg	-55 to +125	°C	

*1 This product is not designed against radioactive ray.

●Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)

Parameter	Symbol	Limits			Unit	Remarks
		MIN	TYP	MAX		
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	2.5	-	5.5	V	LCD drive voltage

●Electrical Characteristics

DC Characteristics (VDD=2.5 to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
"H" level input voltage	VIH	0.7VDD	-	VDD	V	SDA,SCL
"L" level input voltage	VIL	VSS	-	0.3VDD	V	SDA,SCL
"H" level input current	IiH	-	-	1	μA	SDA,SCL
"L" level input current	IiL	-1	-	-	μA	SDA,SCL
LCD Driver on resistance	SEG	RON	-	3.5	kΩ	Iload=±10μA
	COM	RON	-	3.5	kΩ	
Standby current	Ist	-	-	5	μA	Display off, Oscillation off
Power consumption 1	IDD	-	2.5	15	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=80Hz 1/4 bias, Frame inversion
Power consumption 2	ILCD	-	10	20	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=80Hz 1/4 bias, Frame inversion

●Electrical Characteristics – continued

Oscillation Characteristics (VDD=2.5 to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to 85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Frame frequency	fCLK	56	80	104	Hz	FR = 80Hz setting, VDD=3.3V

MPU I/F Characteristics (VDD=2.5 to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	tr	-	-	0.3	μs	
Input fall time	tf	-	-	0.3	μs	
SCL cycle time	tSCYC	2.5	-	-	μs	
“H” SCL pulse width	tSHW	0.6	-	-	μs	
“L” SCL pulse width	tSLW	1.3	-	-	μs	
SDA setup time	tSDS	200	-	-	ns	
SDA hold time	tSDH	0	-	-	ns	
Buss free time	tBUF	1.3	-	-	μs	
START condition hold time	tHD;STA	0.6	-	-	μs	
START condition setup time	tSU;STA	0.6	-	-	μs	
STOP condition setup time	tSU;STO	0.6	-	-	μs	

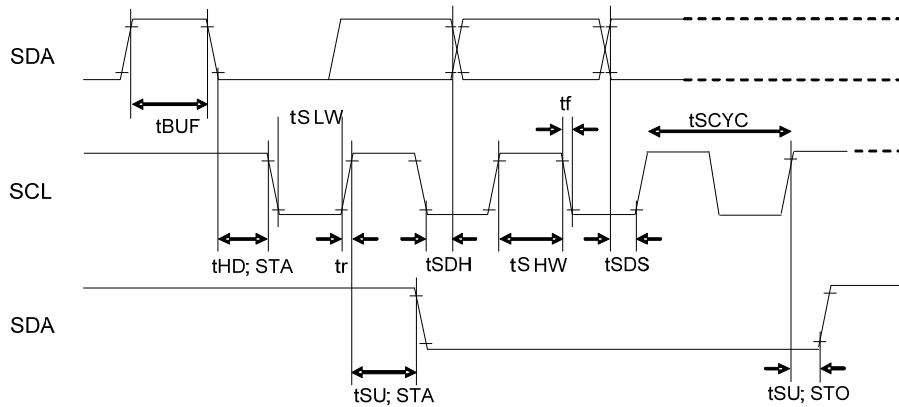


Figure 6. Serial Interface Timing

● I/O equivalent circuit

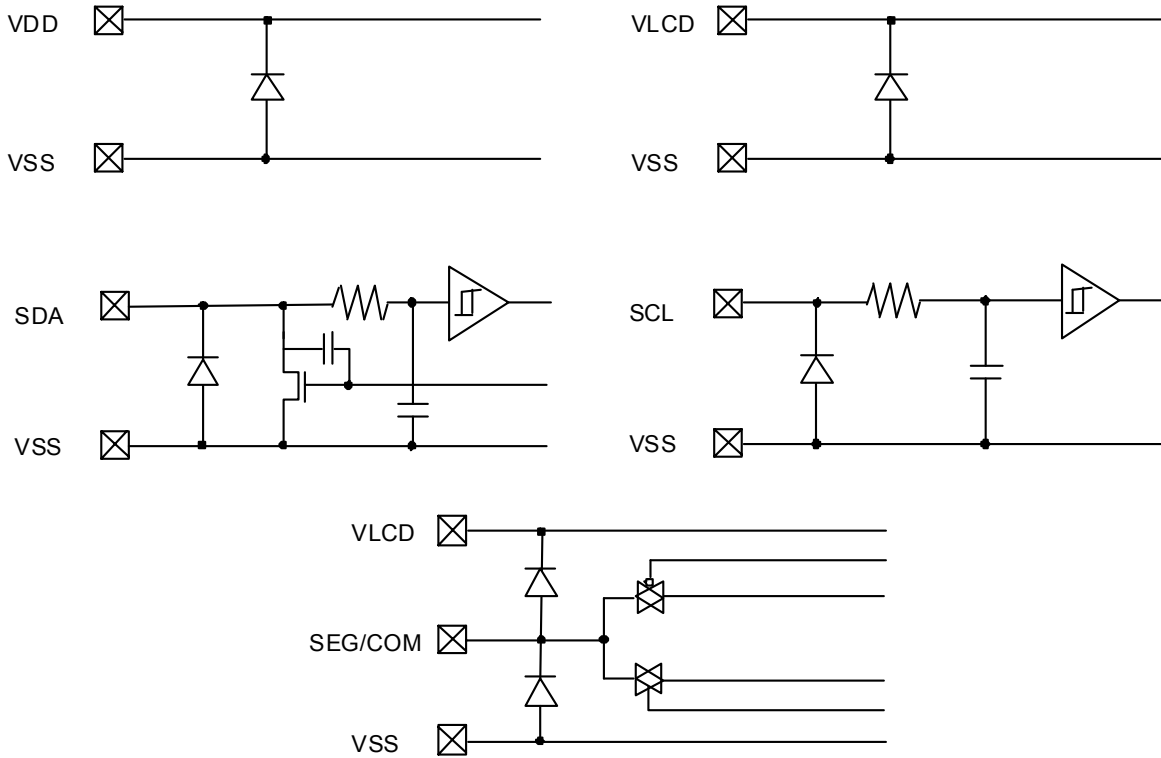


Figure 7. I/O equivalent circuit

● Example of recommended circuit

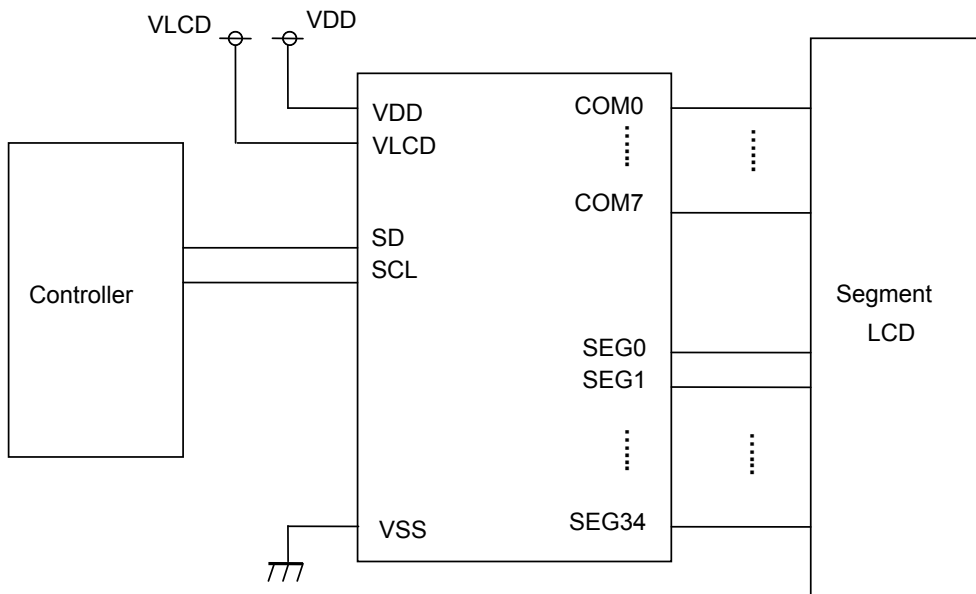


Figure 8. Recommended circuit example

●Function Description

○Command /Data transfer method

This device is controlled by 2wire serial signal (SDA, SCL).

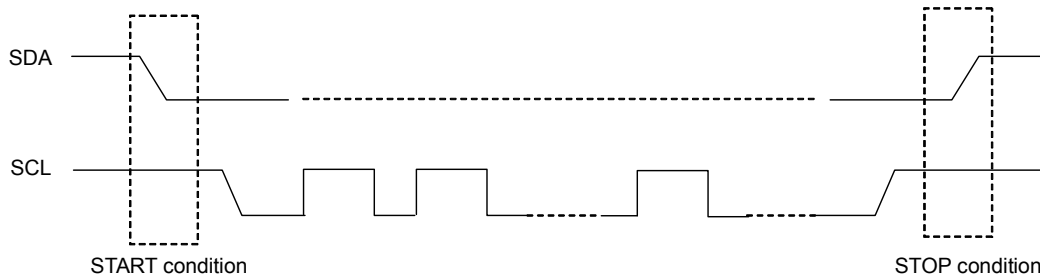


Figure 9. 2wire serial Command/Data transfer Format

It has to generate START and STOP condition in 2wire serial interface transfer method.

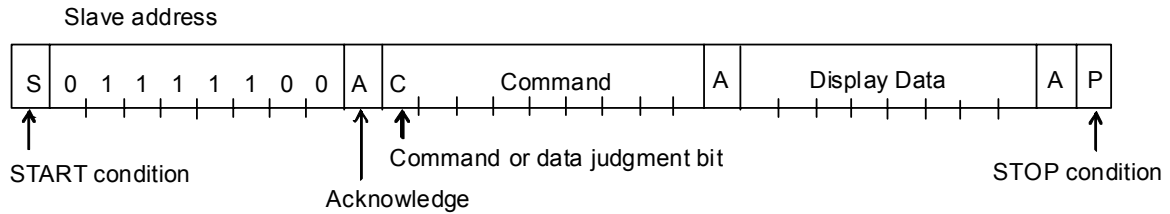


Figure 10. Interface protocol

Method of how to transfer command and data is shown as follows.

- 1) Generate "START condition".
- 2) Issue Slave address.
- 3) Transfer command and display data.

○Acknowledge

Data format is 8bits and return Acknowledge after transfer 8bits data.

When SCL 8th='L' after transfer 8bit data (Slave Address, Command, Display Data), output 'L' and open SDA line.

When SCL 9th='L', stop output function.

(As Output format is NMOS-Open-Drain, can't output 'H' level.)

If no need Acknowledge function, please input 'L' level from SCL 8th='L' to SCL 9th='L'.

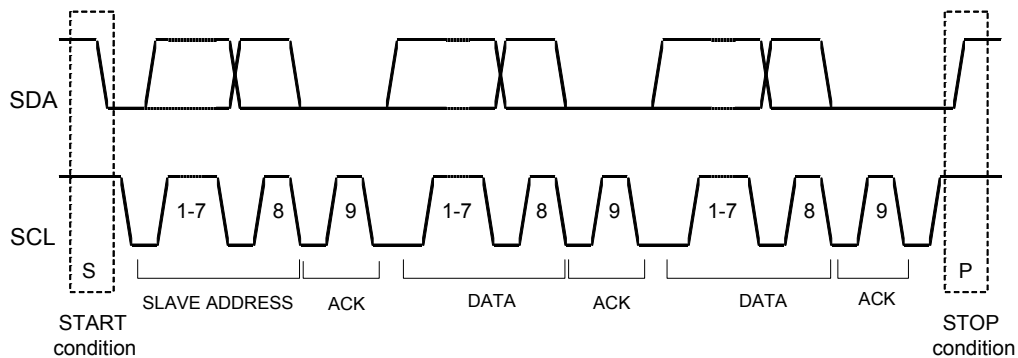


Figure 11. Acknowledge timing

○Command transfer method

Issue the Slave Address (“01111100” for Write Mode or “01111101” for Read Mode) after the “START condition” is generated. Command input follows after the Slave Address. The least significant bit (LSB) of the Slave Address determines if the operation to be done is Write or Read operation.

The MSB is the command/data judgment bit, This bit defines whether succeeding byte is a command or data.

When “command or data judgment bit”=‘1’, the next byte is a command.

When “command or data judgment bit”=‘0’, the next byte is display data.



Once it enters display data transfer condition, it cannot input any command. To input command again, please generate the “START condition” again.

If “START condition” or “STOP condition” is inputted during command transmission, the command will be cancelled. If the Slave address is continuously inputted following “START condition”, it will be in command input condition.

After “START condition” please input “Slave Address” at first. When Slave Address cannot be recognized, Acknowledge does not return and the next transmission will be invalid. When data transmission is in invalid status and the “START condition” is transmitted again, it will return to valid status.

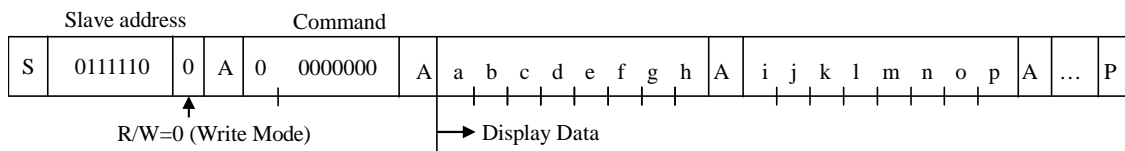
* When transfer command and data, please observe “MPU Interface characteristic” of input rise time, Setup time, and Hold time etc... (Refer to MPU Interface) .

○Write display and transfer method

BU97950FUV enters “Write mode” when R/W bit of Slave address is ‘0’

BU97950FUV has Display Data RAM (DDRAM) of 35×8=280bits.

The relationship between data input and display data, DDRAM data and address are as follows.



The 8-bit display data will be stored in the DDRAM. The address to be written is specified by Address Set command, and the address is automatically incremented after every 8-bits of data.

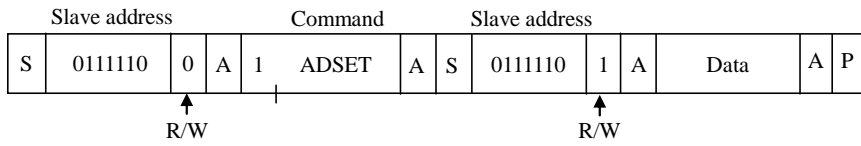
Data can be continuously written in the DDRAM by transmitting Data continuously.

	0	1	2	3	4	5	6	7	21h	22h	
0	a	i										COM0
1	b	j										COM1
2	c	k										COM2
3	d	l										COM3
4	e	m										COM4
5	f	n										COM5
6	g	o										COM6
7	h	p										COM7
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG33	SEG34	

DDRAM address

○Read Command Register and Transfer Method

BU97950FUV enters “Read mode” when R/W bit of Slave address is ‘1’
 During Read mode the command registers can be read.
 The sequence for the command register read is shown below.

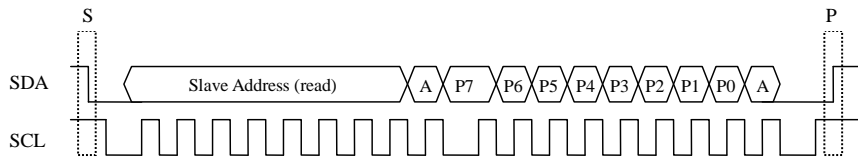


The following register settings can be read in this mode.
 Only one register setting can be read at once, after read register setting BU97950FUV exit from read mode and wait slave address. If all register setting read is needed, please make sequence for “REG1” and “REG2”, respectively.

Register	D7	D6	D5	D4	D3	D2	D1	D0	Address
REG1	0	0	P5	P4	P3	P2	P1	P0	23h
REG2	P7	P6	P5	P4	P3	P2	P1	P0	24h

- REG1: P5 = Software reset condition
 P4 to P0 = EVR setting
- REG2: P7 to P6 = Frame Frequency (FR) setting
 P5 to P4 = Power Save Mode (SR) setting
 P3 = LCD drive waveform setting
 P2 = Display ON/OFF setting
 P1 = APON setting
 P0 = APOFF setting

An example of the command register read sequence is shown below.



- LCD Driver Bias Circuit
 This device generates LCD driving voltage with built in Buffer AMP.
 And it can drive LCD at low power consumption.
 *Line and frame inversion can set in DISCTL command.
 Refer to the “LCD driving waveform” about each LCD driving waveform.

- Reset initialize condition
 Initial condition after execute Software Reset is as follows.
 - Display is OFF.
 - DDRAM address is initialized (DDRAM Data is not initialized).
 Refer to Command Description about initialize value of register.

●Command / Function List

Description List of Command / Function

	Command	Function
1	Address set (ADSET)	DDRAM address setting (00h to 22h) Command register address setting (23h, 24h)
2	EVR set (EVRSET)	EVR setting (0 to 31)
3	Display Control (DISCTL)	Frame Frequency, Power save mode setting
4	IC operation set (ICSET)	LCD drive mode, software reset, display on/off
5	All pixel Control (APCTL)	All pixel control during display ON

●Detailed command description

D7 (MSB) is bit for command or data judgment.

Regarding more detail information, please refer to "Command and data transfer method".

C: 0: Next byte is RAM write data.

1: Next byte is command.

○Address set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	P5	P4	P3	P2	P1	P0

Address data is specified in P[5:0].

The address range can be set as 000000 to 100010(bin) for Write mode.

When the specified address is out of range, the address will be set to "000000".

The Reset initialize condition of the DDRAM address is "000000"

The address can be set 100011 (bin) and 100100 (bin) for Read mode.

It is prohibited to set other address.

P[5:0] = 23h (100011b) - REG1

Register address for Software reset condition and EVR setting

P[5:0] = 24h (100100b) - REG2

Register address for the other settings

(Regarding more detail information, please refer to "Read Command Register and Transfer Method")

○EVR Set (EVRSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	P4	P3	P2	P1	P0

It is able to control 32-step electrical volume register (EVR).

It is able to set V0 voltage level (the max level voltage of LCD driving voltage).

Electrical volume register (EVR) is set "00000" in reset initialize condition

In "00000" condition, V0 voltage output VLCD voltage.

It is prohibited to set EVR V0 voltage under 2.5V.

And please satisfy "VLCD - V0 > 0.6" condition.

If this condition can not be satisfied, IC output voltage will be unstable.

○The relationship of electrical volume register (EVR) setting and V0 voltage

EVR	Calculation formula	VLCD= 5.500	VLCD= 5.000	VLCD= 4.000	VLCD= 3.500	VLCD= 3.000	VLCD= 2.500	[V]
0	VLCD	V0= 5.500	V0= 5.000	V0= 4.000	V0= 3.500	V0= 3.000	V0= 2.500	[V]
1	0.967*VLCD	V0= 5.323	V0= 4.839	V0= 3.871	V0= 3.387	V0= 2.903	V0= 2.419	[V]
2	0.937*VLCD	V0= 5.156	V0= 4.688	V0= 3.750	V0= 3.281	V0= 2.813	V0= 2.344	[V]
3	0.909*VLCD	V0= 5.000	V0= 4.545	V0= 3.636	V0= 3.182	V0= 2.727	V0= 2.273	[V]
4	0.882*VLCD	V0= 4.853	V0= 4.412	V0= 3.529	V0= 3.088	V0= 2.647	V0= 2.206	[V]
5	0.857*VLCD	V0= 4.714	V0= 4.286	V0= 3.429	V0= 3.000	V0= 2.571	V0= 2.143	[V]
6	0.833*VLCD	V0= 4.583	V0= 4.167	V0= 3.333	V0= 2.917	V0= 2.500	V0= 2.083	[V]
7	0.810*VLCD	V0= 4.459	V0= 4.054	V0= 3.243	V0= 2.838	V0= 2.432	V0= 2.027	[V]
8	0.789*VLCD	V0= 4.342	V0= 3.947	V0= 3.158	V0= 2.763	V0= 2.368	V0= 1.974	[V]
9	0.769*VLCD	V0= 4.231	V0= 3.846	V0= 3.077	V0= 2.692	V0= 2.308	V0= 1.923	[V]
10	0.750*VLCD	V0= 4.125	V0= 3.750	V0= 3.000	V0= 2.625	V0= 2.250	V0= 1.875	[V]
11	0.731*VLCD	V0= 4.024	V0= 3.659	V0= 2.927	V0= 2.561	V0= 2.195	V0= 1.829	[V]
12	0.714*VLCD	V0= 3.929	V0= 3.571	V0= 2.857	V0= 2.500	V0= 2.143	V0= 1.786	[V]
13	0.697*VLCD	V0= 3.837	V0= 3.488	V0= 2.791	V0= 2.442	V0= 2.093	V0= 1.744	[V]
14	0.681*VLCD	V0= 3.750	V0= 3.409	V0= 2.727	V0= 2.386	V0= 2.045	V0= 1.705	[V]
15	0.666*VLCD	V0= 3.667	V0= 3.333	V0= 2.667	V0= 2.333	V0= 2.000	V0= 1.667	[V]
16	0.652*VLCD	V0= 3.587	V0= 3.261	V0= 2.609	V0= 2.283	V0= 1.957	V0= 1.630	[V]
17	0.638*VLCD	V0= 3.511	V0= 3.191	V0= 2.553	V0= 2.234	V0= 1.915	V0= 1.596	[V]
18	0.625*VLCD	V0= 3.438	V0= 3.125	V0= 2.500	V0= 2.188	V0= 1.875	V0= 1.563	[V]
19	0.612*VLCD	V0= 3.367	V0= 3.061	V0= 2.449	V0= 2.143	V0= 1.837	V0= 1.531	[V]
20	0.600*VLCD	V0= 3.300	V0= 3.000	V0= 2.400	V0= 2.100	V0= 1.800	V0= 1.500	[V]
21	0.588*VLCD	V0= 3.235	V0= 2.941	V0= 2.353	V0= 2.059	V0= 1.765	V0= 1.471	[V]
22	0.576*VLCD	V0= 3.173	V0= 2.885	V0= 2.308	V0= 2.019	V0= 1.731	V0= 1.442	[V]
23	0.566*VLCD	V0= 3.113	V0= 2.830	V0= 2.264	V0= 1.981	V0= 1.698	V0= 1.415	[V]
24	0.555*VLCD	V0= 3.056	V0= 2.778	V0= 2.222	V0= 1.944	V0= 1.667	V0= 1.389	[V]
25	0.545*VLCD	V0= 3.000	V0= 2.727	V0= 2.182	V0= 1.909	V0= 1.636	V0= 1.364	[V]
26	0.535*VLCD	V0= 2.946	V0= 2.679	V0= 2.143	V0= 1.875	V0= 1.607	V0= 1.339	[V]
27	0.526*VLCD	V0= 2.895	V0= 2.632	V0= 2.105	V0= 1.842	V0= 1.579	V0= 1.316	[V]
28	0.517*VLCD	V0= 2.845	V0= 2.586	V0= 2.069	V0= 1.810	V0= 1.552	V0= 1.293	[V]
29	0.508*VLCD	V0= 2.797	V0= 2.542	V0= 2.034	V0= 1.780	V0= 1.525	V0= 1.271	[V]
30	0.500*VLCD	V0= 2.750	V0= 2.500	V0= 2.000	V0= 1.750	V0= 1.500	V0= 1.250	[V]
31	0.491*VLCD	V0= 2.705	V0= 2.459	V0= 1.967	V0= 1.721	V0= 1.475	V0= 1.230	[V]

 Prohibit setting

*In case EVR using, please satisfy VLCD-V0 >0.6 V condition.

If do not satisfy this condition, IC output will be unstable.

*Do not use V0 < 2.5V area. If EVR set this area, IC operating will be unstable.

ODisplay control (DISCTL)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	P3	P2	P1	P0

Set Power save mode FR.

Power save mode FR	P3	P2	Reset initialize condition
Normal mode (80Hz)	0	0	○
Power save mode1 (71Hz)	0	1	
Power save mode2 (64Hz)	1	0	
Power save mode3 (50Hz)	1	1	

* Operation current decrease in
Normal mode > Power save mode1 > Power save mode2 > Power save mode 3 order.

Set Power save mode SR.

Setup	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

* Operation current increase in order of
Power save mode 1 < Power save mode 2 < Normal mode < High power mode order.

Note:

Power save mode FR / LCD drive waveform / Power save mode SR will affect the display image.
Select the best value depending on the current consumption and display image using LCD panel
(under real application).

Mode	Flicker	Display grade/Contrast
Power save mode FR	○	-
LCD drive waveform (ICSET)	○	○
Power save mode SR	-	○

OSet IC Operation (ICSET)

MSB						LSB	
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	P2	P1	P0

Set LCD drive waveform.

Setup	P2	Reset initialize condition
Line inversion mode	0	
Frame inversion mode	1	○

Operation current: Line inversion > Frame inversion
 For drive mode of Line inversion and Frame inversion, refer to LCD waveform.

Set Software Reset condition.

Setup	P1	Reset initialize condition
No operation	0	○
Software reset	1	

When "Software Reset" is executed, this device is reset to initial condition.
 (Refer to Reset initialize condition)
 Software reset is asserted only once when P1 is set.
 Other settings can be set after this.

Set Display ON and OFF

Setup	P0	Reset initialize condition
Display OFF (DISPOFF)	0	○
Display ON (DISPON)	1	

Display OFF : The DDRAM content is not affected. All SEGMENT and COMMON output stop after a frame.
 Display OFF mode ends when Display ON is set.

Display ON : SEGMENT and COMMON outputs are active.
 Start read operation to display data from the DDRAM.

OAll Pixel control (APCTL)

MSB						LSB	
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	0	P1	P0

All display set ON

APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

All display set OFF

APOFF	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

All pixels ON : All pixels are ON regardless of DDRAM data.
 All pixels OFF : All pixels are OFF regardless of DDRAM data.

Note:

All pixels ON/OFF is effective only at the time of "Display ON" status.
 The contents of DDRAM do not change at this time.
 When P1 and P0='1', APOFF is selected. APOFF has higher priority than APON.

●LCD driving waveform

(1/4bias, 1/8duty)

Line inversion mode

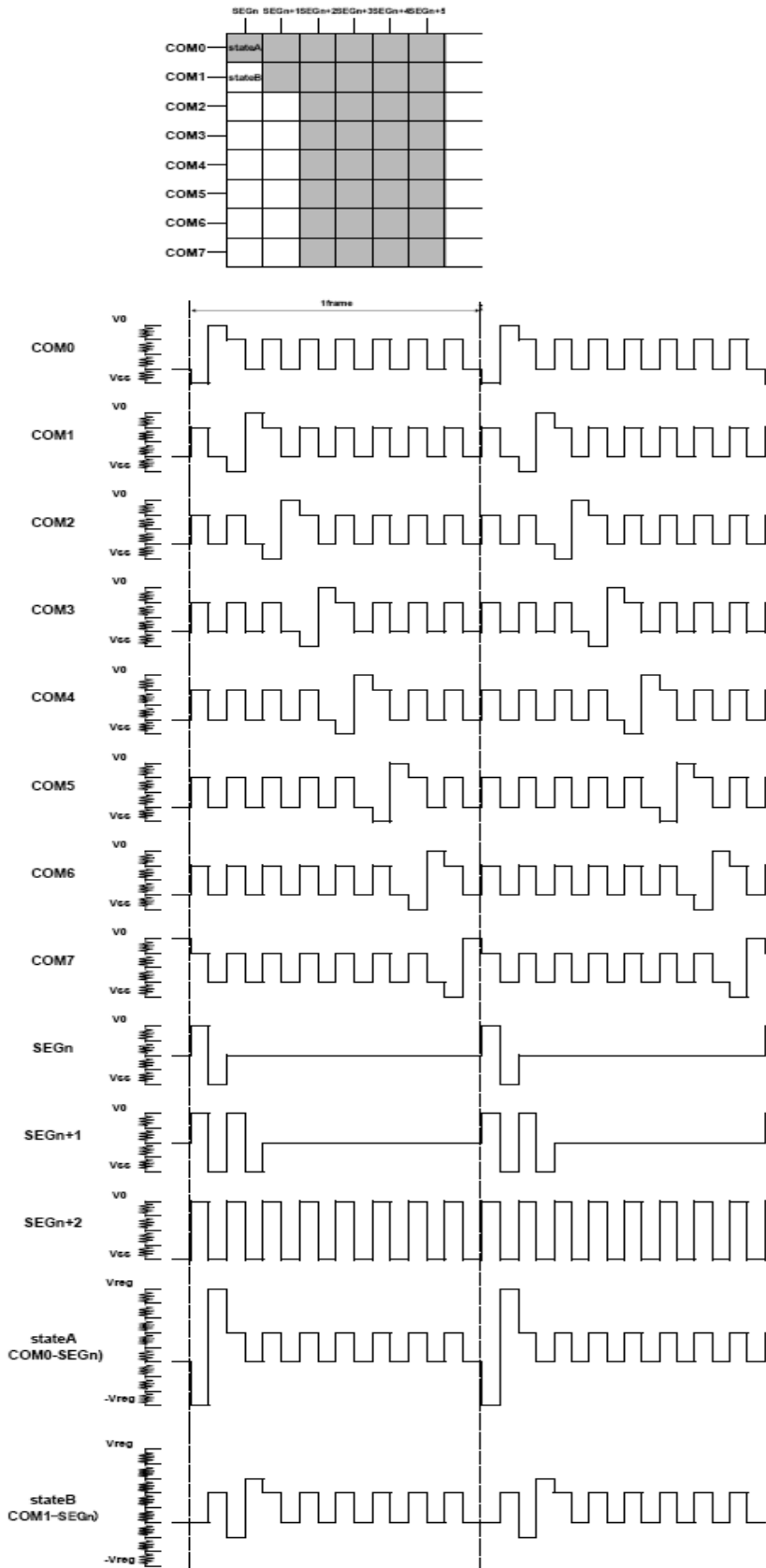


Figure 12. Wave form of line inversion

Frame inversion mode

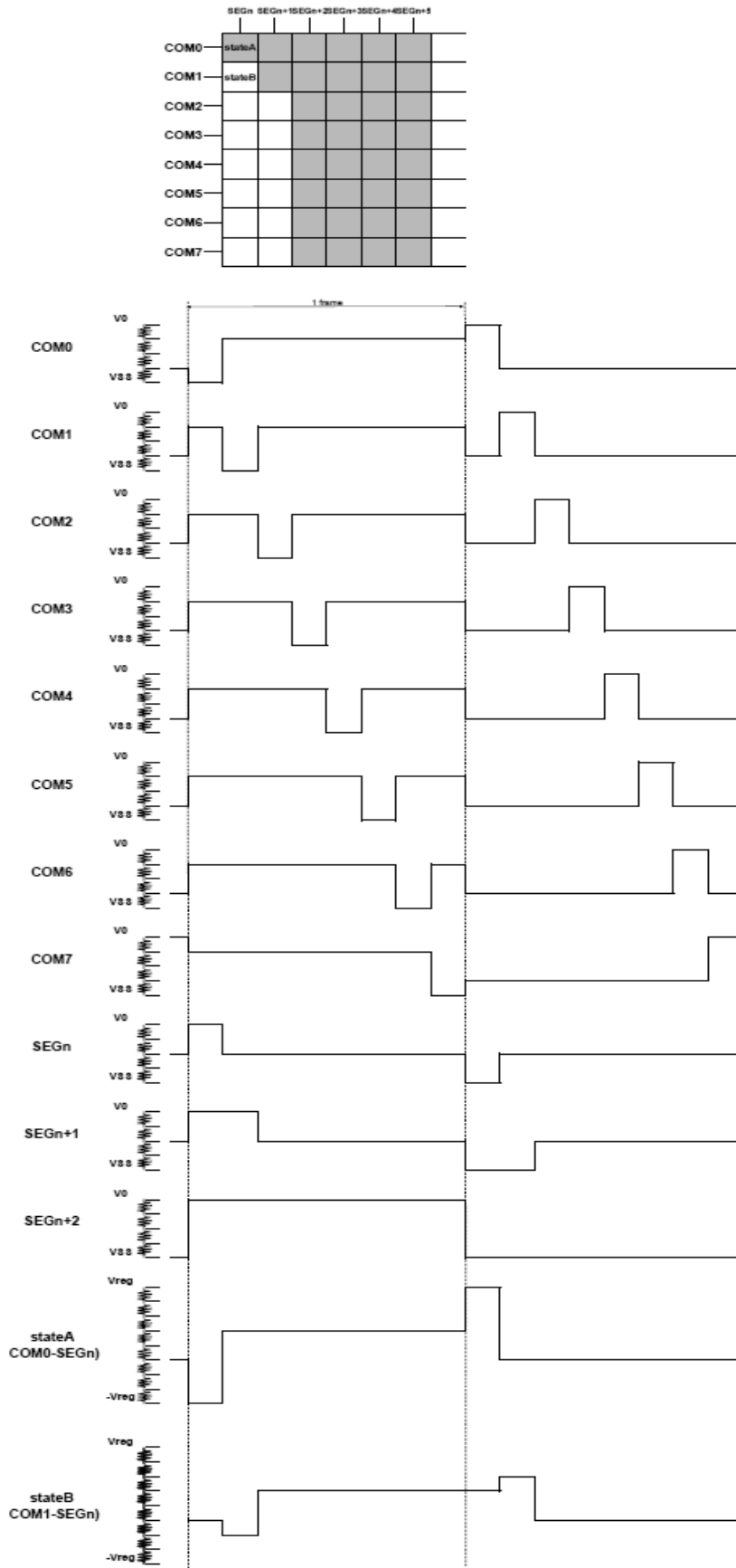
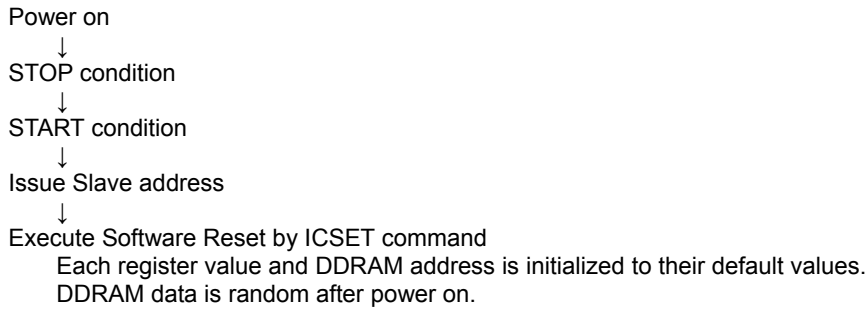


Figure 13. Wave form of frame inversion

●Initialize sequence

Please follow the sequence below after Power-On to set this device to initial condition.



●Start sequence

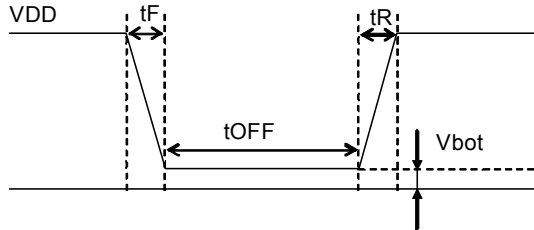
○Start sequence example

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0 to 5V (Tr=0.1ms)
	↓									
2	wait 100us									Initialize IC
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
5	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
6	ICSET	1	1	1	1	0	*	1	*	Software Reset
	↓									
7	DISCTL	1	1	1	0	0	0	1	0	Unnecessary when initial value setup (If you need to change the condition)
	↓									
8	EVRSET	1	1	0	0	0	0	0	0	Unnecessary when initial value setup (If you need to change the condition)
	↓									
9	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	Address 00h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	Address 22h
	↓									
11	Stop									Stop condition
	↓									
12	Start									Start condition
13	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
14	ICSET	1	1	1	1	0	*	0	1	Display ON

●Caution in P.O.R circuit use

This device has "P.O.R" (Power-On Reset) circuit and Software Reset function. Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended t_R , t_F , t_{OFF} , and V_{bot} spec below in order to ensure P.O.R operation



Recommended condition of t_R , t_F , t_{OFF} , V_{bot} ($T_a=25\text{ }^\circ\text{C}$)

t_R	t_F	t_{OFF}	V_{bot}
Less than 5ms	Less than 5ms	More than 20ms	Less than 0.3V

Figure 14. Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.

- (1) STOP condition

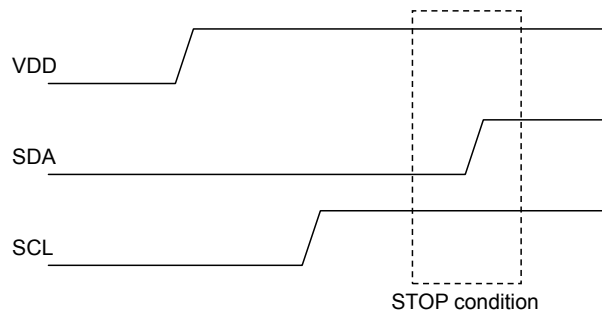


Figure 15. STOP condition

- (2) START condition.
- (3) Issue Slave address.
- (4) Execute Software Reset (ICSET) command.

●Note on the number of LSIs being connected to the same bus.

Do not access the other device without power supply (VDD) to the BU97950.

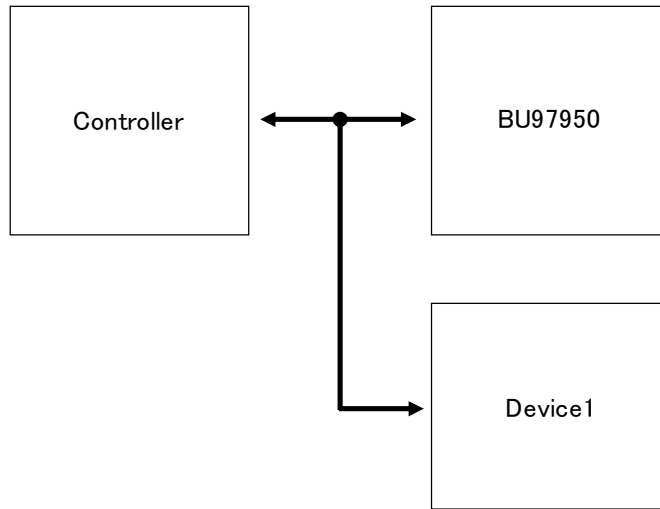


Figure 16. Example of BUS connection

To control the slope of the falling edge, a capacitor is connected between gate and drain of a NMOS transistor (Refer to Figure 17).

The gate is in a high-impedance state if the power (VDD) is not supplied.

In this condition, the gate voltage is pulled up by the current flow through the capacitance as a result of the SDA signal's transition from LOW to HIGH.

The NMOS transistor turns on and draw some current (I_{ds}) from the SDA port if the gate voltage (V_g) is higher than the threshold voltage (V_{th}).

An external resistor (R) is connected between the power line and SDA line to keep the SDA line as a logic HIGH. But the line cannot be kept as a logic HIGH if the voltage drop ($R \cdot I_{ds}$) is large.

Access the other LSIs with power supply to BU9792x to control the gate voltage as logic level of 1 or 0 if the number of LSIs are connected to the same bus.

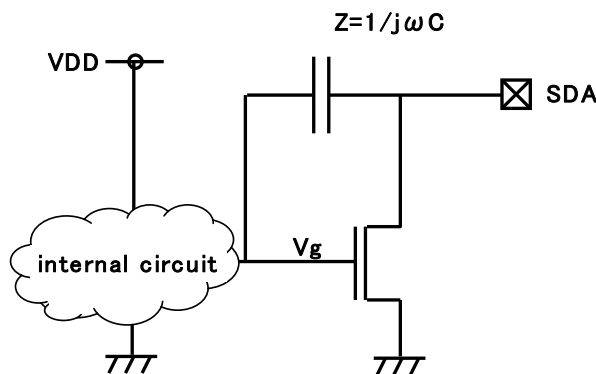


Figure 17. SDA output cell structure

Status of this document

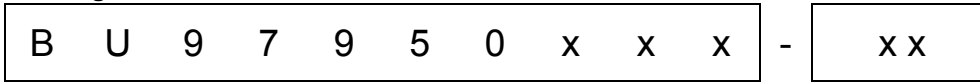
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

●Operational Notes

- (1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.
- (2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.
- (3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.
- (4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.
- (5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.
- (6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.
- (7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.
- (8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.
- (9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.
- (10) Ground wiring pattern
If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.
- (11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.
- (12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.
- (13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

●Ordering Information



Part Number

Package

FUV : TSSOP-C48V
KS2 : SQFP-T52

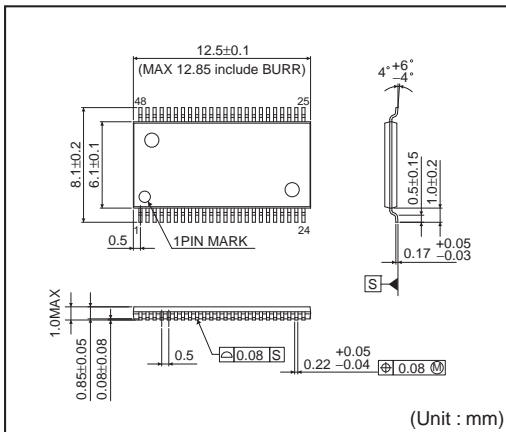
Packaging and forming specification
E2: Embossed tape and reel
(TSSOP-C48V)

●Lineup

Package		Orderable Part Number
TSSOP-C48V	Reel of 2000	BU97950FUV-E2
SQFP-T52	Tray of 1000	BU97950KS2

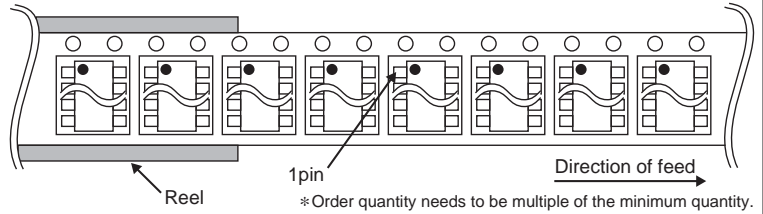
●Physical Dimension Tape and Reel Information

TSSOP-C48V

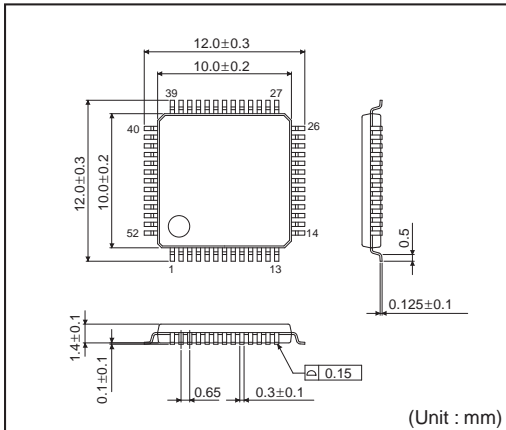


<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

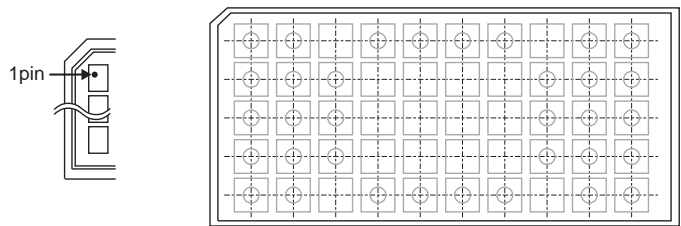


SQFP-T52



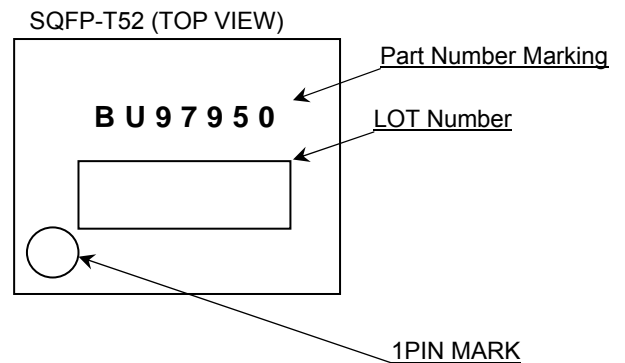
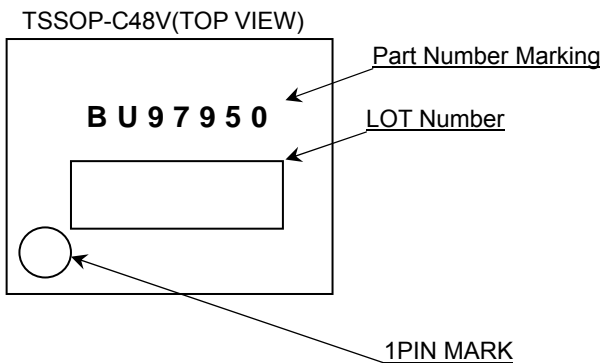
<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray



* Order quantity needs to be multiple of the minimum quantity.

●Marking Diagrams



●Revision History

Date	Revision	Changes
1.Jun.2012	001	New Release

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 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
- 4) The Products are not subject to radiation-proof design.
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- 6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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- 8) Confirm that operation temperature is within the specified range described in the product specification.
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- 2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
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