2-Channel RGB Charge Pump LED Driver with Illumination

BD2812GU

●General Description

The BD2812GU is a RGB LED driver for decorative purposes. This RGB driver has lighting patterns and can illuminate LEDs without load of CPU. This RGB driver is best-suited for illumination using RGB LEDs, and decoration using monochrome LEDs. The DC/DC block adopts a charge pump system and not uses an inductor. This RGB driver has been miniaturized through the use of a VCSP85H3 (3.1 mm×3.1 mm 0.5 mm pitch) chip size package.

●Features

■RGB LED driver (dual drivers)
- ➢ A slope control function is incorporated (allowing dual drivers to be controlled independently).
- ➢ Slope control can be implemented using the DC current.
- ➢ Two modes “continuous illumination mode” and “illumination single cycle mode” are supported.
- ➢ Independent external ON/OFF synchronizing terminals (of dual drivers) are provided.
- ➢ Multiple drivers can be used concurrently by using the I^2C address change function and supporting reference clock I/O.
- ➢ Low consumption operation is possible by the Sleep operation mode function.

●Features – **continued**

■Charge pump system DC/DC
- ➢ Boost magnification is changed automatically (x1, x1.5, x2)
- ➢ Supports an output voltage auto mode function (It adjusts to voltage required for LED automatically)
- ➢ Supports an output voltage fixed mode function (3.9V/4.2V/4.5V/4.8V)
- ➢ Mounts a soft start function, an over voltage protection function (auto recovery type) and an over current protection (auto recovery)

■Thermal shutdown

■I^2C BUS fast mode support (maximum rate: 400 kHz) format
- ➢ A device address can be changed via an external pin.

●Key Specifications

- ■ Operating power supply voltage range: 2.7V to 5.5V
- ■ LED maximum setting current: 30.48mA (Max.)
- ■ Oscillator Frequency: 1.0MHz(Typ.)
- ■ Operating temperature range: -40℃ to +85℃

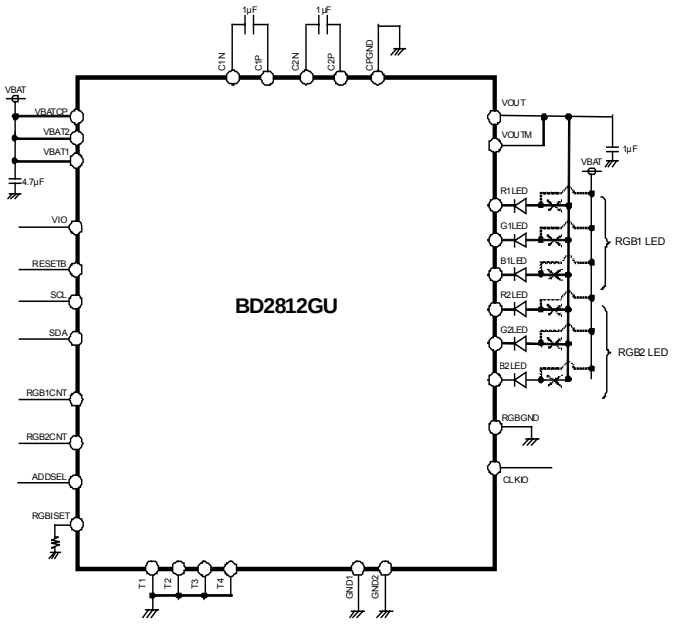
●Package

	W(Typ.) x D(Typ.) x H(Max.)
VCSP85H3	3.10mm x 3.10mm x 1.00mm

●Application

■ Mobile Phone, Portable device

●Typical Application Circuit



●Pin Configuration [Bottom View]

	1	2	3	4	5	6
F	T4	VBAT1	B2LED	RGBGND	B1LED	T3
E	GND1	RGBISET	G2LED	R2LED	G1LED	R1LED
D	RGB2CNT	RGB1CNT			VOUTM	VOUT
C	VBAT2	CLKIO	index		C1P	C2P
B	GND2	SCL	SDA	ADDSEL	C1N	VBATCP
A	T1	VIO	RESETB	CPGND	C2N	T2

●**Absolute Maximum Ratings** (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Maximum Applied Voltage	VMAX	7	V
Power Dissipation	Pd	1460 *1	mW
Operating Temperature Range	Topr	-40 to +85	℃
Storage Temperature Range	Tstg	-55 to +150	℃

*1 Power dissipation deleting is –11.68mW/ ℃, when it's used in over 25 ℃. (It's deleting is on the board that is ROHM's standard)

●**Recommended Operating Ratings** (VBAT≥VIO, Ta=-40 to 85℃)

Parameter	Symbol	Ratings	Unit
VBAT Input Voltage	VBAT	2.7 to 5.5	V
VIO Pin Voltage	VIO	1.65 to 3.3	V

●**Electrical Characteristics** (Unless otherwise specified, Ta=25℃, VBAT=3.6V, VIO=1.8V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
【Circuit Current】						
VBAT Circuit Current 1	IBAT1	-	0.1	3.0	μA	RESETB=0V, VIO =0V
VBAT Circuit Current 2	IBAT2	-	0.5	3.0	μA	RESETB=0V, VIO=1.8V
VBAT Circuit Current 3	IBAT3	-	0.8	1.2	mA	LED 6Ch ON, ILED=10mA setting Exclusive of LED current, RGBISET =120kΩ
VBAT Circuit Current 4	IBAT4	-	61	65	mA	DC/DC x1mode, Io=60mA, VBAT=4.0V
VBAT Circuit Current 5	IBAT5	-	92	102	mA	DC/DC x1.5mode, Io=60mA, VBAT=3.6V
VBAT Circuit Current 6	IBAT6	-	123	140	mA	DC/DC x2mode, Io=60mA, VBAT=2.7V
VBAT Circuit Current 7	IBAT7	-	5	7.5	μA	External clock Sleep operation mode External clock = 31.25kHz, ILED=0mA
【LED Driver】						
LED Current Step	ILEDSTP		128		step	RGB1 group, RGB2 group
LED Maximum Setup Current	IMAX	-	-	30.48	mA	RGB1 group, RGB2 group RGBISET=100kΩ
LED Current Accurate	ILED	18	20	22	mA	RGB1 group, RGB2 group, Terminal voltage =1V ILED=20mA setting, RGBISET =120kΩ
LED Current Matching	ILEDMT	-	5	10	%	RGB1 group, between RGB2 group, Terminal voltage =1V ILED=20mA setting
LED OFF Leak Current	ILKL	-	-	1.0	μA	
【DC/DC (Charge Pump)】						
Output Voltage 1	VoCP1	-	Vf+0.2	Vf +0.25	V	At output voltage auto mode, Vf is forward direction of LED
Output Voltage 2	VoCP2	3.705	3.9	4.095	V	At fixed voltage output mode, Io=60mA VBAT≥3.2V
		3.99	4.2	4.41	V	
		4.275	4.5	4.725	V	
		4.56	4.8	5.04	V	
Load Stability	Iout	-	-	255	mA	VBAT≥3.2V, VOUT=4V
Oscillator Frequency	fosc	0.8	1.0	1.2	MHz	
Over Voltage Protection Detect Voltage	OVP	-	6.0	6.5	V	
Over Current Protection Detect Current	OCP	-	250	375	mA	VOUT=0V

●**Electrical Characteristics - continued** (Unless otherwise specified, Ta=25 ℃, VBAT=3.6V, VIO=1.8V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
【SDA, SCL】(I^2C interface)						
L level Input Voltage	VILI	-0.3	-	0.25 ×VIO	V	
H level Input Voltage	VIHI	0.75 ×VIO	-	VBAT +0.3	V	
Hysteresis of Schmitt Trigger Input	VhysI	0.05 ×VIO	-	-	V	
L Level Output Voltage	VOLI	0	-	0.3	V	SDA pin, IOL=3 mA
Input Current	IinI	-10	-	10	μA	Input voltage = 0.1×VIO to 0.9×VIO
【RESETB, ADDSEL】(CMOS input pin)						
L Level input Voltage	VILR	-0.3	-	0.25 ×VIO	V	
H Level input Voltage	VIHR	0.75 ×VIO	-	VBAT +0.3	V	
Input Current	IinR	-10	-	10	μA	Input voltage = 0.1×VIO to 0.9×VIO
【RGB1CNT, RGB2CNT】(CMOS input pin with Pull-down resistance)						
L Level Input Voltage	VILCNT	-0.3	-	0.25 ×VIO	V	
H Level Input Voltage	VIHCNT	0.75 ×VIO	-	VBAT +0.3	V	
Input Current	IinCNT	-	3.6	10	μA	Input voltage = 1.8V
【CLKIO(Output)】(CMOS output pin)						
L Level Output Voltage	VOLCLK	-	-	0.2	V	IOL=1mA
H Level Output Voltage	VOHCLK	VIO -0.2	-	-	V	IOH=1mA
Output Frequency1	fclk1	200	250	300	kHz	FSEL=0 setting
Output Frequency2	fclk2	25	31.25	37.5	kHz	FSEL=1 setting
【CLKIO (Input)】(CMOS input pin with Pull-down resistance)						
L Level Input Voltage	VILCLK	-0.3	-	0.25 ×VIO	V	
H Level Input Voltage	VIHCLK	0.75 ×VIO	-	VIO +0.3	V	
Input Current	IinCLK	-	3.6	10	μA	Input voltage = 1.8V

●**Timing diagram**

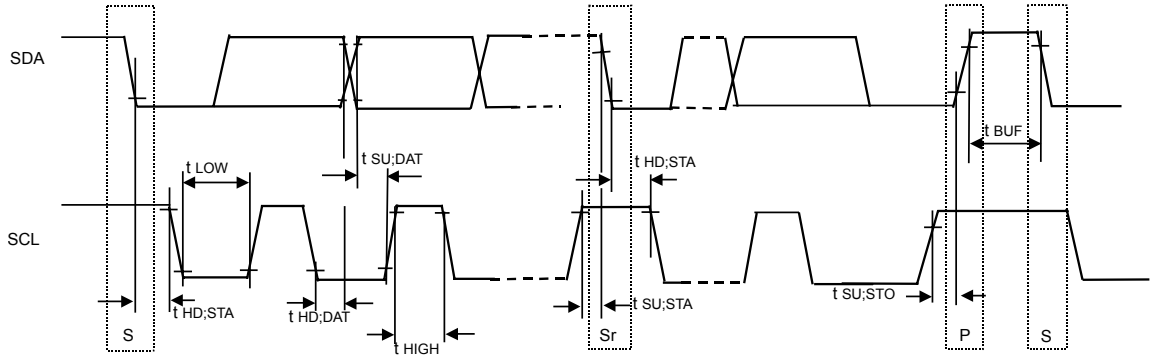


Figure 1 Timing diagram

(Unless otherwise specified, Ta=25℃, VBAT=3.6V, VIO=1.8V)

Parameter	Symbol	Standard-mode			Fast-mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
【I^2C BUS format】								
SCL clock frequency	f_{SCL}	0	-	100	0	-	400	kHz
LOW period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	μs
Hold time (repeated) START condition After this period, the first clock is generated	$t_{HD;STA}$	4.0	-	-	0.6	-	-	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	-	0.6	-	-	μs
Data hold time	$t_{HD;DAT}$	0	-	3.45	0	-	0.9	μs
Data set-up time	$t_{SU;DAT}$	250	-	-	100	-	-	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	-	0.6	-	-	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	μs

●**Pin Descriptions**

No	Pin No.	Pin Name	I/O	Input Level		ESD Diode	Functions
				For Power	For GND		
1	B6	VBATCP	-	-	GND	Battery is connected	A
2	F2	VBAT1	-	-	GND	Battery is connected	A
3	C1	VBAT2	-	-	GND	Battery is connected	A
4	A1	T1	-	VBAT	GND	Test Pin (short to GND)	L
5	A6	T2	-	VBAT	GND	Test Pin (short to GND)	L
6	F6	T3	-	VBAT	GND	Test Pin (short to GND)	L
7	F1	T4	-	VBAT	-	Test Pin (short to GND)	B
8	A2	VIO	-	VBAT	GND	I/O voltage source is connected	C
9	A3	RESETB	I	VBAT	GND	Reset input (L: RESET, H: RESET cancel)	H
10	B3	SDA	I/O	VBAT	GND	I^2C data input	I
11	B2	SCL	I	VBAT	GND	I^2C clock input	H
12	A4	CPGND	-	VBAT	-	Ground	B
13	E1	GND1	-	VBAT	-	Ground	B
14	B1	GND2	-	VBAT	-	Ground	B
15	F4	RGBGND	-	VBAT	-	Ground	B
16	B5	C1N	I/O	VBAT	GND	Charge pump Capacitor is connected	F
17	C5	C1P	I/O	-	GND	Charge pump Capacitor is connected	A
18	A5	C2N	I/O	VBAT	GND	Charge pump Capacitor is connected	F
19	C6	C2P	I/O	-	GND	Charge pump Capacitor is connected	A
20	D6	VOUT	O	-	GND	Charge pump Output terminal	A
21	D5	VOUTM	O	-	GND	Charge pump Output terminal	A
22	E2	RGBISET	I	VBAT	GND	RGB LED reference current	G
23	E6	R1LED	I	-	GND	Red LED1 connected	E
24	E5	G1LED	I	-	GND	Green LED1 connected	E
25	F5	B1LED	I	-	GND	Blue LED1 connected	E
26	E4	R2LED	I	-	GND	Red LED2 connected	E
27	E3	G2LED	I	-	GND	Green LED2 connected	E
28	F3	B2LED	I	-	GND	Blue LED2 connected	E
29	D2	RGB1CNT	I	VBAT	GND	RGB1 LED external ON/OFF Synchronism (L:OFF, H:ON)*	J
30	D1	RGB2CNT	I	VBAT	GND	RGB2 LED external ON/OFF Synchronism (L:OFF, H:ON)*	J
31	B4	ADDSEL	I	VBAT	GND	I^2C device address change terminal	H
32	C2	CLKIO	I/O	VBAT	GND	Standard clock input-and-output terminal	N

* A setup of a register is separately necessary to validate it.

●**Pin ESD Type**

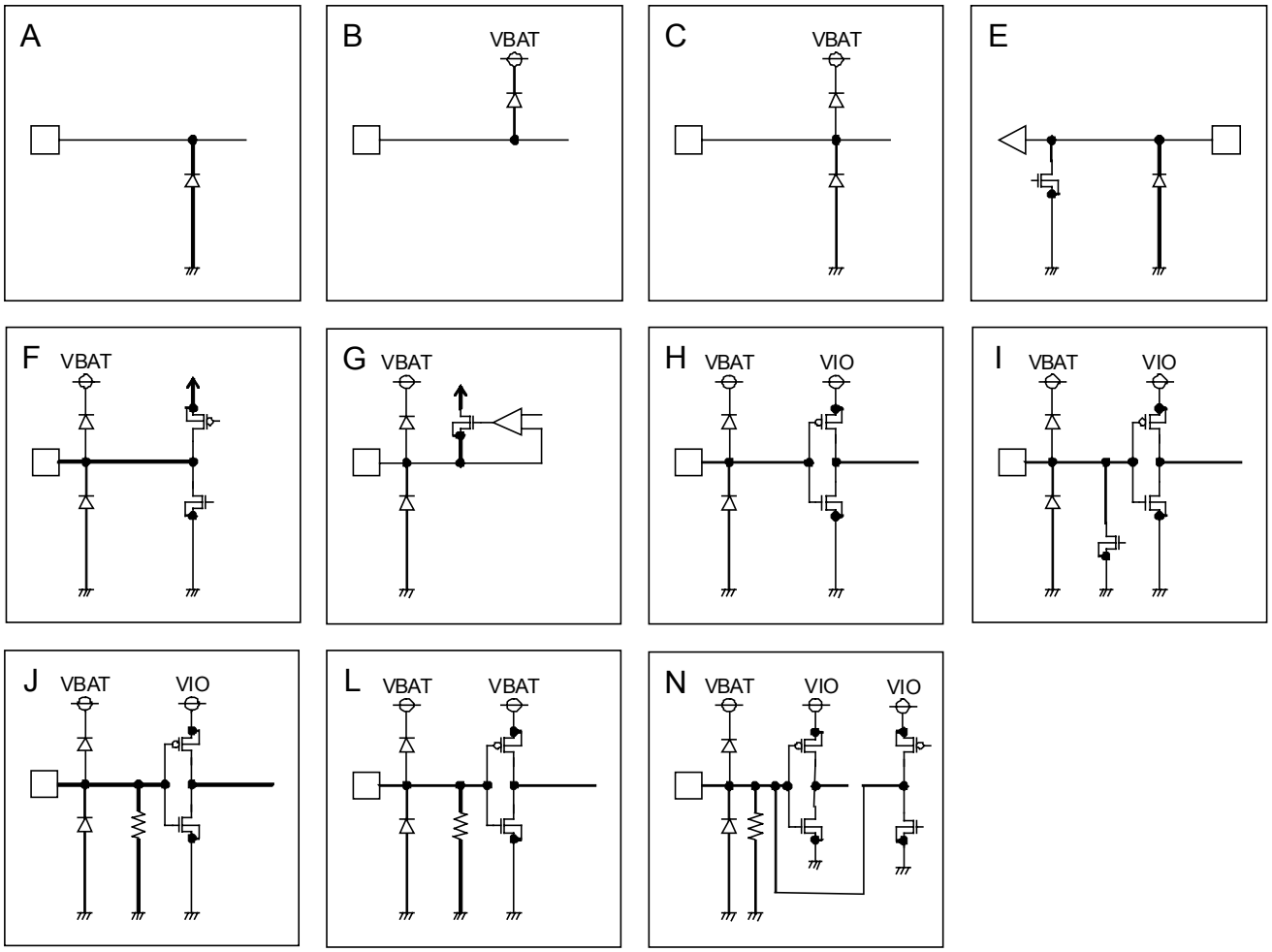
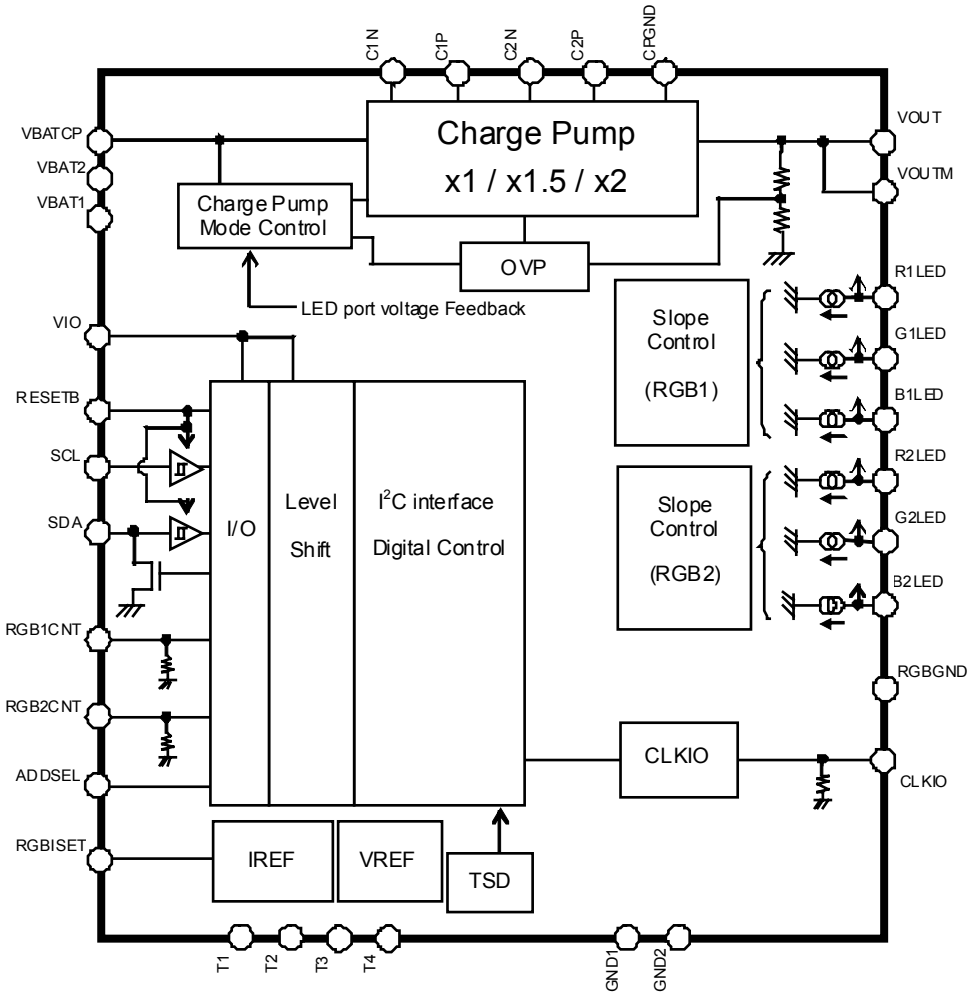


Figure 2. Pin ESD Type

●**Block Diagram**



●I²C BUS Format

The writing operation is based on the I²C slave standard.

・Slave address (Slave address can be changed with the external terminal ADDSEL.)

	A7	A6	A5	A4	A3	A2	A1	R/W
ADDSEL=L	0	0	1	1	0	1	0	1/0
ADDSEL=H	0	0	1	1	0	1	1	1/0

・Bit Transfer

SCL transfers 1-bit data during H. SCL cannot change signal of SDA during H at the time of bit transfer. If SDA changes while SCL is H, START conditions or STOP conditions will occur and it will be interpreted as a control signal.

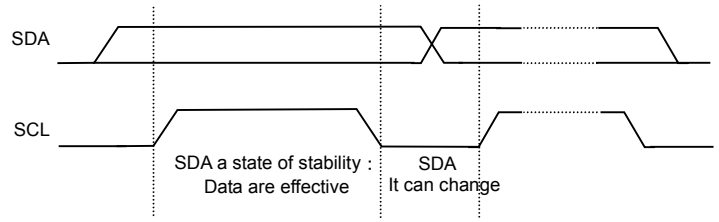


Figure 3. Bit Transfer

・START and STOP condition

When SDA and SCL are H, data is not transferred on the I²C- bus. This condition indicates, if SDA changes from H to L while SCL has been H, it will become START (S) conditions, and an access start, if SDA changes from L to H while SCL has been H, it will become STOP (P) conditions and an access end.

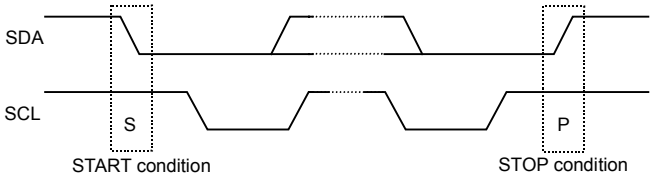


Figure 4. START and STOP condition

・Acknowledge

It transfers data 8 bits each after the occurrence of START condition. A transmitter opens SDA after transfer 8bits data, and a receiver returns the acknowledge signal by setting SDA to L.

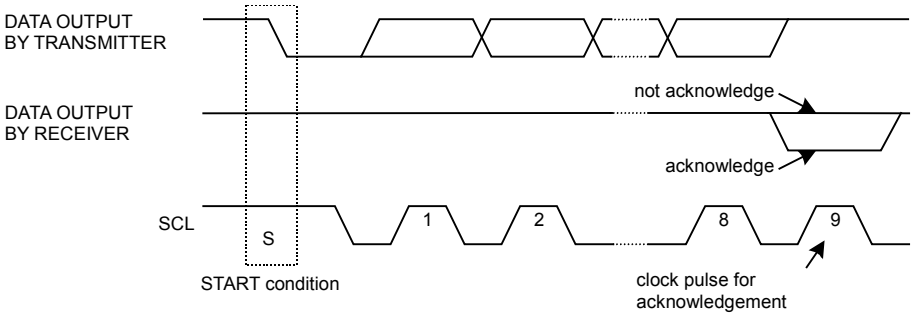


Figure 5. Acknowledge

●I²C BUS Format - continued

・Writing protocol

A register address is transferred by the next 1 byte that transferred the slave address and the write-in command. The 2nd byte is register address. The 3rd byte writes data in the internal register written in by the 2nd byte, and after 4th byte or, the increment of register address is carried out automatically. However, when a register address turns into the last address (15h), it is set to 00h by the next transmission. After the transmission end, the increment of the address is carried out.

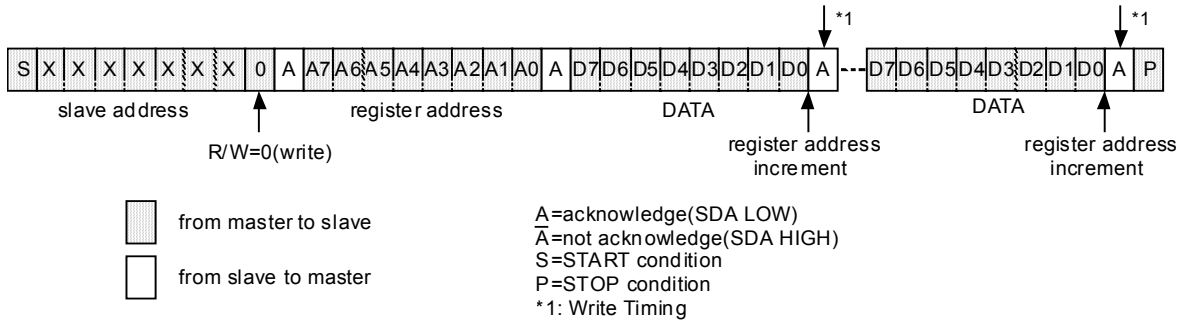


Figure 6. Writing protocol

・Reading protocol

After inputting start conditions, the register address is transferred by the next 1 byte that transferred the slave address and the write-in command. The register address to read is transmitted and the 2nd byte of stop conditions is inputted once. Start conditions are inputted again and a slave address and 1 byte of read-out command are transmitted. The internal data of the register address specified previously is outputted to the 2nd byte. After the transmission of the 2nd byte end, the master side should input the not acknowledge and input stop conditions.

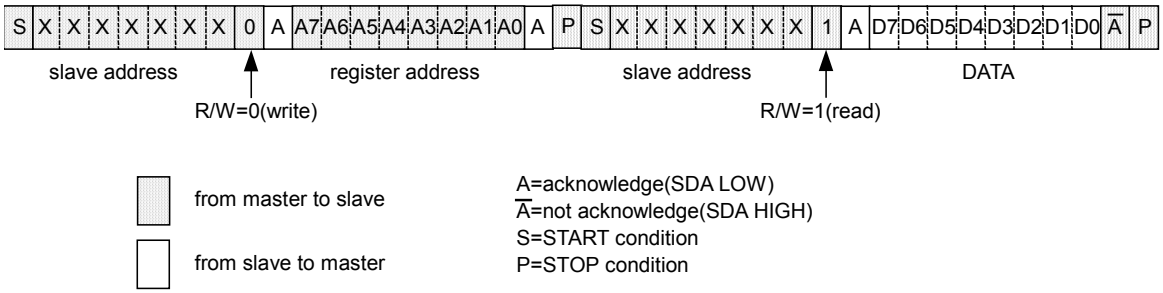


Figure 7. Reading protocol

●Register Map

Address	Write Or Read	Resister data								Function
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	R/W	SLPMD	FSEL	CLKMD	CLKEN	-	-	-	SFTRST	Soft Reset DC/DC driver function
01h	R/W	-	RGB2MEL	RGB2OS	RGB2EN	-	RGB1MEL	RGB1OS	RGB1EN	RGB LED control
02h	W	SFRGB1(1)	SFRGB1(0)	SRRGB1(1)	SRRGB1(0)	-	TRGB1(2)	TRGB1(1)	TRGB1(0)	RGB1 time setup
03h	W	-	IR11(6)	IR11(5)	IR11(4)	IR11(3)	IR11(2)	IR11(1)	IR11(0)	R1 current 1 setup
04h	W	-	IR12(6)	IR12(5)	IR12(4)	IR12(3)	IR12(2)	IR12(1)	IR12(0)	R1 current 2 setup
05h	W	-	-	-	-	PR1(3)	PR1(2)	PR1(1)	PR1(0)	R1 Wave pattern setup
06h	W	-	IG11(6)	IG11(5)	IG11(4)	IG11(3)	IG11(2)	IG11(1)	IG11(0)	G1 current 1 setup
07h	W	-	IG12(6)	IG12(5)	IG12(4)	IG12(3)	IG12(2)	IG12(1)	IG12(0)	G1 current 2 setup
08h	W	-	-	-	-	PG1(3)	PG1(2)	PG1(1)	PG1(0)	G1 Wave pattern setup
09h	W	-	IB11(6)	IB11(5)	IB11(4)	IB11(3)	IB11(2)	IB11(1)	IB11(0)	B1 current 1 setup
0Ah	W	-	IB12(6)	IB12(5)	IB12(4)	IB12(3)	IB12(2)	IB12(1)	IB12(0)	B1 current 2 setup
0Bh	W	-	-	-	-	PB1(3)	PB1(2)	PB1(1)	PB1(0)	B1 Wave pattern setup
0Ch	W	SFRGB2(1)	SFRGB2(0)	SRRGB2(1)	SRRGB2(0)	-	TRGB2(2)	TRGB2(1)	TRGB2(0)	RGB2 time setup
0Dh	W	-	IR21(6)	IR21(5)	IR21(4)	IR21(3)	IR21(2)	IR21(1)	IR21(0)	R2 current 1 setup
0Eh	W	-	IR22(6)	IR22(5)	IR22(4)	IR22(3)	IR22(2)	IR22(1)	IR22(0)	R2 current 2 setup
0Fh	W	-	-	-	-	PR2(3)	PR2(2)	PR2(1)	PR2(0)	R2 Wave pattern
10h	W	-	IG21(6)	IG21(5)	IG21(4)	IG21(3)	IG21(2)	IG21(1)	IG21(0)	G2 current 1 setup
11h	W	-	IG22(6)	IG22(5)	IG22(4)	IG22(3)	IG22(2)	IG22(1)	IG22(0)	G2 current 2 setup
12h	W	-	-	-	-	PG2(3)	PG2(2)	PG2(1)	PG2(0)	G2 Wave pattern setup
13h	W	-	IB21(6)	IB21(5)	IB21(4)	IB21(3)	IB21(2)	IB21(1)	IB21(0)	B2 current 1 setup
14h	W	-	IB22(6)	IB22(5)	IB22(4)	IB22(3)	IB22(2)	IB22(1)	IB22(0)	B2 current 2 setup
15h	W	-	-	-	-	PB2(3)	PB2(2)	PB2(1)	PB2(0)	B2 Wave pattern setup
16h ~ 3Fh	-	Reserved								-
40h	R/W	VOUT(1)	VOUT(0)	DCDCMD	DCDCFON	-	-	-	-	DC/DC driver function
41h	R/W	-	-	-	-	RGB2PW(1)	RGB2PW(0)	RGB1PW(1)	RGB1PW(0)	LED pin function

Input "0" for "-".
Vacancy address may be use for test.
Prohibit to accessing the address that isn't mentioned and the register for test.

●**Register Map - continued**

Address 00h <Soft Reset>

BIT	Name	Init	Function	
			0	1
D7	SLPMD	0	Illuminations Normal mode	Illuminations Sleep mode
D6	FSEL	0	Standard clock output : 250kHz	Standard clock output : 31.25kHz
D5	CLKMD	0	Clock Input mode	Clock Output mode
D4	CLKEN	0	Clock input and output invalid	Clock input and output Effective
D3	-	-	-	-
D2	-	-	-	-
D1	-	-	-	-
D0	SFTRST	0	Reset Release	Reset

Access to D7-D4 bit under operation is prohibition.

Address 01h <RGB LED control >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	RGB2MEL	0	RGB2 external control invalid	RGB2 external control valid
D5	RGB2OS	0	RGB2 Stop	RGB2 1 periodic operation
D4	RGB2EN	0	RGB2 Stop	RGB2 continuous operation
D3	-	-	-	-
D2	RGB1MEL	0	RGB1 external control invalid	RGB1 external control valid
D1	RGB1OS	0	RGB1 Stop	RGB1 1 periodic operation
D0	RGB1EN	0	RGB1 Stop	RGB1 continuous operation

RGB*OS returns to 0 automatically after 1 cycle operation.
RGB*EN precedes to RGB*OS. In use in 1 cycle operation, there is the necessity for RGB*EN=0.

Address 02h <RGB1 time>

BIT	Name	Init	Function	
			0	1
D7	SFRGB1(1)	0	SFRGB1(1) / SFRGB1(0) / Slope Down transition 0 / 0 / 0 0 / 1 / Wave form cycle / 16 1 / 0 / Wave form cycle / 8 1 / 1 / Wave form cycle / 4 It is a theoretical value on logic control, and the reaction time of the analog section is not included. "Slope time" is the time from a slope start to a slope end.	
D6	SFRGB1(0)	0		
D5	SRRGB1(1)	0	SRRGB1(1) / SRRGB1(0) / Slope Up transition 0 / 0 / 0 0 / 1 / Wave form cycle / 16 1 / 0 / Wave form cycle / 8 1 / 1 / Wave form cycle / 4 It is a theoretical value on logic control, and the reaction time of the analog section is not included. "Slope time" is the time from a slope start to a slope end.	
D4	SRRGB1(0)	0		
D3	-	-	-	-
D2	TRGB1(2)	0	TRGB1(2) / TRGB1(1) / TRGB1(0) / Wave form cycle 0 / 0 / 0 / 0.131 s 0 / 0 / 1 / 0.52 s 0 / 1 / 0 / 1.05 s 0 / 1 / 1 / 2.10 s 1 / 0 / 0 / 4.19 s 1 / 0 / 1 / 8.39 s 1 / 1 / 0 / 12.6 s 1 / 1 / 1 / 16.8 s	
D1	TRGB1(1)	0		
D0	TRGB1(0)	0		

Setting time is counted based on the frequency of OSC. The above-mentioned value is a value at the time of Typ (1MHz).
When operating by the external clock, input frequency is a value at the time of Typ (31.25kHz).
Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 03h <R1 current 1setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IR11(6)	0		
D5	IR11(5)	0		
D4	IR11(4)	0		
D3	IR11(3)	0		
D2	IR11(2)	0		
D1	IR11(1)	0		
D0	IR11(0)	0		

IR11(6)	IR11(5)	IR11(4)	IR11(3)	IR11(2)	IR11(1)	IR11(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 04h <R1 current2 setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IR12(6)	0		
D5	IR12(5)	0		
D4	IR12(4)	0		
D3	IR12(3)	0		
D2	IR12(2)	0		
D1	IR12(1)	0		
D0	IR12(0)	0		

IR12(6)	IR12(5)	IR12(4)	IR12(3)	IR12(2)	IR12(1)	IR12(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	0.2mA step
1	1	1	1	1	1	0	25.2m
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 05h <R1 Wave Pattern >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	PR1(3)	0		
D2	PR1(2)	1		
D1	PR1(1)	1		
D0	PR1(0)	1		

PR1(3)	PR1(2)	PR1(1)	PR1(0)	Wave
0	0	0	0	Pattern1
0	0	0	1	Pattern2
0	0	1	0	Pattern3
・ ・	・ ・	・ ・	・ ・	・ ・
1	1	0	1	Pattern14
1	1	1	0	Pattern15
1	1	1	1	Pattern16

Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 06h <G1 current1 setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IG11(6)	0		
D5	IG11(5)	0		
D4	IG11(4)	0		
D3	IG11(3)	0		
D2	IG11(2)	0		
D1	IG11(1)	0		
D0	IG11(0)	0		

IG11(6)	IG11(5)	IG11(4)	IG11(3)	IG11(2)	IG11(1)	IG11(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 07h <G1 current2 setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IG12(6)	0		
D5	IG12(5)	0		
D4	IG12(4)	0		
D3	IG12(3)	0		
D2	IG12(2)	0		
D1	IG12(1)	0		
D0	IG12(0)	0		

IG12(6)	IG12(5)	IG12(4)	IG12(3)	IG12(2)	IG12(1)	IG12(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 08h <G1 Wave Pattern >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	PG1(3)	0		
D2	PG1(2)	1		
D1	PG1(1)	1		
D0	PG1(0)	1		

PG1(3)	PG1(2)	PG1(1)	PG1(0)	Wave
0	0	0	0	Pattern 1
0	0	0	1	Pattern 2
0	0	1	0	Pattern 3
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪
1	1	0	1	Pattern 14
1	1	1	0	Pattern 15
1	1	1	1	Pattern 16

Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 09h <B1 current1setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IB11(6)	0		
D5	IB11(5)	0		
D4	IB11(4)	0		
D3	IB11(3)	0		
D2	IB11(2)	0		
D1	IB11(1)	0		
D0	IB11(0)	0		

IB11(6)	IB11(5)	IB11(4)	IB11(3)	IB11(2)	IB11(1)	IB11(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 0Ah <B1 current2setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IB12(6)	0		
D5	IB12(5)	0		
D4	IB12(4)	0		
D3	IB12(3)	0		
D2	IB12(2)	0		
D1	IB12(1)	0		
D0	IB12(0)	0		

IB12(6)	IB12(5)	IB12(4)	IB12(3)	IB12(2)	IB12(1)	IB12(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 0Bh <B1 Wave Pattern >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	PB1(3)	0		
D2	PB1(2)	1		
D1	PB1(1)	1		
D0	PB1(0)	1		

PB1(3)	PB1(2)	PB1(1)	PB1(0)	Wave
0	0	0	0	Pattern1
0	0	0	1	Pattern2
0	0	1	0	Pattern3
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪
1	1	0	1	Pattern14
1	1	1	0	Pattern15
1	1	1	1	Pattern16

Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 0Ch <RGB2 time >

BIT	Name	Init	Function	
			0	1
D7	SFRGB2(1)	0		
D6	SFRGB2(0)	0		

SFRGB2(1)	SFRGB2(0)	Slope Down transition
0	0	0
0	1	Wave form cycle / 16
1	0	Wave form cycle / 8
1	1	Wave form cycle / 4

It is a theoretical value on logic control, and the reaction time of the analog section is not included.
"Slope time" is the time from a slope start to a slope end.

BIT	Name	Init	Function	
			0	1
D5	SRRGB2(1)	0		
D4	SRRGB2(0)	0		

SRRGB2(1)	SRRGB2(0)	Slope up transition
0	0	0
0	1	Wave form cycle / 16
1	0	Wave form cycle / 8
1	1	Wave form cycle / 4

It is a theoretical value on logic control, and the reaction time of the analog section is not included.
"Slope time" is the time from a slope start to a slope end.

BIT	Name	Init	Function	
			0	1
D3	-	-	-	-

BIT	Name	Init	Function	
			0	1
D2	TRGB2(2)	0		
D1	TRGB2(1)	0		
D0	TRGB2(0)	0		

TRGB2(2)	TRGB2(1)	TRGB2(0)	Wave form cycle
0	0	0	0.131 s
0	0	1	0.52 s
0	1	0	1.05 s
0	1	1	2.10 s
1	0	0	4.19 s
1	0	1	8.39 s
1	1	0	12.6 s
1	1	1	16.8 s

Setting time is counted based on the frequency of OSC. The above-mentioned value is a value at the time of Typ (1MHz).
When operating by the external clock, input frequency is a value at the time of Typ (31.25kHz)
Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 0Dh <R2 current 1setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IR21(6)	0		
D5	IR21(5)	0		
D4	IR21(4)	0		
D3	IR21(3)	0		
D2	IR21(2)	0		
D1	IR21(1)	0		
D0	IR21(0)	0		

IR21(6)	IR21(5)	IR21(4)	IR21(3)	IR21(2)	IR21(1)	IR21(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 0Eh <R2 current 2setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IR22(6)	0		
D5	IR22(5)	0		
D4	IR22(4)	0		
D3	IR22(3)	0		
D2	IR22(2)	0		
D1	IR22(1)	0		
D0	IR22(0)	0		

IR22(6)	IR22(5)	IR22(4)	IR22(3)	IR22(2)	IR22(1)	IR22(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 0Fh <R2 Wave Pattern setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	PR2(3)	0		
D2	PR2(2)	1		
D1	PR2(1)	1		
D0	PR2(0)	1		

PR2(3)	PR2(2)	PR2(1)	PR2(0)	Wave
0	0	0	0	Pattern 1
0	0	0	1	Pattern 2
0	0	1	0	Pattern 3
・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・	・ ・ ・
1	1	0	1	Pattern 14
1	1	1	0	Pattern 15
1	1	1	1	Pattern 16

Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 10h <G2 current 1setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IG21(6)	0		
D5	IG21(5)	0		
D4	IG21(4)	0		
D3	IG21(3)	0		
D2	IG21(2)	0		
D1	IG21(1)	0		
D0	IG21(0)	0		

IG21(6)	IG21(5)	IG21(4)	IG21(3)	IG21(2)	IG21(1)	IG21(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 11h <G2 current 2setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IG22(6)	0		
D5	IG22(5)	0		
D4	IG22(4)	0		
D3	IG22(3)	0		
D2	IG22(2)	0		
D1	IG22(1)	0		
D0	IG22(0)	0		

IG22(6)	IG22(5)	IG22(4)	IG22(3)	IG22(2)	IG22(1)	IG22(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	・ ・	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 12h <G2 Wave Pattern setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	PG2(3)	0		
D2	PG2(2)	1		
D1	PG2(1)	1		
D0	PG2(0)	1		

PG2(3)	PG2(2)	PG2(1)	PG2(0)	Wave
0	0	0	0	Pattern 1
0	0	0	1	Pattern 2
0	0	1	0	Pattern 3
・ ・	・ ・	・ ・	・ ・	・ ・
1	1	0	1	Pattern 14
1	1	1	0	Pattern 15
1	1	1	1	Pattern 16

Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 13h <B2 current 1setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IB21(6)	0		
D5	IB21(5)	0		
D4	IB21(4)	0		
D3	IB21(3)	0		
D2	IB21(2)	0		
D1	IB21(1)	0		
D0	IB21(0)	0		

IB21(6)	IB21(5)	IB21(4)	IB21(3)	IB21(2)	IB21(1)	IB21(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 14h <B2 current 2setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	IB22(6)	0		
D5	IB22(5)	0		
D4	IB22(4)	0		
D3	IB22(3)	0		
D2	IB22(2)	0		
D1	IB22(1)	0		
D0	IB22(0)	0		

IB22(6)	IB22(5)	IB22(4)	IB22(3)	IB22(2)	IB22(1)	IB22(0)	Current
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0.2mA
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪	0.2mA step
1	1	1	1	1	1	0	25.2mA
1	1	1	1	1	1	1	25.4mA

At RGBISETpin 120kΩ connection

Address 15h <B2 Wave Pattern setup >

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	PB2(3)	0		
D2	PB2(2)	1		
D1	PB2(1)	1		
D0	PB2(0)	1		

PB2(3)	PB2(2)	PB2(1)	PB2(0)	Wave
0	0	0	0	Pattern 1
0	0	0	1	Pattern 2
0	0	1	0	Pattern 3
▪ ▪	▪ ▪	▪ ▪	▪ ▪	▪ ▪
1	1	0	1	Pattern 14
1	1	1	0	Pattern 15
1	1	1	1	Pattern 16

Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●**Register Map - continued**

Address 40h < DC/DC driver function >

BIT	Name	Init	Function	
			0	1
D7	VOUT(1)	0		
D6	VOUT(0)	0		
D5	DCDCMD	0		
D4	DCDCFON	0		
D3	-	-	-	-
D2	-	-	-	-
D1	-	-	-	-
D0	-	-	-	-

VOUT(1)	VOUT(0)	DC/DC output voltage
0	0	3.9V
0	1	4.2V
1	0	4.5V
1	1	4.8V

DCDCMD	DCDCFON	DC/DC Return mode	DC/DC ON/OFF control
0	0	LED pin Return	LED ON
0	1	LED pin Return	LED ON
1	0	Output voltage fixation	LED ON
1	1	Output voltage fixation	Forced ON

Address 41h <LED pin function setup>

BIT	Name	Init	Function	
			0	1
D7	-	-	-	-
D6	-	-	-	-
D5	-	-	-	-
D4	-	-	-	-
D3	RGB2PW(1)	0		
D2	RGB2PW(0)	0		
D1	RGB1PW(1)	0		
D0	RGB1PW(0)	0		

RGB2PW(1)	RGB2PW(0)	R2 connection	G2 connection	B2 connection
0	0	VBAT	VBAT	VBAT
0	1	VBAT	VBAT	VOUT
1	0	VBAT	VOUT	VOUT
1	1	VOUT	VOUT	VOUT

RGB1PW(1)	RGB1PW(0)	R1 connection	G1 connection	B1 connection
0	0	VBAT	VBAT	VBAT
0	1	VBAT	VBAT	VOUT
1	0	VBAT	VOUT	VOUT
1	1	VOUT	VOUT	VOUT

RGB*PW (1:0) does not assume to change dynamically. Please perform a fixed setup per design.
And, do the setup of RGB*PW (1:0) when each LED is Off.
Refer to "●RGB Waveform Setting " for the detailed function of each register of this page.

●RGB LED Driver Operation Description

- Two drivers “RGB1 (R1LED, G1LED, B1LED)” and “RGB2 (R2LED, G2LED, B2LED)” are mounted.
- A slope function is incorporated to control drivers independently.
- Refer to ●RGB Waveform Setting for more information about output waveform setting.
- The LED current can be set via a resistance value (RISET) to be connected to the RGBISET terminal.
  The maximum current value can be derived from the following expression:
  ILEDmax [A] = 3.048 / RISET [kΩ] (Typ)
  However, this setting must be made so that the maximum current value can be less than or equal to 30.48mA. In addition, the RGBISET terminal has an over current protection circuit to prevent the excessive LED current from flowing for low impedance to the ground.
- Connection of each LED of RGB can be set up in VBAT or VOUT by the register RGB1PW (1:0) and RGB2PW (1:0). When Vf is low, it is connected to VBAT, and it is possible that efficiency is raised. When a VBAT connection is chosen, a return route to the DC/DC circuit is interrupted, and it works as a simple constant current driver. In this case, set it up to be less low than the saturation voltage (0.2V) of the fixed electric current circuit.

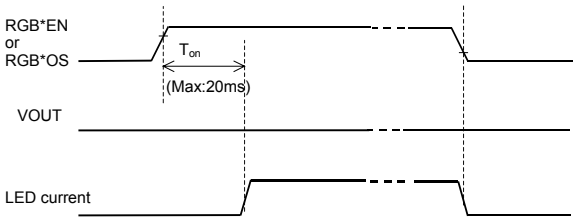


Figure 8. LED electric current When DC/DC isn't used.

●The synchronism of RGB1/RGB2

The period of RGB1 and RGB2 and start, stop timing can be set up independently.
When synchronizes RGB1 and RGB2, You must start an internal counter at the same time under the state of resetting. (Internal Counter is prepared for each of RGB1 and RGB2, so you must reset both.)

<How to reset internal Counter>
Inside Counter can be reset by carrying out one of following actions.

- Reset by hard reset (RSTB_IL). (RGB1, RGB2 is reset together.)
- Reset by soft reset. (RGB1, RGB2 is reset together.)
- It is written register of the current setup (I1・I2), the slope setup, the period setup and the pattern setup.
  Internal Counter of RGB1 is reset when it is written between Address=0Bh from 02h.
  Internal Counter of RGB2 is reset when it is written between Address=15h from 0Ch.
  Counter is reset as to overwriting the same value.

Note)
Internal Counter isn't reset if write RGB1EN =L and RGB2EN =L. (Address=01h).
When it write RGB1EN=L (RGB2EN=L), inside Counter is held, and IC will operate from the held state at next restart.

●**RGB Waveform Setting**

Various kinds of RGB control can be implemented by designating waveform cycles, waveform patterns, current settings 1, 2 and rising/falling slope times.
To activate a RGB waveform, a continuous operation via RGB*EN or a single-shot operation via RGB*OS can be selected.
In addition, when control via the external terminal RGB*CNT is enabled via RGB*MEL, the corresponding LED can be lit in synchronization with the external signal.

1. Waveform cycle
   - A single cycle time is set for a waveform pattern.
   - This setting can be made independently for RGB1 and RGB2.
2. Waveform pattern
   - A pattern in a waveform cycle is set.
   - Sixteen types of waveform patterns can be set in units of waveform patterns.
   - For concrete waveform patterns, refer to the timing diagram shown on the next page.
3. Current settings 1 and 2 (I1, I2)
   - Two currents (I1, I2) in a waveform pattern are set.
   - When the maximum current value is 25.4mA, it is possible to set the current ranging from 0 to 25.4mA with an increment of 0.2mA (128 steps).
   - The polarity of a waveform is determined by the greater-than/ less-than relationship in the current setting.
   - This setting can be made in units of terminals.
4. Rising/falling slope time
   - A current change time during switching between current settings 1 and 2 is set.
   - A time per step (0.2mA) is calculated based on a difference between the currents selected in current settings 1, 2 and a setting slope time.
     For this reason, a time per step (0.2mA) is short when a difference between setting currents I1 and I2 is large.
     In contrast, it is long when a difference between setting currents I1 and I2 is small.
   - Regardless of current settings 1 and 2, a rising slope time applies at current increase and a falling slope time applies at current decrease. For concrete waveform images, refer to the timing diagram shown on the next page.
5. External terminal synchronization control
   When control via the external terminal RGB*CNT is enabled via RGB*MEL, lighting is enabled if the input external signal goes “H.” In contrast, it is disabled if the external input signal goes “L.” In this way, synchronization with the external signal is enabled so that LED can be blinked in conjunction with a ringing tone (a melody signaling a ring tone).

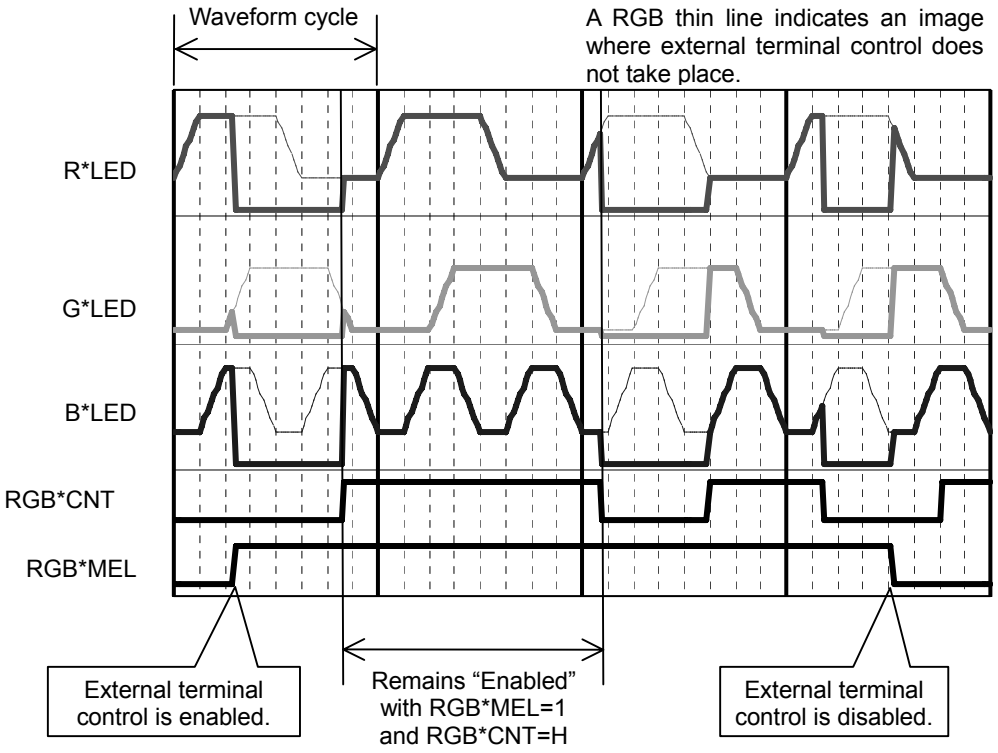


Figure 9.Example of RGB*CNT

●**RGB Waveform Setting - continued**

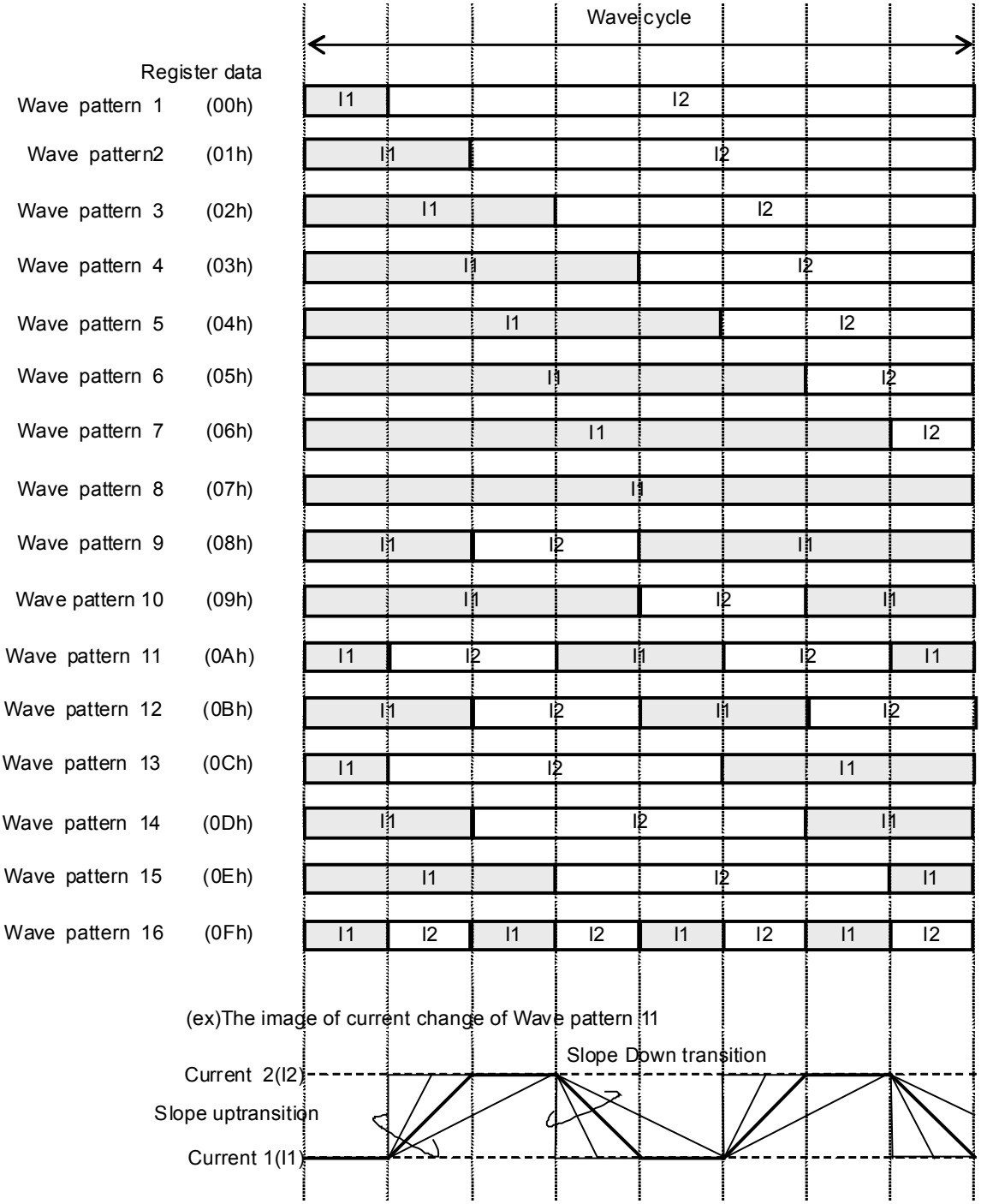


Figure 10. RGB wave setting timing diagram

●**RGB Waveform Setting - continued**

6. Clock I/O

A reference clock I/O function is mounted in this IC chip. When two IC chips are used to extend an illumination capability, clock supply to the other RGB LED driver can be accomplished for synchronization with this LSI chip. This setting can be made via the register.
Clock output can be made with CLKEN=1 and CLKMD=1.
Please refer to the table in Sleep operation mode for details.

7. Sleep operation mode

It can be set as a sleep mode by SLPMD=1 setup. In a sleep mode, all the LED current under lighting operation serves as low consumption operation mode at 0mA. Therefore, an analog block unnecessary for operation can be turned off. In an internal clock sleep mode, a block required for clock generation remains turning on.
Starting sequence of charge pump enters by LED lighting. Therefore, lighting timing changes compared with the normal mode.

CLKEN	CLKMD	FSEL	SLPMD	CLKIO Terminal condition	Illuminations Sleep mode
0	*	*	*	Clock I/O invalid	Normal mode
1	0	1	0	Input (fin=31.25kHz)	Normal mode
			1	Input (fin=31.25kHz)	External clock Sleep mode
	1	0	0	Output (fout=250kHz)	Normal mode
		1	0	Output (fout=31.25kHz)	Normal mode
			1	Output (fout=31.25kHz)	Internal clock Sleep mode

Setup other than the above is prohibition.

●**When two BD2812GU drivers are used and the clock is shared by CLKIO:**

Because a sequence is already programmed within an IC chip for RGB falling, “Enable” shall be set to “OFF” and clock supply shall be continued for at least three clocks so that operations can be performed using external clocks

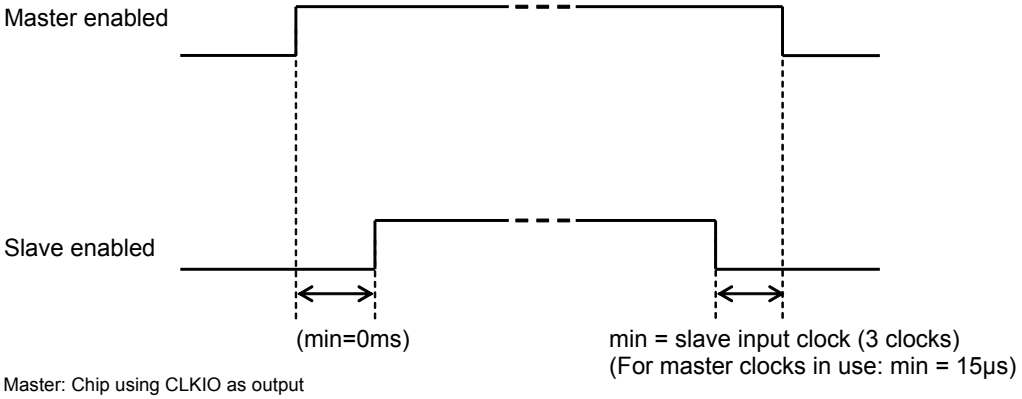


Figure 11. The example of a setting at used two ICs

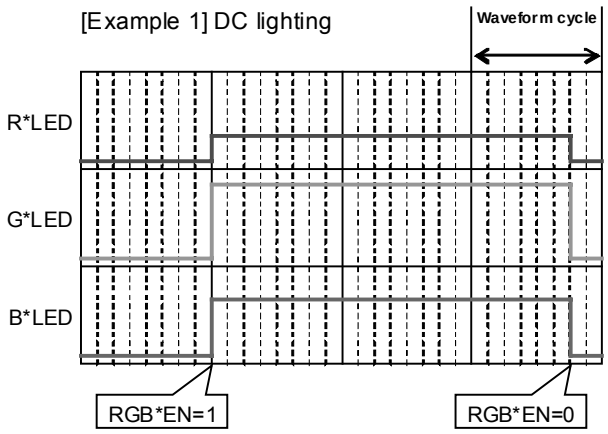
* Even in independent slave mode, its setting “Enable” shall be reset to “OFF” and then clock supply must be continued or 3 clocks or more.
Clock I/O switching shall be avoided during RGB operation.
Enable: CLKEN, RGB1EN, RGB2EN, RGB1OS, RGB2OS

・Setting example

Master side	(clock output side)	RGB waveform setting
↓		
Slave side	(clock input side)	RGB waveform setting
↓		
Master side	Clock output setting CLKEN=1, CLKMD=1	…Performs clock output.
↓		
Slave side	Clock input setting CLKEN=1, CLKMD=0	…Allows clock reception.
↓		
Master side	RGB lighting	
↓		
↓	This duration shall be short as much as possible.	
↓		
Slave side	RGB lighting	

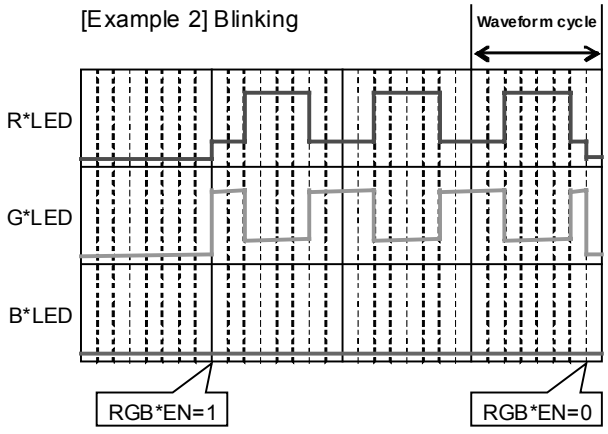
8. RGB waveform setting examples

[Example 1] DC lighting



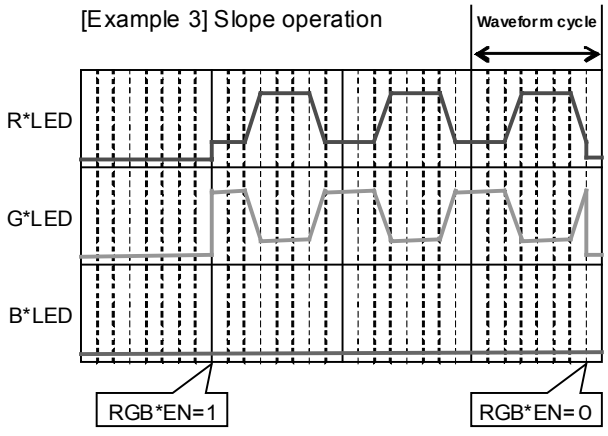
Selecting a waveform pattern 8 causes a continuous normal operation to take place through the setting current 1.

[Example 2] Blinking



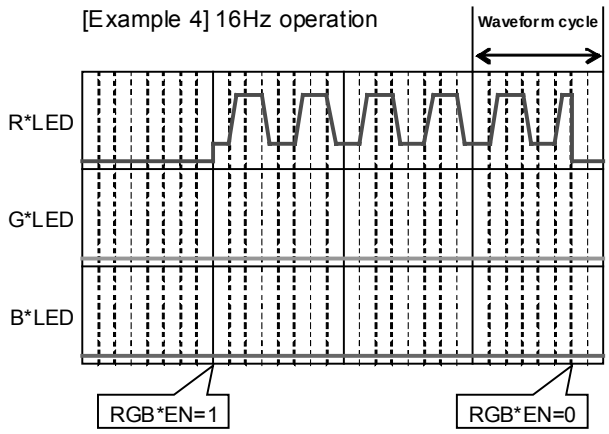
Setting a rising/falling slope time to “0” causes blinking to take place. Phase switching takes place via the setting currents of R and G.

[Example 3] Slope operation



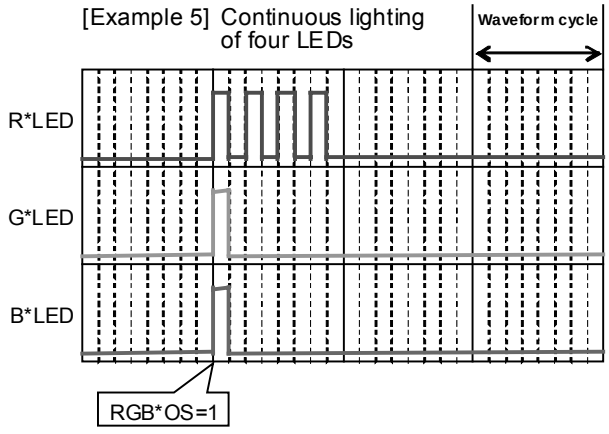
When a rising/falling slope time is longer than the setting made in example 2, a continuous color change is made by slope operation.

[Example 4] 16Hz operation



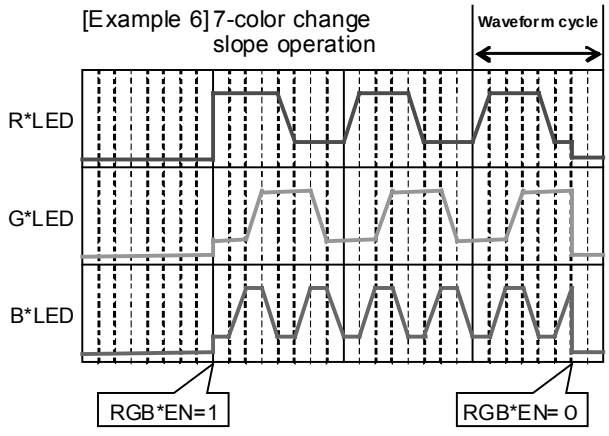
Combining the settings of a waveform pattern 11 and a waveform cycle 131ms causes blinking at a rate of 15.3Hz (approx. 16Hz).

[Example 5] Continuous lighting of four LEDs



This example shows that lighting occurs continuously in the order of white, red, red and red. To achieve this, waveform patterns 16, 1 and RGB*OS single cycle operation need to be combined.

[Example 6] 7-color change slope operation



R, G and B waveform patterns are set in a way that any of R, G and B changes constantly.

9. RGB slope waveforms

・Example of waveform at activation (Waveform pattern=14)

Current setting: I1 < I2

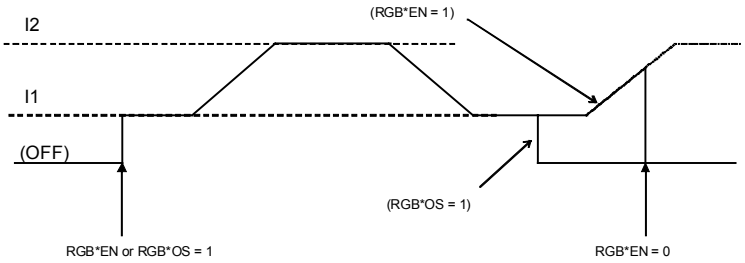


Figure 12. The example 1 of a wave pattern at LED current start-up

Current setting: I1 > I2

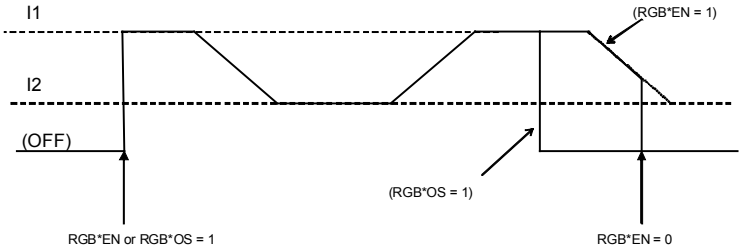


Figure 13. The example 2 of a wave pattern at LED current start-up

・Current difference in each channel (example)

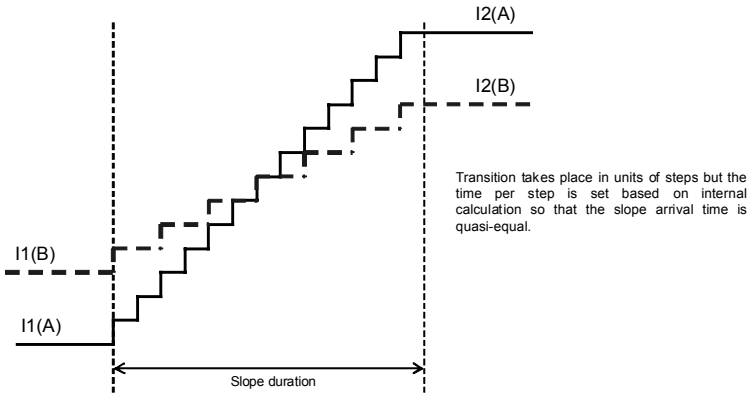


Figure 14. The slope waveform by the difference in an LED current

9. Setting change in slope duration

A slope operation is performed by an internal sequencer.

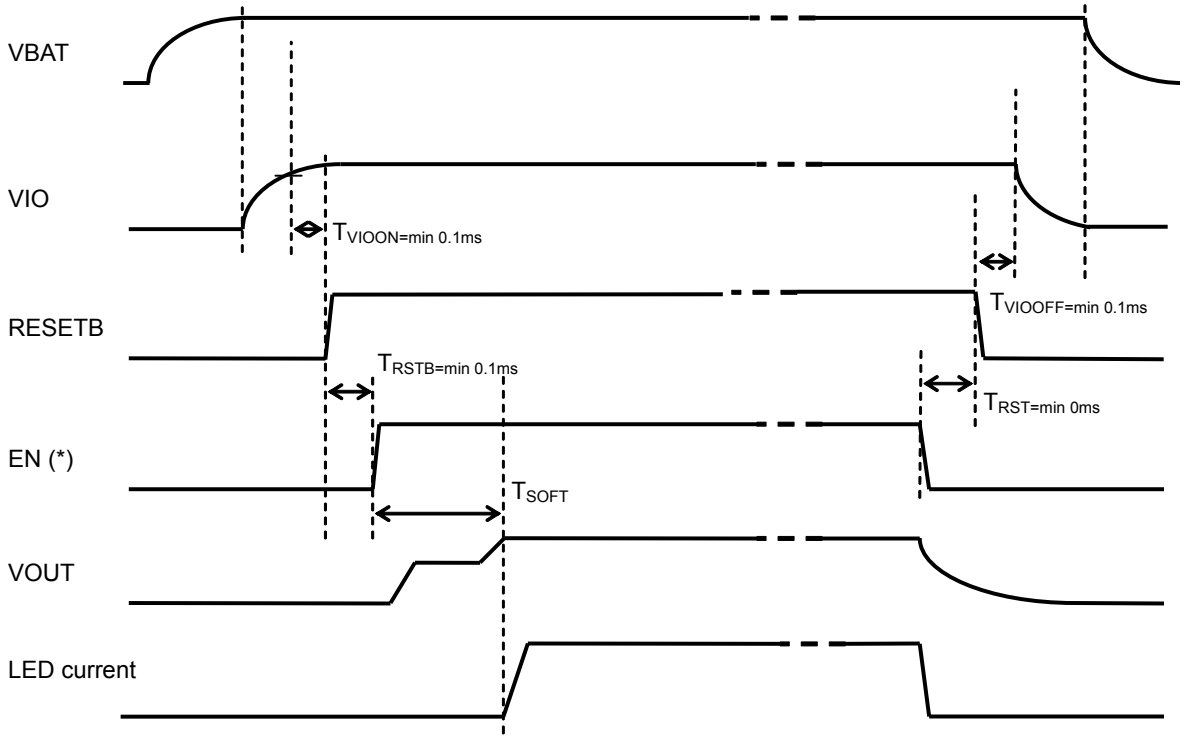
When an attempt is made to change the setting (Address 02h to 15h) in a slope duration, the active slope operation is reset and a newly set slope operation is restarted.

In this case, however, LED lighting stops for a maximum of 16.4ms (OSC frequency=Typ) for synchronization with the internal clock until the operation is restarted.

●**Description of REG Operations**

Activation

The DC/DC circuit is activated when any LED is subject to lighting control (DCDCFON=0).
(However, this is true only when the output (VOUT) of the DC/DC circuit is set as a LED connection destination.)
A soft start function is available to prevent the rush current at DC/DC circuit activation.
Note that voltage should apply to both VBAT and VIO as follows:
DCDCMD=1 must be set in the fixed voltage mode and DCDCMD=DCDCFON=1 must be set when DCDC output takes place regardless of LEDs.



(*) An EN signal means the following in the upper figure.
EN = “MLEDEN” or “W*EN” or “RGB*EN” or “RGB*OS” (= LED The LED lighting control of a setup of connection VOUT)
But, as for Ta > T_{TSD} (Typ: 195° C), a protection function functions, and an EN signal doesn't become effective.
T_{SOFT} changes by the capacitor connected to VOUT and inside OSC.
T_{SOFT} is Typ 200μs (when the output capacitor of VOUT =1.0μF).

Figure 15. DC/DC starting sequence

Over voltage protection/Over current protection

The DC/DC circuit output (VOUT) is provided with an over voltage protection function and an over current protection function. VOUT over voltage detection voltage: approx. 6.0V (during a VOUT voltage rise)
A detection voltage has a hysteresis and its detection cancel voltage is approx. 5.75V (reference design value). In addition, when the VOUT output is short-circuited to GND, the leak current is suppressed via the over current protection function.

●Description of REG Operations - continued

Mode transition

A step-up (pressure rising) multiple switches automatically depending on the VBAT voltage and VOUT terminal voltage.

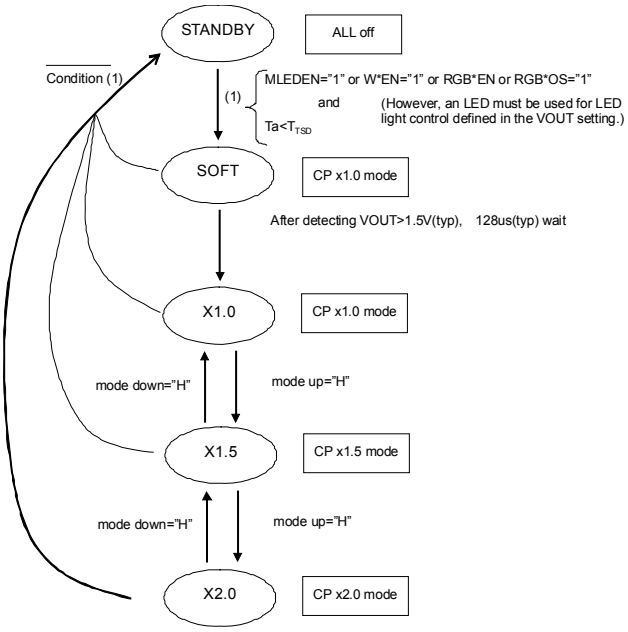


Figure 16. DC/DC state transition diagram

The charge pump mode transits as follows.

<Mode transition: x1.0 → x1.5 → x2.0>

VBAT and VOUT are compared and mode transition is allowed only when the following conditions are satisfied.

Mode transition from x1.0 to x1.5 VBAT ≤ VOUT + (Ron10×Iout) (LED terminal feedback: VOUT = Vf+0.2(Typ)) Mode transition from x1.5 to x2.0 VBAT×1.5 ≤ VOUT + (Ron15×Iout) (LED terminal feedback: VOUT = Vf+0.2(Typ))

Where, Ron10 and Ron15 represent a 0n resistance at a charge pump.
Ron10=1Ω (Typ), Ron15=5Ω (Typ) (design value)

<Mode transition: x2.0 → x1.5 → x1.0>

1. VOUT and VBAT rates are detected and mode transition is performed only when a prescribed rate is exceeded. The rates are as follows:

Mode transition from x1.5 to x1.0 VBAT/VOUT=1.07 (design value) Mode transition from x2.0 to x1.5 VBAT/VOUT=0.96 (design value)

2. If DCDCMD (register00h) '1'→'0' (switch from output voltage fixed mode to LED pin return mode) is operated, a mode down will be performed until it fulfils mode up conditions.

●Description of Other Operations

1. Reset
   There are two types of reset: software reset and hardware reset.
   (1)Software reset
   - Setting the register (SFTRST) to “1” causes all the registers to be initialized.
   - The registers subject to software reset automatically return to zero (Auto Return 0).

   (2)Hardware reset
   - Changing the RESETB terminal setting from “H” to “L” causes a state subject to hardware reset.
   - Attempting hardware reset causes the states of all registers and output terminals to be initialized to their initial values, so that address reception is entirely stopped.
   - Attempting reset in the hardware reset state causes the RESETB terminal state to change from “L” to “H” and vice versa.
   - The RESETB terminal is provided with a filter circuit and a duration of 5μs or less with the terminal set to “L” is not recognized as hardware reset.

   (3) Reset sequence
   - When hardware reset is attempted during software reset, software reset is already cleared when hardware reset is cleared (because the software reset initial value is 0).

2. Thermal shutdown
   The thermal shutdown is effective for LED and OSC portions.
   The thermal shutdown function is activated when the detected temperature is approx. 195°C.
   The detected temperature has a hysteresis and the detection cancel temperature is approx 175°C(reference value in design).

3. I/O portion
   While the RESETB terminal is in “L” state, no input signal is propagated to the IC logic portion because SDA and SCL input buffer operations are all stopped.

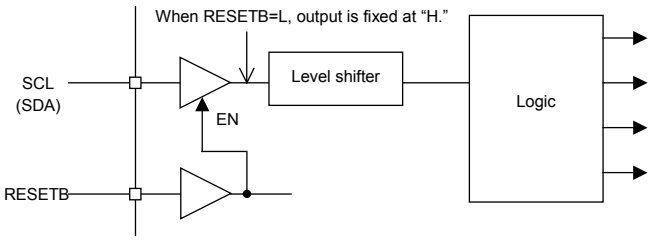


Figure 17. I/O block

Special care should be taken because a current path may be formed via a terminal protection diode, depending on an I/O power-on sequence or an input level.

4. Power on/off sequence
   Voltage shall be applied as follows at driver activation. When a delay element is connected to a VIO voltage source and a reset cancel signal is input to the RESETB terminal, special care should be taken to the rising time of VIO voltage to delay the RESETB signal without fail.

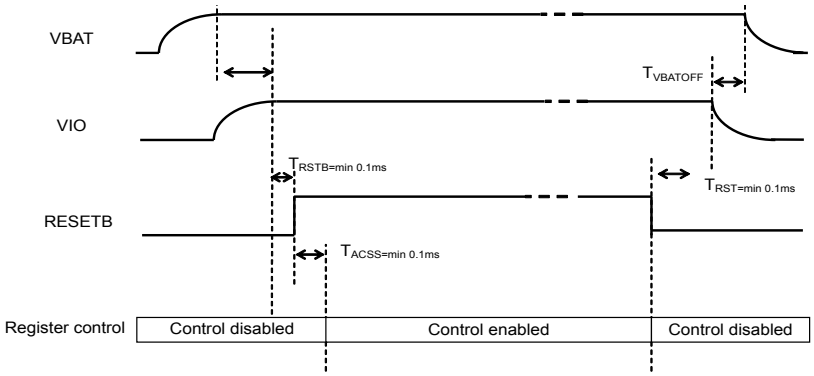


Figure 18. Power supply ON/OFF sequence

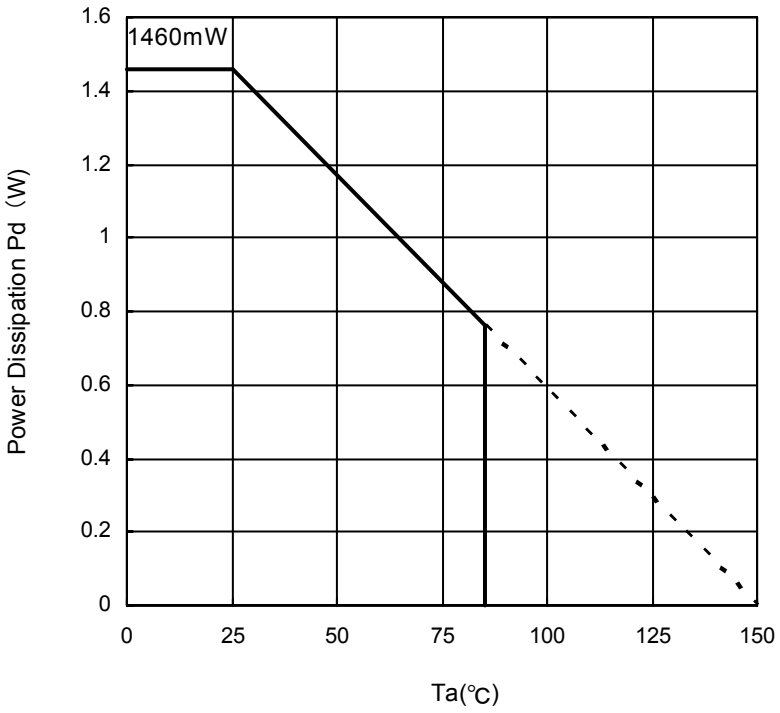
●**Description of Other Operations - continued**

5. Terminating the unused terminals

Be sure to set the test terminals and unused terminals as summarized in the following table.
In addition, refer to the preceding equivalent circuit and terminate the above terminals in a way that no problem occurs during actual use.

T1, T2, T3, T4	Short to GND because pin for test
LED terminals not to be used	Short-circuit these terminals to GND. In this case, don't set the registers related to LEDs not to be used.
RGB1CNT, RGB2CNT	Short-circuit these terminals to GND. (Built-in pull-down resistance)
CLKIO	Short-circuit these terminals to GND. (Built-in pull-down resistance)
ADDSEL	Be sure to short-circuit this terminal to VBAT or GND.

●**Power Dissipation** (On the ROHM's standard board)



Information of the ROHM's standard board
Material: glass-epoxy
Size: 50mm×58mm×1.75mm (8Layer)

Figure 19. Power Dissipation

●Operational Notes

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and ground line
Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) Ground voltage
Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient.

(4) Short circuit between pins and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

(5) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input pins
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then break down of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)
This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) About the pin for the test, the un-use pin
Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to this Datasheet. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

(11) About the rush current
Because the rush current flows momentarily for internal logic instability caused by a power-on sequence or delay, special care should be taken to the power supply coupling capacity, power supply, ground pattern wiring width and wiring.

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority.

●Ordering Information

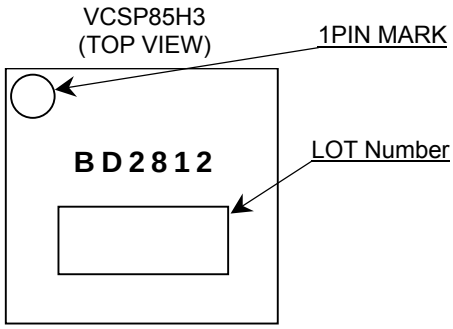
B D 2 8 1 2 G U	-	E 2

Part Number

Package
GU: VCSP85H3

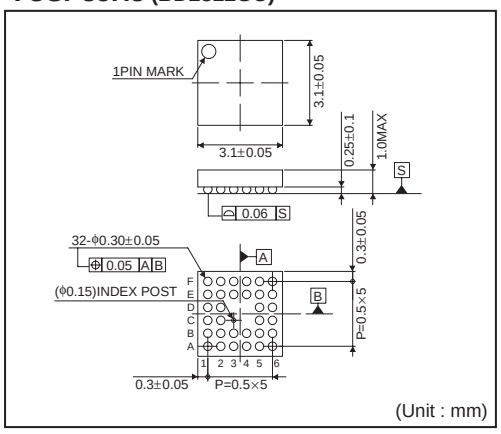
Packaging and forming specification
E2: Embossed tape and reel

●Marking Diagram



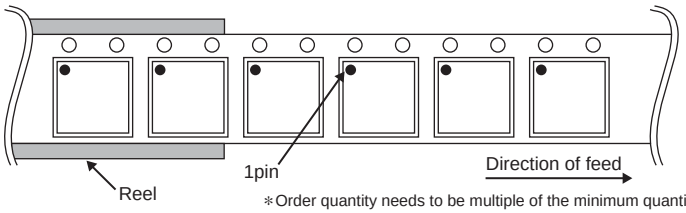
●Physical Dimension Tape and Reel Information

VCSP85H3 (BD2812GU)



<Tape and Reel information>

Tape	Embossed carrier tape (heat sealing method)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●**Revision History**

Date	Revision	Changes
26.Sep.2012	001	New Release

Notice

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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●Precaution for Disposition

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