ROHM's Selection Operational Amplifier/Comparator Series

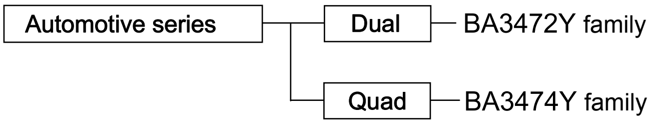
Automotive High Speed with High Voltage Operational Amplifiers

BA3472YFV-C, BA3472YFVM-C, BA3474YFV-C

No.12049EAT25

●Description

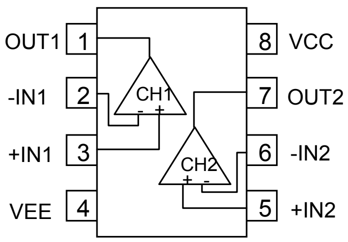
Automotive BA3472/BA3474 family integrate two/four Independent Op-amps and phase compensation capacitors on a single chip and have some features of high-gain, low power consumption, and wide operating voltage range of +3[V] ~ +36[V](single power supply). Especially, characteristics are high slew rate (10V/μs) and high Maximum frequency (4MHz).



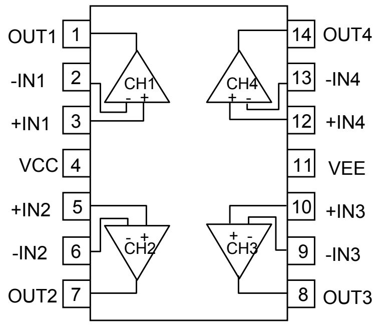
●Characteristics

1) Operable with a single power supply
2) Wide operating supply voltage
   ＋3.0[V]～＋36.0[V](single supply)
   ±1.5[V]～±18.0[V](split supply)
3) Standard Op-Amp. Pin-assignments
4) Internal phase compensation
5) High slew rate : 10[V/μs]
6) Maximum frequency : 4[MHz]
7) High open loop voltage gain
8) Internal ESD protection
   Human body model (HBM) ±5000[V](Typ.)
9) Operable low input voltage around GND level
10) Wide output voltage range
    VEE+0.3[V]～VCC-1.0[V](Typ.)
    with VCC-VEE=30[V]

●Pin Assignment



SSOP-B8 BA3472YFV-C
MSOP8 BA3472YFVM-C



SSOP-B14 BA3474YFV-C

●ABSOLUTE MAXIMUM RATINGS(Ta=25[℃])

○BA3472Y / BA3474Y family

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC-VEE	+36	V
Differential Input Voltage (*1)	Vid	36	V
Input Common-mode Voltage Range	Vicm	(VEE-0.3)～VEE+36	V
Operating Temperature	Topr	-40～+125	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum junction Temperature	Tjmax	150	℃

・This IC is not designed for protection against radioactive rays.

(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VEE.

●OPERATING CONDITION(Ta=-40[℃]～+125[℃])

○BA3472Y / BA3474Y family

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	＋3.0～＋36.0 (Single Supply)	V
		±1.5～±18.0 (Split Supply)	

●ELECTRICAL CHARACTERISTICS

○BA3472Y family (unless otherwise specified VCC=+15[V]、VEE=-15[V], Ta=25[℃])

Parameter	Symbol	range	Guaranteed Limit			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*2)	Vio	full range	-	-	10	mV	Vicm=0[V],VOUT=0[V]
			-	-	10		VCC=5[V],VEE=0[V], Vicm=0[V], VOUT=VCC/2
Input Offset Current (*2)	Iio	25℃	-	6	75	nA	Vicm=0[V],VOUT=0[V]
		full range	-	-	100		
Input Bias Current (*2)	Ib	25℃	-	100	150	nA	Vicm=0[V],VOUT=0[V]
		full range	-	-	200		
Supply Current	ICC	25℃	-	4	5	mA	RL=∞ All Op-Amps
		full range	-	-	5.5		
High Level Output Voltage	VOH	25℃	3.7	4	-	V	VCC=5[V],RL=2[kΩ]
		full range	3.5	-	-		
		25℃	13.7	14	-		RL=10[kΩ]
		full range	13.5	-	-		
		25℃	13.5	-	-		RL=2[kΩ]
Low Level Output Voltage	VOL	25℃	-	0.1	0.3	V	VCC=5[V],RL=2[kΩ]
		full range	-	-	0.6		
		25℃	-	-14.7	-14.3		RL=10[kΩ]
		full range	-	-	-14.0		
		25℃	-	-	-13.5		RL=2[kΩ]
Large Signal Voltage Gain	AV	25℃	80	100	-	dB	RL≧2[kΩ],VOUT=±10[V]
		full range	70	-	-		
Input Common-mode Voltage Range	Vicm	25℃	0	-	VCC-2.0	V	VCC=5[V],VEE=0[V], VOUT=VCC/2
		full range	0	-	VCC-2.6		
Common-mode Rejection Ratio	CMRR	25℃	60	97	-	dB	Vicm=0[V],VOUT=0[V]
Power Supply Rejection Ratio	PSRR	25℃	60	97	-	dB	Vicm=0[V],VOUT=0[V]
Output Source Current (*3)	IOH	25℃	10	30	-	mA	VIN+=1[V],VIN=0[V], VOUT=0[V], only 1CH output short
		full range	10	-	-		
Output Sink Current (*3)	IOL	25℃	20	30	-	mA	VIN+=0[V],VIN=1[V], VOUT=5[V], only 1CH output short
		full range	20	-	-		
Slew Rate	SR	25℃	-	10	-	V/μs	Av=1,Vin=-10[V] to +10[V], RL=2[kΩ]
		full range	5	-	-		

(*2) Absolute value.

(*3) Under the high temperature environment, consider the power dissipation of IC when select the output current.
When output terminal short circuits continuously, the output current reduce to climb temperature inside IC by flash.

●ELECTRICAL CHARACTERISTICS

○BA3474Y family (unless otherwise specified VCC=+15[V]、VEE=-15[V], Ta=25[℃])

Parameter	Symbol	range	Guaranteed Limit			Unit	Condition
			Min.	Typ.	Max.		
Input Offset Voltage (*4)	Vio	full range	-	-	10	mV	Vicm=0[V],VOUT=0[V]
			-	-	10		VCC=5[V],VEE=0[V], Vicm=0[V], VOUT=VCC/2
Input Offset Current (*4)	Iio	25℃	-	6	75	nA	Vicm=0[V],VOUT=0[V]
		full range	-	-	100		
Input Bias Current (*4)	Ib	25℃	-	100	150	nA	Vicm=0[V],VOUT=0[V]
		full range	-	-	200		
Supply Current	ICC	25℃	-	8	10	mA	RL=∞ All Op-Amps
		full range	-	-	11		
High Level Output Voltage	VOH	25℃	3.7	4	-	V	VCC=5[V],RL=2[kΩ]
		full range	3.5	-	-		
		25℃	13.7	14	-		RL=10[kΩ]
		full range	13.5	-	-		
		25℃	13.5	-	-		RL=2[kΩ]
Low Level Output Voltage	VOL	25℃	-	0.1	0.3	V	VCC=5[V],RL=2[kΩ]
		full range	-	-	0.6		
		25℃	-	-14.7	-14.3		RL=10[kΩ]
		full range	-	-	-14.0		
		25℃	-	-	-13.5		RL=2[kΩ]
Large Signal Voltage Gain	AV	25℃	80	100	-	dB	RL≧2[kΩ],VOUT=±10[V]
		full range	70	-	-		
Input Common-mode Voltage Range	Vicm	25℃	0	-	VCC-2.0	V	VCC=5[V],VEE=0[V], VOUT=VCC/2
		full range	0	-	VCC-2.6		
Common-mode Rejection Ratio	CMRR	25℃	60	97	-	dB	Vicm=0[V],VOUT=0[V]
Power Supply Rejection Ratio	PSRR	25℃	60	97	-	dB	Vicm=0[V],VOUT=0[V]
Output Source Current (*5)	IOH	25℃	10	30	-	mA	VIN+=1[V],VIN=0[V], VOUT=0[V], only 1CH output short
		full range	10	-	-		
Output Sink Current (*5)	IOL	25℃	20	30	-	mA	VIN+=0[V],VIN=1[V], VOUT=5[V], only 1CH output short
		full range	20	-	-		
Slew Rate	SR	25℃	-	10	-	V/μs	Av=1,Vin=-10[V] to +10[V], RL=2[kΩ]
		full range	5	-	-		

(*4) Absolute value.

(*5) Under the high temperature environment, consider the power dissipation of IC when select the output current.
When output terminal short circuits continuously, the output current reduce to climb temperature inside IC by flash.

●Reference Data BA3472Y family

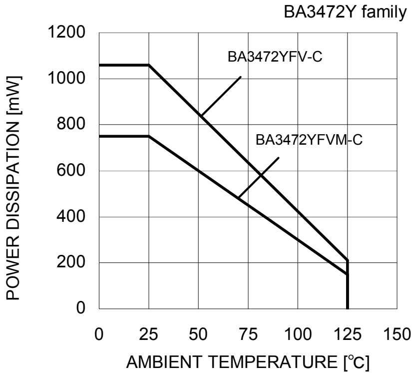


Fig. 1
Derating Curve

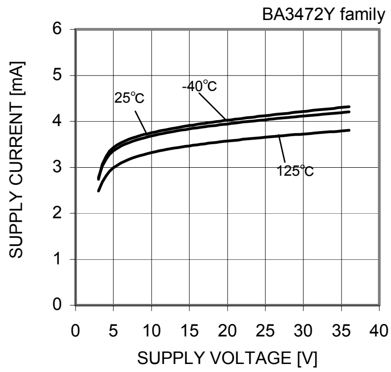


Fig. 2
Supply Current - Supply Voltage

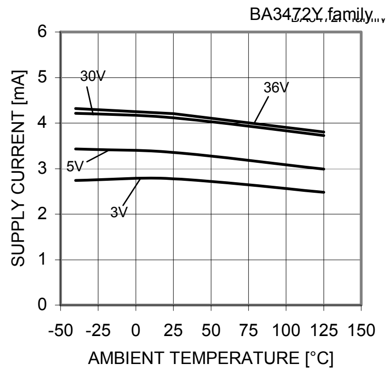


Fig. 3
Supply Current - Ambient Temperature

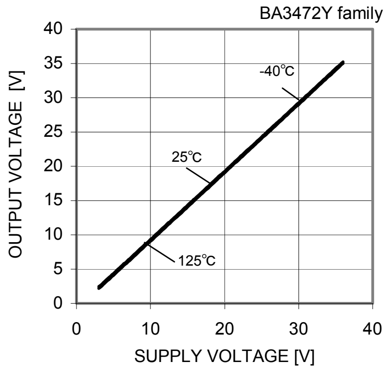


Fig. 4
High level Output Voltage
- Supply Voltage
(RL=10kΩ)

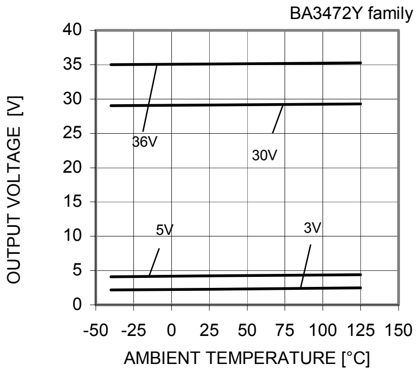


Fig. 5
High level Output Voltage
- Ambient Temperature
(RL=10kΩ)

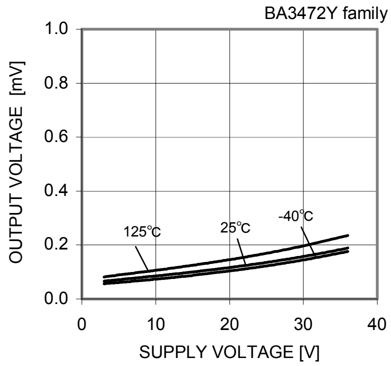


Fig. 6
Low level Output Voltage
- Supply Voltage
(RL=10kΩ)

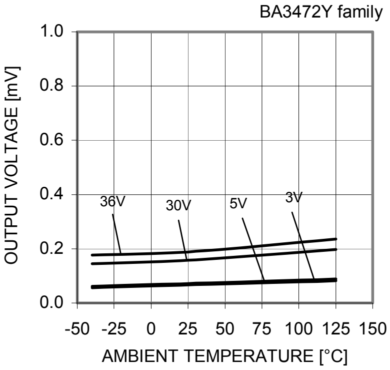


Fig. 7
Low level Output Voltage
- Ambient Temperature
(RL=10kΩ)

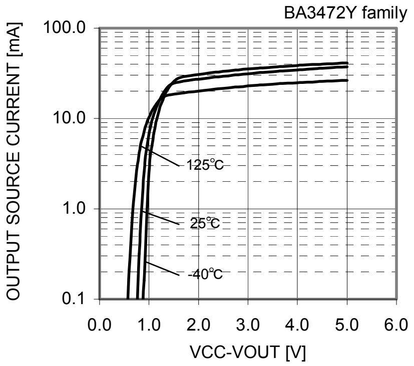


Fig.8
Output Source Current - (VCC-VOUT)
(VCC/VEE = 5[V]/0[V])

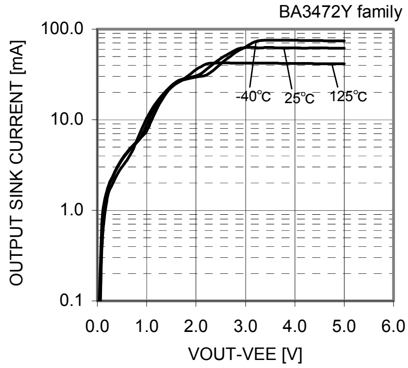


Fig. 9
Output Source Current - (VOUT-VEE)
(VCC/VEE = 5[V]/0[V])

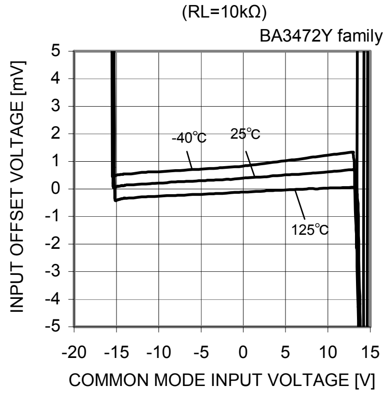


Fig. 10
Input Offset Voltage -
Common Mode Input Voltage
(VCC/VEE = 15[V]/-15[V])

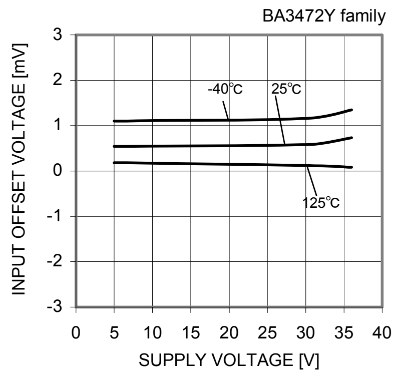


Fig. 11
Input Offset Voltage - Supply Voltage

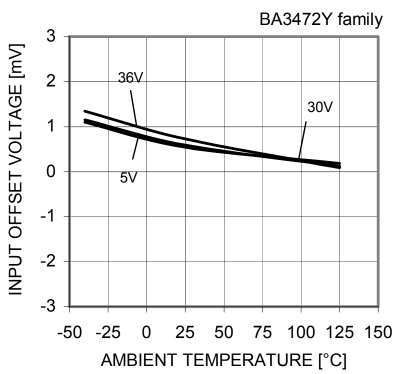


Fig. 12
Input Offset Voltage - Ambient Temperature

(*)The data above is ability value of sample, it is not guaranteed

●Reference Data BA3472Y family

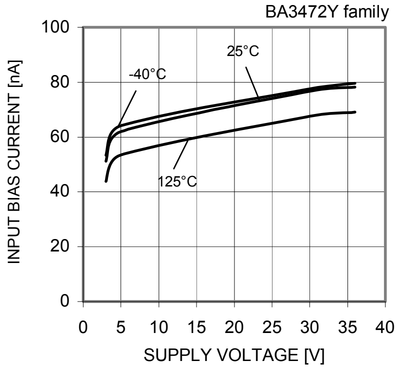


Fig. 13
Input Bias Current - Supply Voltage

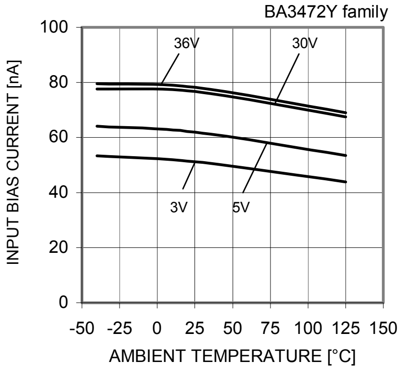


Fig. 14
Input Bias Current - Ambient Temperature

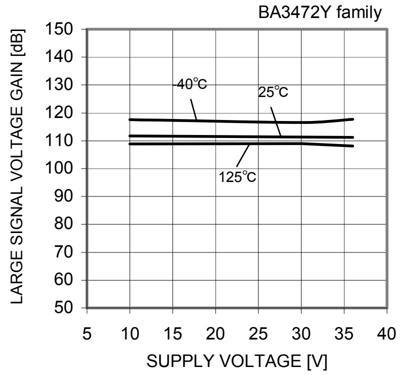


Fig. 15
Large Signal Voltage Gain
- Supply Voltage

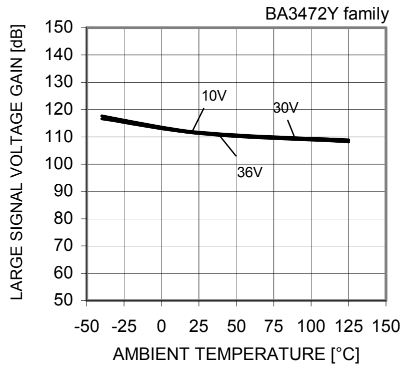


Fig. 16
Large Signal Voltage Gain
- Ambient Temperature

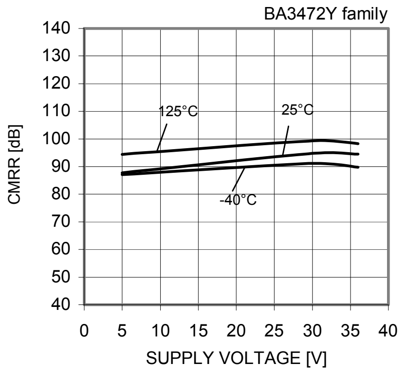


Fig. 17
Common Mode Rejection Ratio
- Supply Voltage

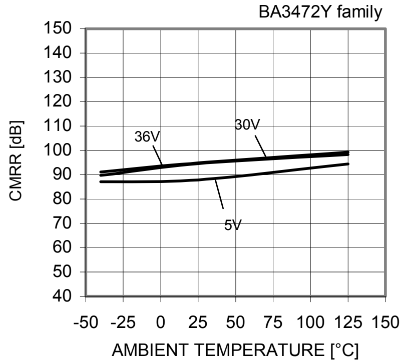


Fig. 18
Common Mode Rejection Ratio
- Ambient Temperature

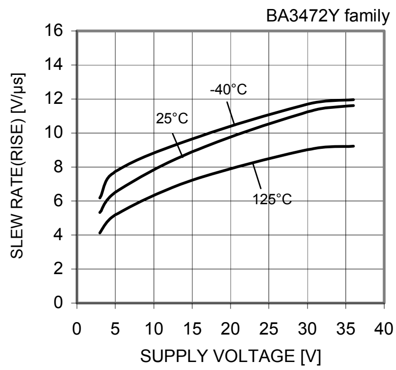


Fig. 19
Slew Rate L-H - Supply Voltage
(RL=10kΩ)

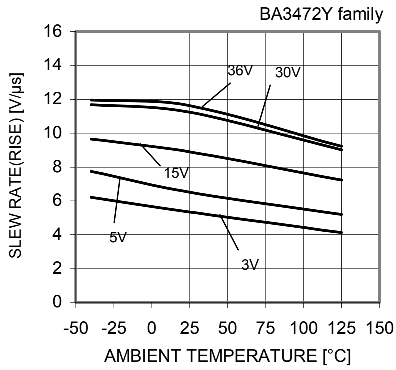


Fig. 20
Slew Rate L-H Ambient Temperature
(RL=10kΩ)

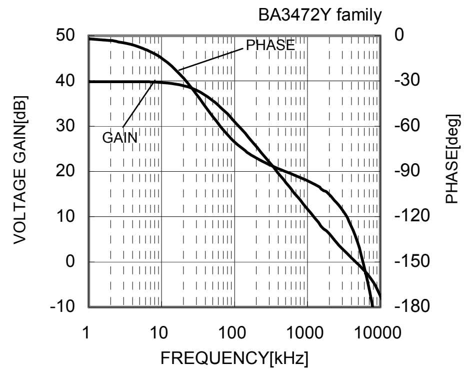


Fig. 21
Voltage Gain - Frequency
(VCC=7.5[V]/-7.5[V], Av=40[dB],
RL=2[kΩ], CL=100[pF], Ta=25[°C])

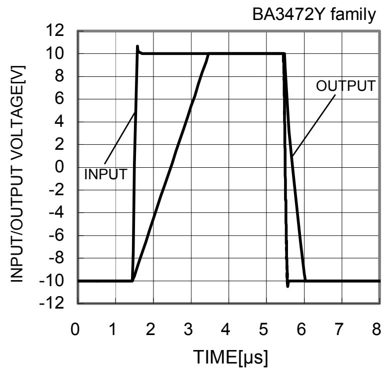


Fig. 22
Input / Output Voltage - Time
(VCC/VEE=15[V]/-15[V], Av=0dB,
RL=2[kΩ], CL=100[pF], Ta=25[°C])

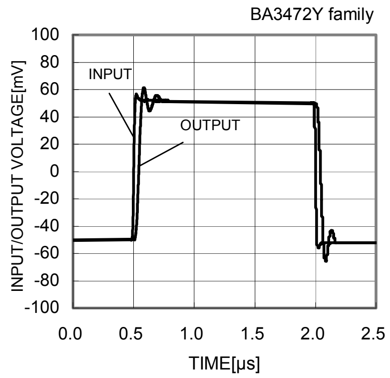


Fig. 23
Input / Output Voltage - Time
(VCC/VEE=15[V]/-15[V], Av=0dB,
RL=2[kΩ], CL=100[pF], Ta=25[°C])

(*)The data above is ability value of sample, it is not guaranteed

●Reference Data BA3474Y family

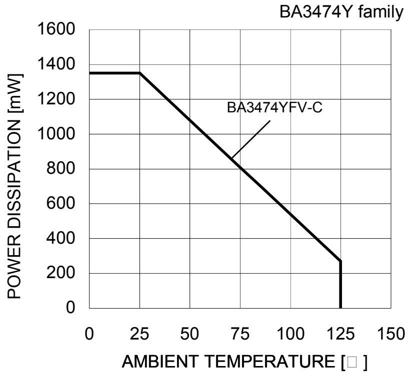


Fig. 24
Derating Curve

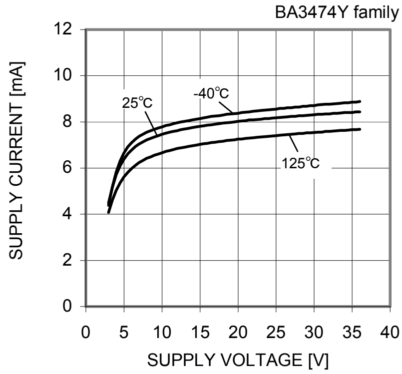


Fig. 25
Supply Current - Supply Voltage

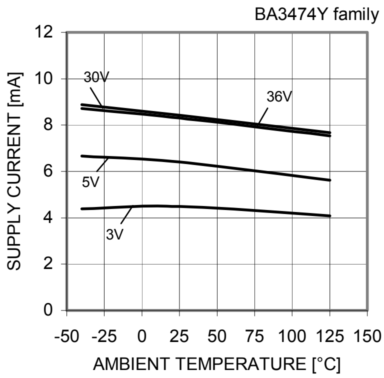


Fig. 26
Supply Current - Ambient Temperature

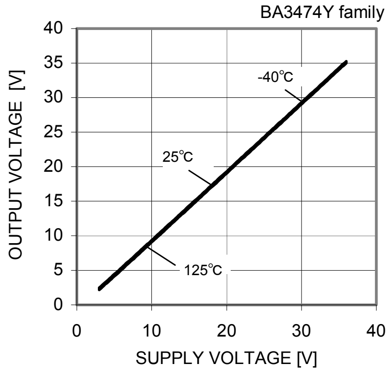


Fig. 27
High level Output Voltage
- Supply Voltage
(RL=10kΩ)

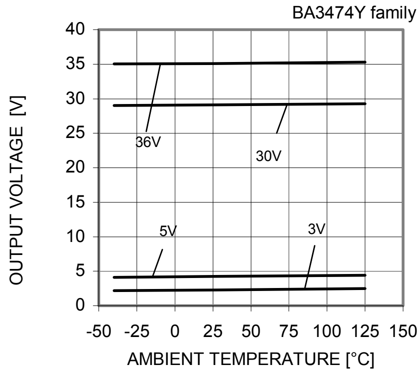


Fig. 28
High level Output Voltage
- Ambient Temperature
(RL=10kΩ)

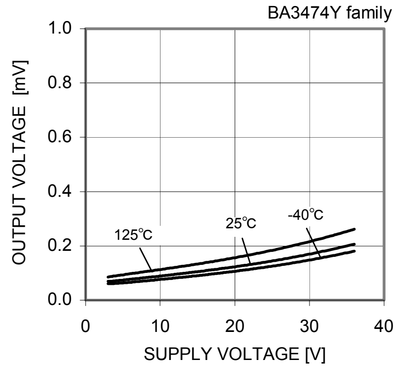


Fig. 29
Low level Output Voltage
- Supply Voltage
(RL=10kΩ)

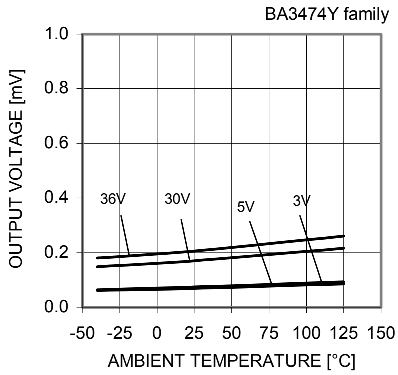


Fig. 30
Low level Output Voltage
- Ambient Temperature
(RL=10kΩ)

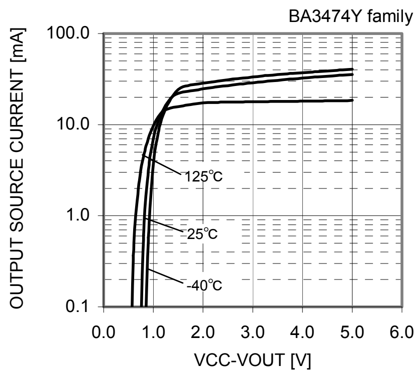


Fig. 31
Output Source Current - (VCC-VOUT)
(VCC/VEE = 5[V]/0[V])

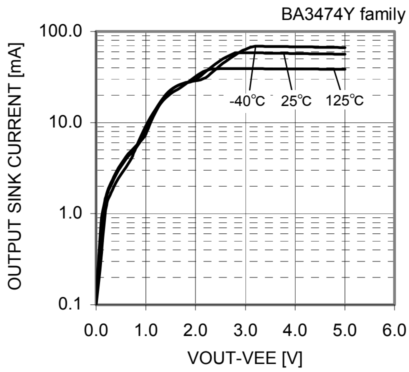


Fig. 32
Output Source Current - (VOUT-VEE)
(VCC/VEE = 5[V]/0[V])

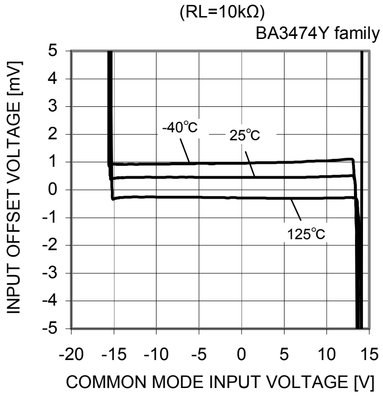


Fig. 33
Input Offset Voltage -
Common Mode Input Voltage
(VCC/VEE = 15[V]/-15[V])

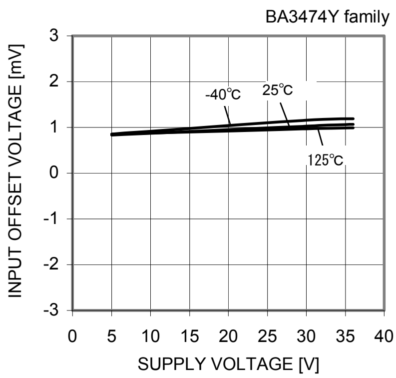


Fig. 34
Input Offset Voltage - Supply Voltage

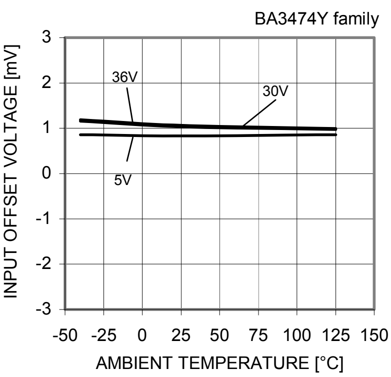


Fig. 35
Input Offset Voltage - Ambient Temperature

(*)The data above is ability value of sample, it is not guaranteed

●Reference Data BA3474Y family

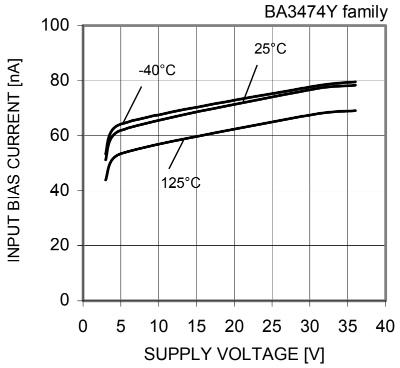


Fig. 36
Input Bias Current - Supply Voltage

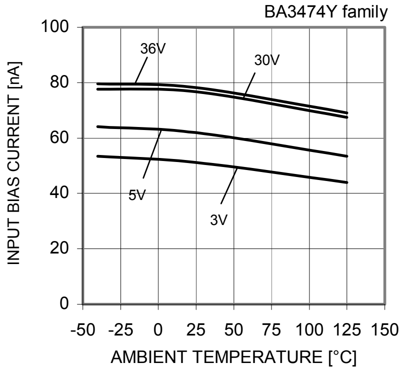


Fig. 37
Input Bias Current - Ambient Temperature

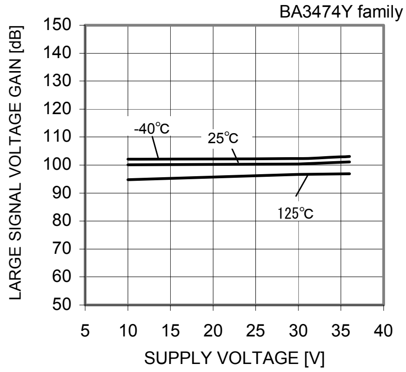


Fig. 38
Large Signal Voltage Gain
- Supply Voltage

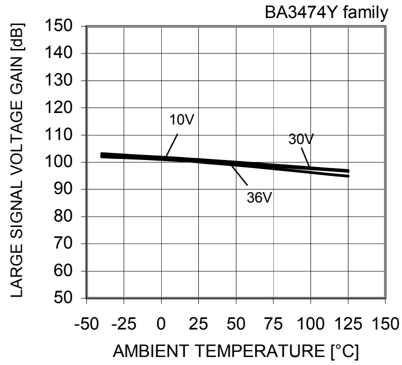


Fig. 39
Large Signal Voltage Gain
- Ambient Temperature

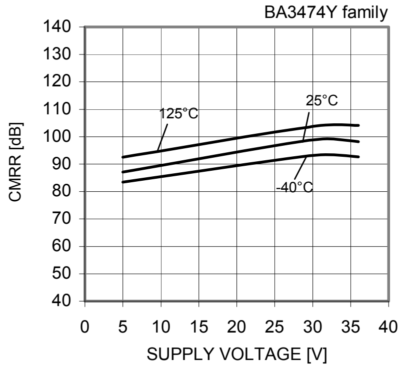


Fig. 40
Common Mode Rejection Ratio
- Supply Voltage

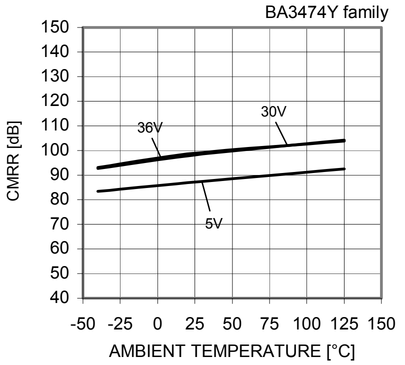


Fig. 41
Common Mode Rejection Ratio
- Ambient Temperature

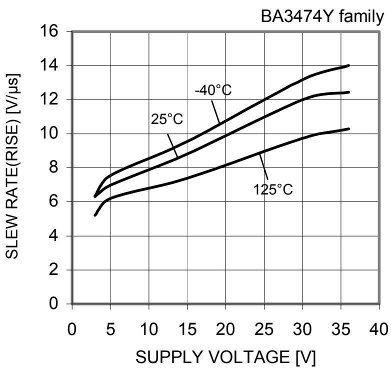


Fig. 42
Slew Rate L-H - Supply Voltage
(RL=10kΩ)

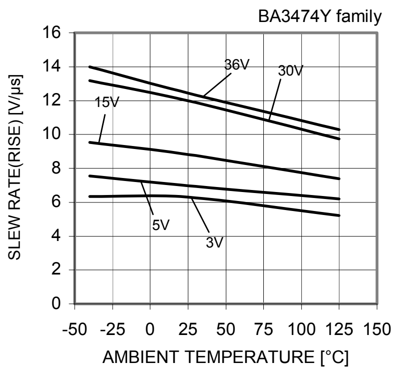


Fig. 43
Slew Rate L-H Ambient Temperature
(RL=10kΩ)

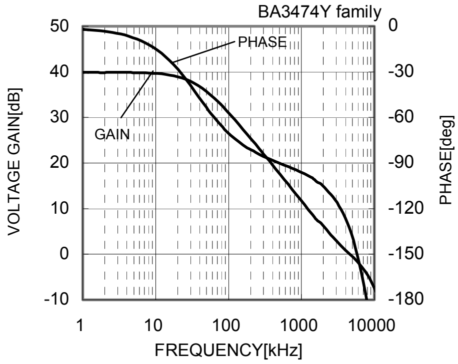


Fig. 44
Voltage Gain - Frequency
(VCC=7.5[V]/-7.5[V], Av=40[dB],
RL=2[kΩ], CL=100[pF], Ta=25[°C])

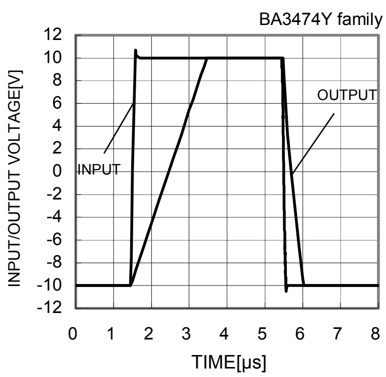


Fig. 45
Input / Output Voltage - Time
(VCC/VEE=15[V]/-15[V], Av=0dB,
RL=2[kΩ], CL=100[pF], Ta=25[°C])

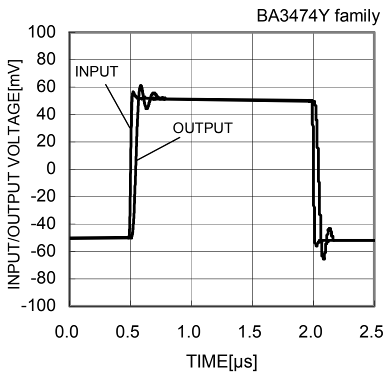


Fig. 46
Input / Output Voltage - Time
(VCC/VEE=15[V]/-15[V], Av=0dB,
RL=2[kΩ], CL=100[pF], Ta=25[°C])

(*)The data above is ability value of sample, it is not guaranteed

●Schematic diagram

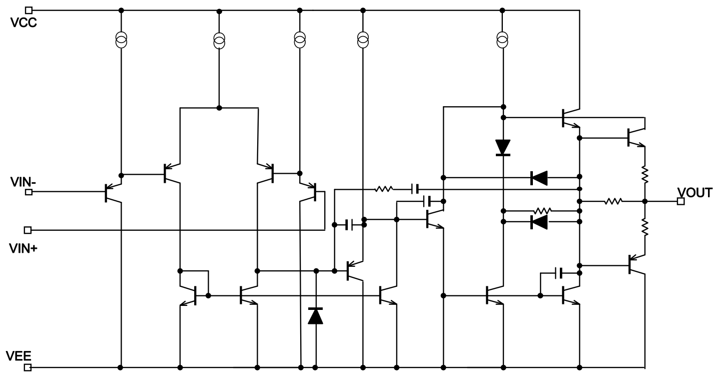


Fig.47 Schematic diagram (one channel only)

●Test circuit1 NULL method

VCC,VEE,EK,Vicm Unit : [V]

Parameter	VF	S1	S2	S3	VCC	VEE	EK	Vicm	Calculation
Input Offset Voltage	VF1	ON	ON	OFF	15	-15	0	0	1
Input Offset Current	VF2	OFF	OFF	OFF	15	-15	0	0	2
Input Bias Current	VF3	OFF	ON	OFF	15	-15	0	0	3
	VF4	ON	OFF						
Large Signal Voltage Gain	VF5	ON	ON	ON	15	-15	＋10	0	4
	VF6				15	-15	-10	0	
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	VF7	ON	ON	OFF	15	-15	0	-15	5
	VF8				15	-15	0	13	
Power Supply Rejection Ratio	VF9	ON	ON	OFF	2	-2	0	0	6
	VF10				18	-18	0	0	

－Calculation－

1. Input Offset Voltage (Vio)

$$Vio = \frac{|VF1|}{1 + Rf / Rs} \quad [V]$$

2. Input Offset Current (Iio)

$$Iio = \frac{|VF2-VF1|}{Ri \times (1 + Rf / Rs)} \quad [A]$$

3. Input Bias Current (Ib)

$$Ib = \frac{|VF4-VF3|}{2 \times Ri \times (1 + Rf / Rs)} \quad [A]$$

4. Large Signal Voltage Gain (Av)

$$Av = 20 \times Log \frac{\Delta EK \times (1+Rf/Rs)}{|VF5-VF6|} \quad [dB]$$

5. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20 \times Log \frac{\Delta Vicm \times (1+Rf/Rs)}{|VF8-VF7|} \quad [dB]$$

6. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20 \times Log \frac{\Delta Vcc \times (1+Rf/Rs)}{|VF10-VF9|} \quad [dB]$$

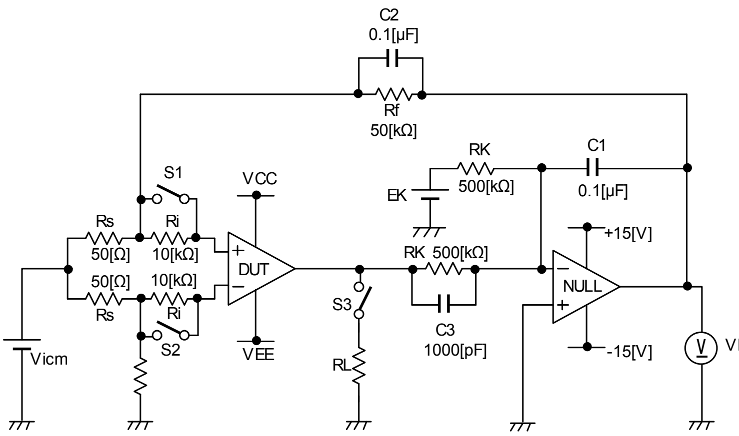


Fig.48 Test circuit 1 (one channel only)

●Test circuit2 switch condition

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12	SW 13	SW 14
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
High Level Output Voltage	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
Low Level Output Voltage	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Equivalent Input Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

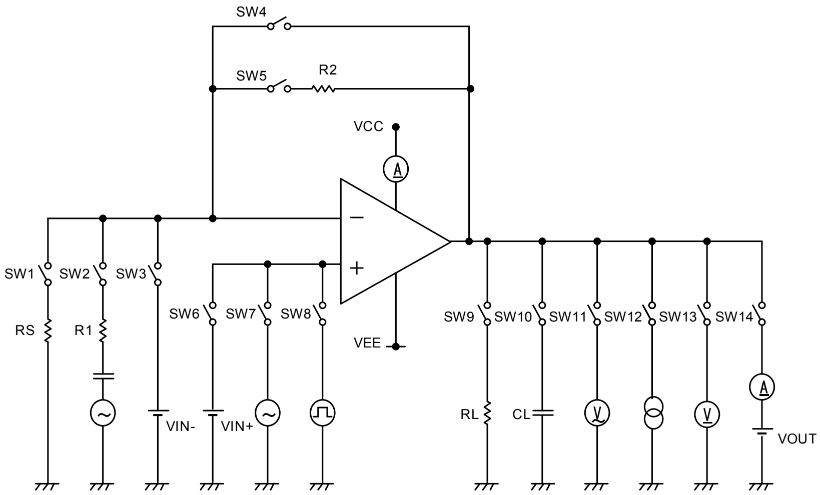


Fig.49 Test circuit 2 (one channel only)

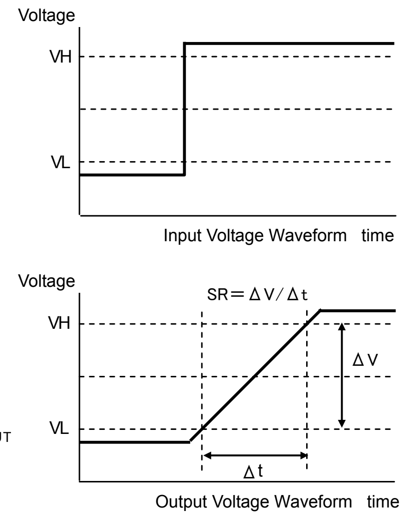
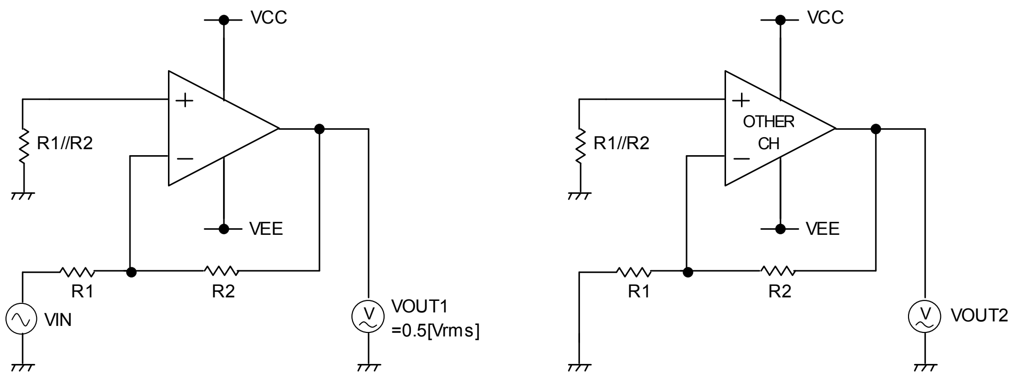


Fig.50 Slew rate input output wave

●Test circuit3 Channel separation



$$CS = 20 \times \log \frac{100 \times VOUT1}{VOUT2}$$

Fig.51 Test circuit 3

●Examples of circuit

○Voltage follower

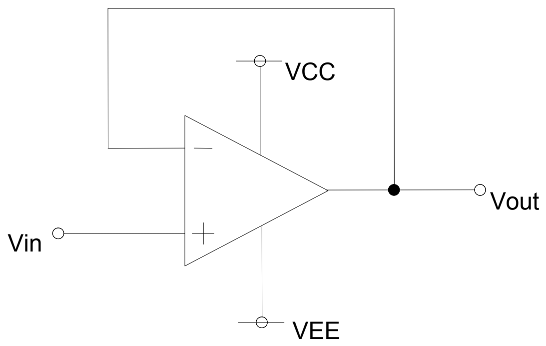


Fig. 52 Voltage follower circuit

Voltage gain is 0 [dB].
This circuit controls output voltage (Vout) equal input voltage (Vin), and keeps Vout with stable because of high input impedance and low output impedance.
Vout is shown next formula.
Vout=Vin

○Inverting amplifier

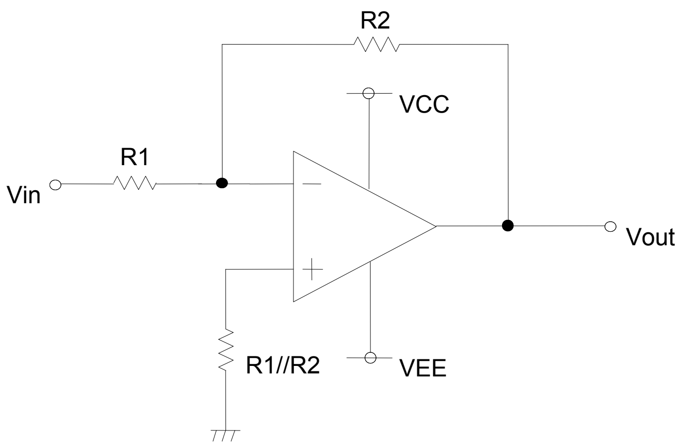


Fig. 53 Inverting amplifier circuit

For inverting amplifier, Vi(b) Derating curve voltage gain decided R1 and R2, and phase reversed voltage is outputted.
Vout is shown next formula.
Vout=-(R2/R1)・Vin
Input impedance is R1.

○Non-inverting amplifier

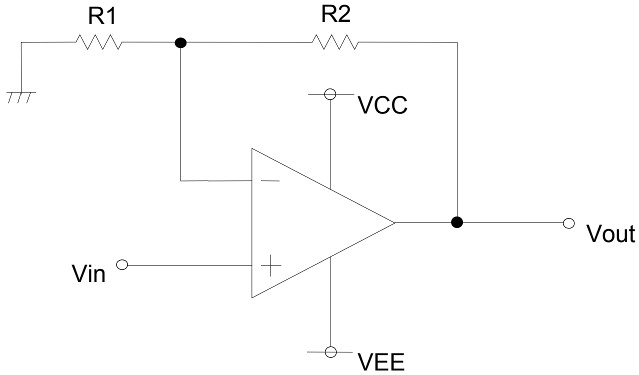


Fig. 54 Non-inverting amplifier circuit

For non-inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase is same with Vin.
Vout is shown next formula.
Vout=(1 + R2/R1)・Vin
This circuit realizes high input impedance because Input impedance is operational amplifier's input Impedance.

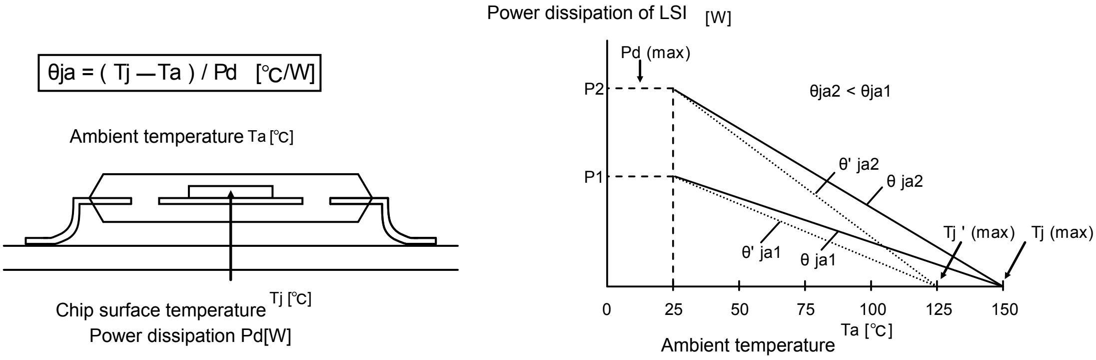
●Derating curves

Power dissipation(total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicatesthis heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θja[℃/W].The temperature of IC inside the package can be estimated by this thermal resistance. Fig.55(a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below:

$$\theta ja = (Tj - Ta) / Pd \quad [℃/W] \quad \cdot\cdot\cdot\cdot\cdot \quad (\mathrm{I})$$

Derating curve in Fig.55(b) indicates power that can be consumed by IC with reference to ambient temperature.Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient iis determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package,ambient temperature, package condition, wind velocity, etc even when the same of package is used.

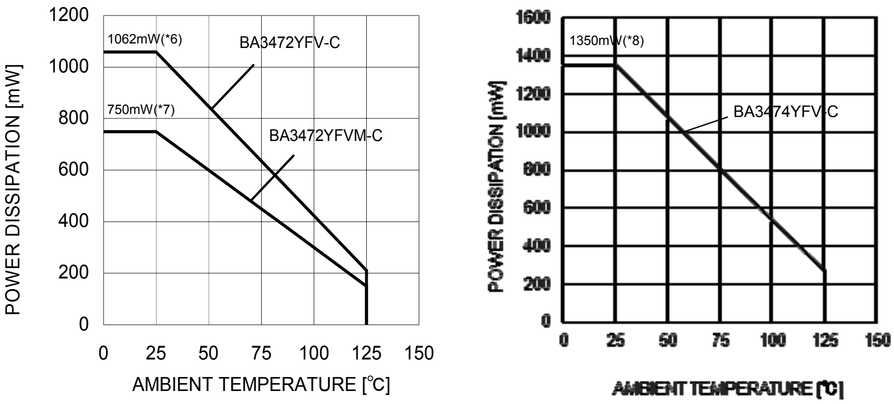
Thermal reduction curve indicates a reference value measured at a specified condition. Fig.56(c),(d) show a derating curve for an example of BA3472Y, BA3474Y.



(a) Thermal resistance (b) Derating curve

Fig. 55 Thermal resistance and Derating curve

<Reference>
When the part is mounted on 70mm x 70mm x 1.6mm 4 layer Glass Epoxy PCB with 70mm x 70mm full copper area, Pd at 125℃ is 270mW so Vcc has to be below 22V.



(c) BA3472Y family (d) BA3474Y family

(*6)	(*7)	(*8)	Unit
8.5	6.0	10.8	[mW/℃]

When using the unit above Ta=25[℃], subtract the value above per degree [℃].

Derating curve
Mounted on a glass epoxy 4 layers
PCB 70[mm]×70[mm]×1.6[mm]
(70[mm]×70[mm] full copper area)

Fig. 56 Derating curve

<Reference>
When the part is mounted on 70mm x 70mm x 1.6mm 4 layer Glass Epoxy PCB with 70mm x 70mm full copper area, Pd at 125℃ is 270mW so Vcc has to be below 22V.

●Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms.
Please note that item names, symbols and their meanings may differ from those on another manufacturer's documents.

1. Absolute maximum ratings
The absolute maximum ratings are values that should never be exceeded, since doing so may result in deterioration of electrical characteristics or damage to the part itself as well as peripheral components.

1.1 Power supply voltage (VCC-VEE)
Expresses the maximum voltage that can be supplied between the positive and negative supply terminals without causing deterioration of the electrical characteristics or destruction of the internal circuitry.

1.2 Differential input voltage (Vid)
Indicates the maximum voltage that can be supplied between the non-inverting and inverting terminals without damaging the IC.

1.3 Input common-mode voltage range (Vicm)
Signifies the maximum voltage that can be supplied to non-inverting and inverting terminals without causing deterioration of the characteristics or damage to the IC itself. Normal operation is not guaranteed within the common-mode voltage range of the maximum ratings – use within the input common-mode voltage range of the electric characteristics instead.

1.4 Power dissipation (Pd)
Indicates the power that can be consumed by a particular mounted board at ambient temperature (25℃). For packaged products, Pd is determined by the maximum junction temperature and the thermal resistance.

2. Electrical characteristics

2.1 Input offset voltage (Vio
Signifies the voltage difference between the non-inverting and inverting terminals. It can be thought of as the input voltage difference required for setting the output voltage to 0 V.

2.2 Input offset current (Iio)
Indicates the difference of input bias current between the non-inverting and inverting terminals.

2.3 Input bias current (Ib)
Denotes the current that flows into or out of the input terminal, it is defined by the average of the input bias current at the non-inverting terminal and the input bias current at the inverting terminal.

2.4 Circuit current (ICC)
Indicates the current of the IC itself that flows under specified conditions and during no-load steady state.

2.5 Maximum output voltage(VOM)
Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into high-level output voltage and low-level output voltage.

2.6 Large signal voltage gain (AV)
The amplifying rate (gain) of the output voltage against the voltage difference between non-inverting and inverting terminals, it is (normally) the amplifying rate (gain) with respect to DC voltage.
AV = (output voltage fluctuation) / (input offset fluctuation)

2.7 Input common-mode voltage range (Vicm)
Indicates the input voltage range under which the IC operates normally.

2.8 Common-mode rejection ratio (CMRR)
Signifies the ratio of fluctuation of the input offset voltage when the in-phase input voltage is changed (DC fluctuation).
CMRR = (change in input common-mode voltage) / (input offset fluctuation)

2.9 Power supply rejection ratio (PSRR)
Denotes the ratio of fluctuation of the input offset voltage when supply voltage is changed (DC fluctuation).
SVR = (change in power supply voltage) / (input offset fluctuation)

2.10 Channel separation (CS)
Expresses the amount of fluctuation of the input offset voltage or output voltage with respect to the change in the output voltage of a driven channel.

2.11 Slew rate (SR)
Indicates the time fluctuation ratio of the output voltage when an input step signal is supplied.

2.12 Gain bandwidth product (GBW)
The product of the specified signal frequency and the gain of the op-amp at such frequency, it gives the approximate value of the frequency where the gain of the op-amp is 1 (maximum frequency, and unity gain frequency)

●Application example

(1) Absolute maximum ratings

Absolute maximum ratings are the values which indicate the limits, within which the given voltage range can be safely charged to the terminal. However, it does not guarantee the circuit operation.

(2) The example of disabled circuit application

When there is a circuit not in use, it is recommended to make the non-inverting input terminal be the potential in the common-mode input voltage range like in Fig.1. Circuit operation is guaranteed within "Operating Conditions".

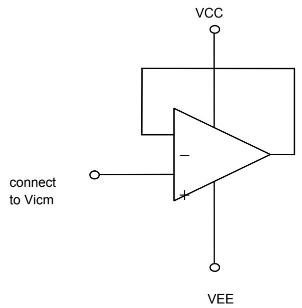


Fig.57 The example of disabled circuit

(3) Applied voltage to the input terminal

For normal circuit operation of operational amplifier, please input voltage for its input terminal within input common mode voltage VCC-2.0[V]. Then, regardless of power supply voltage,VEE+36[V] can be applied to input terminals without deterioration or destruction of its characteristics.

(4) Operating power supply (split power supply/single power supply)

The OP-Amp operates if a given level of voltage is applied between VCC and VEE. Therefore, the OP-Amp can be operated under single power supply or split power supply.

(5) Power dissipation(Pd)

In case of using the device beyond the rated Power Dissipation, the chip could be damaged exhibiting deteriorated characteristics such as reduced output current capability due to its chip surface temperature rising up. Therefore, please take Power Dissipation Derating into consideration and have enough margin in thermal design. Use below Power Dissipation Derating curve for reference.

(6) Short circuits between pins and incorrect mounting

Short circuits between pins and incorrect mounting when mounting the IC on a printed circuits board,take notice of the direction and positioning of the IC. If IC is mounted erroneously, It may be damaged. Also, when a foreign object is inserted between output, between output and VCC terminal or VEE terminal which causes short circuit, the IC may be damaged.

(7) Using under strong electromagnetic field

Be careful when using the IC under strong electromagnetic field because it may malfunction.

(8) Usage of IC

When stress is applied to the IC through warp of the printed circuit board. The characteristics may fluctuate due to the piezo effect. Be careful of the warp of the printed circuit board.

(9) Testing IC on the set board

When testing IC on the set board, in cases where the capacitor is connected to the low impedance,make sure to discharge per fabrication because there is a possibility that IC may be damaged by stress.When removing IC from the set board, it is essential to cut supply voltage.As a countermeasure against the static electricity, observe proper grounding during fabrication process and take due care when carrying and storage it.

(10) The IC destruction caused by capacitive load

The transistors in circuits may be damaged when VCC terminal and VEE terminal is shorted with the charged output terminal capacitor.

When IC is used as a comparator or as application circuits no constructed negative feed back, where oscillation is not activated by an output capacitor, the output capacitor must be kept below 0.1[μF] in order to prevent the damage mentioned above.

(11) The oscillation caused by capacitive load

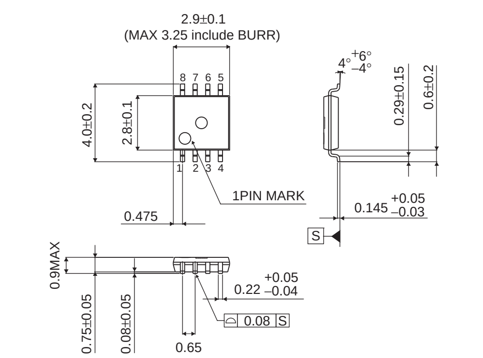
Designed negative feedback circuit using this IC, verify output oscillation caused by capacitive load.

●Ordering part number

B	A	3	4	7	2	Y	F	V	-	C	E	2

Part No.	Part No.	Package	Automotive series	Packaging and forming specification
	3472Y 3474Y	FV : SSOP-B8 SSOP-B14 FVM : MSOP8		E2: Embossed tape and reel (SSOP-B8/SSOP-B14) TR: Embossed tape and reel (MSOP8)

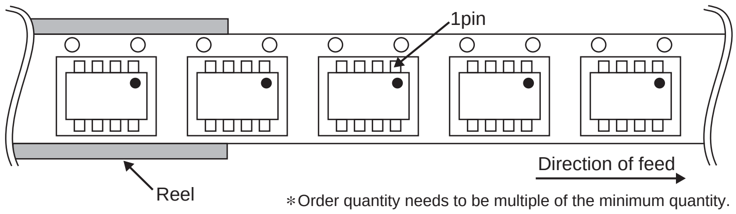
MSOP8



(Unit : mm)

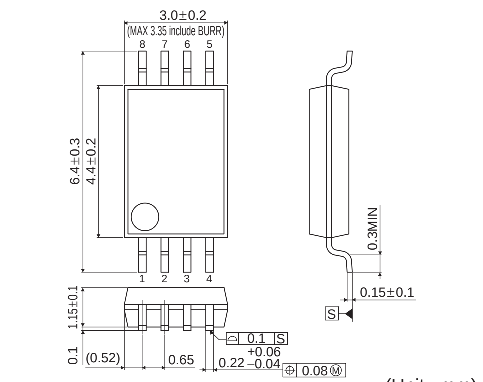
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

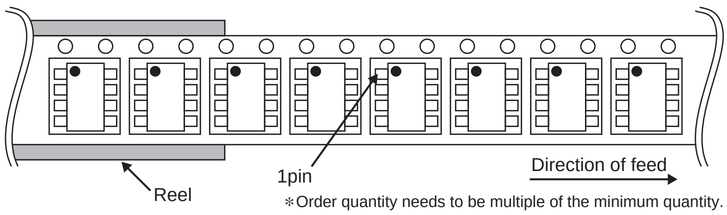
SSOP-B8



(Unit : mm)

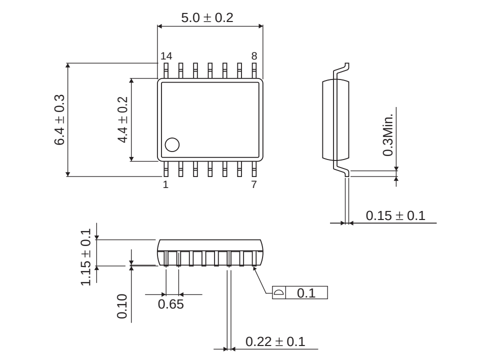
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

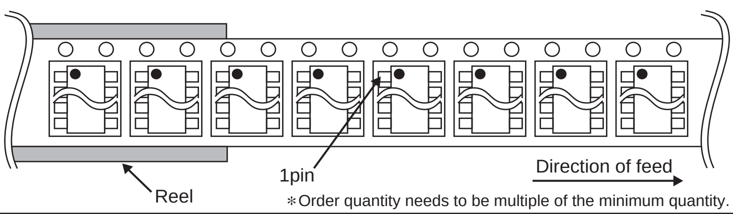
SSOP-B14



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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