

**Automotive Series Serial EEPROMs  
125°C SPI BUS ICs BR25xxxxFamily**



# BR25H320-2C

● **General Description**

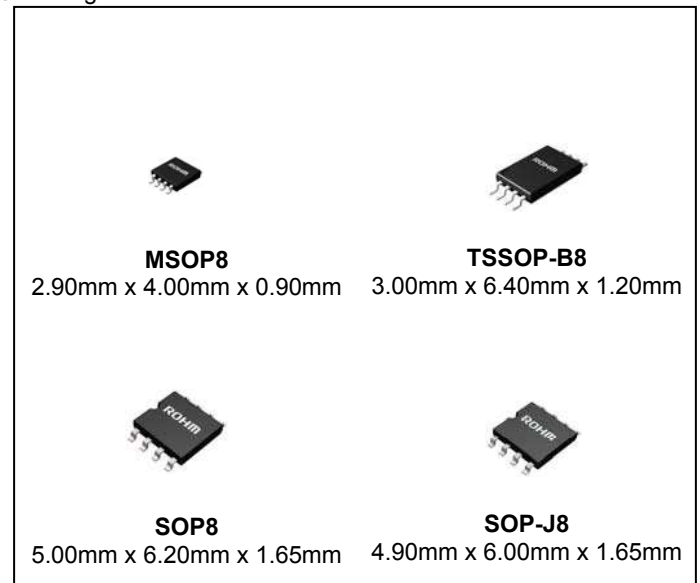
BR25H320-2C is a serial EEPROM of SPI BUS interface method.

● **Features**

- High speed clock action up to 10MHz (Max.)
- Wait function by HOLDB terminal.
- Part or whole of memory arrays settable as read only memory area by program.
- 2.5~5.5V single power source action most suitable for battery use.
- Page write mode useful for initial value write at factory shipment.
- For SPI bus interface (CPOL, CPHA)=(0, 0), (1, 1)
- Auto erase and auto end function at data rewrite.
- Low current consumption  
At write action (5V) : 1.5mA (Typ.)  
At read action (5V) : 1.0mA (Typ.)  
At standby action (5V) : 0.1μA (Typ.)
- Address auto increment function at read action
- Write mistake prevention function  
Write prohibition at power on.  
Write prohibition by command code (WRDI).  
Write prohibition by WPB pin.  
Write prohibition block setting by status registers (BP1, BP0).
- Write mistake prevention function at low voltage.

- MSOP8, TSSOP-B8, SOP8, SOP-J8 Package
- Data at shipment Memory array: FFh, status register WPEN, BP1, BP0 : 0
- Data kept for 20 years (Ta ≤ 125°C).
- Data rewrite up to 300,000 times (Ta ≤ 125°C).

● **Package**



● **Page write**

Number of pages	32 Byte
Product number	BR25H320-2C

● **BR25H320-2C**

Capacity	Bit format	Type	Power source voltage	MSOP8	TSSOP-B8	SOP8	SOP-J8
32Kbit	4Kx8	BR25H320-2C	2.5~5.5V	●	●	●	●

**● Absolute maximum ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit
Impressed voltage	VCC	-0.3~+6.5	V
Permissible dissipation	Pd	380(MSOP8) <sup>*1</sup>	mW
		410(TSSOP-B8) <sup>*2</sup>	
		560(SOP8) <sup>*3</sup>	
		560(SOP-J8) <sup>*4</sup>	
Storage temperature range	Tstg	-65~+150	°C
Operating temperature range	Topr	-40~+125	°C
Terminal voltage	—	-0.3~VCC+0.3	V

· When using at Ta=25°C or higher, 3.1mW(\*1), 3.3mW(\*2), 4.5mW (\*3,\*4) to be reduced per 1°C

**● Memory cell characteristics (VCC=2.5V~5.5V)**

Parameter	Limits			Unit	Condition
	Min.	Typ.	Max.		
Number of data rewrite times <sup>*5</sup>	1,000,000	—	—	Times	Ta ≤ 85°C
	500,000	—	—	Times	Ta ≤ 105°C
	300,000	—	—	Times	Ta ≤ 125°C
Data hold years <sup>*5</sup>	40	—	—	Years	Ta ≤ 25°C
	25	—	—	Years	Ta ≤ 105°C
	20	—	—	Years	Ta ≤ 125°C

\*5: Not 100% TESTED

**● Recommended Operating Ratings**

Parameter	Symbol	Limits	Unit
Power source voltage	VCC	2.5~5.5	V
Input voltage	Vin	0~VCC	

**● Input / output capacity (Ta=25°C, frequency=5MHz)**

Parameter	Symbol	Conditions	Min	Max	Unit
Input capacity <sup>*6</sup>	C <sub>IN</sub>	V <sub>IN</sub> =GND	—	8	pF
Output capacity <sup>*6</sup>	C <sub>OUT</sub>	V <sub>OUT</sub> =GND	—	8	

\*6: Not 100% TESTED

●Electrical characteristics (Unless otherwise specified, Ta=-40~+125°C, VCC=2.5~5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
"H" input voltage	VIH	0.7xVCC	—	VCC +0.3	V	2.5 ≤ VCC ≤ 5.5V
"L" input voltage	VIL	-0.3	—	0.3x VCC	V	2.5 ≤ VCC ≤ 5.5V
"L" output voltage	VOL	0	—	0.4	V	IOL=2.1mA
"H" output voltage	VOH	VCC-0.5	—	VCC	V	IOH=-0.4mA
Input leak current	ILI	-2	—	2	μA	VIN=0~VCC
Output leak current	ILO	-2	—	2	μA	VOUT=0~VCC, CSB=VCC
Current consumption at write action	ICC1	—	—	2.0	mA	VCC=2.5V, fSCK=5MHz, tE/W=4ms VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Byte write, Page write, Write status register
	ICC2	—	—	3.0	mA	VCC=5.5V, fSCK=5 or 10 MHz, tE/W=4ms VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Byte write, Page write, Write status register
Current consumption at read action	ICC3	—	—	1.5	mA	VCC=2.5V, fSCK=5MHz VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Read, Read status register
	ICC4	—	—	2.0	mA	VCC=5.5V, fSCK=5MHz VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Read, Read status register
	ICC5	—	—	4.0	mA	VCC=5.5V, fSCK=10MHz VIH/VIL=0.9VCC/0.1VCC, SO=OPEN Read, Read status register
Standby current	ISB	—	—	10	μA	VCC=5.5V CSB=HOLDB=WPB=VCC, SCK=SI=VCC or =GND, SO=OPEN

\*Radiation resistance design is not made

**● Operating timing characteristics** (Ta=-40~+125°C, unless otherwise specified, load capacity CL1=100pF)

Parameter	Symbol	2.5 ≤ VCC ≤ 5.5V			4.5 ≤ VCC ≤ 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCK frequency	fCSK	—	—	5	—	—	10	MHz
SCK high time	tSCKWH	85	—	—	40	—	—	ns
SCK low time	tSCKWL	85	—	—	40	—	—	ns
CSB high time	tCS	85	—	—	40	—	—	ns
CSB setup time	tCSS	90	—	—	30	—	—	ns
CSB hold time	tCSH	85	—	—	30	—	—	ns
SCK setup time	tSCKS	90	—	—	30	—	—	ns
SCK hold time	tSCKH	90	—	—	30	—	—	ns
SI setup time	tDIS	20	—	—	10	—	—	ns
SI hold time	tDIH	30	—	—	10	—	—	ns
Data output delay time1	tPD1	—	—	60	—	—	40	ns
Data output delay time2 (CL2=30pF)	tPD2	—	—	50	—	—	30	ns
Output hold time	tOH	0	—	—	0	—	—	ns
Output disable time	tOZ	—	—	100	—	—	40	ns
HOLDB setting setup time	tHFS	0	—	—	0	—	—	ns
HOLDB setting hold time	tHFH	40	—	—	30	—	—	ns
HOLDB release setup time	tHRS	0	—	—	0	—	—	ns
HOLDB release hold time	tHRH	70	—	—	30	—	—	ns
Time from HOLDB to output High-Z	tHOZ	—	—	100	—	—	40	ns
Time from HOLDB To output change	tHPD	—	—	60	—	—	40	ns
SCK rise time <sup>*1</sup>	tRC	—	—	1	—	—	1	μs
SCK fall time <sup>*1</sup>	tFC	—	—	1	—	—	1	μs
OUTPUT rise time <sup>*1</sup>	tRO	—	—	40	—	—	40	ns
OUTPUT fall time <sup>*1</sup>	tFO	—	—	40	—	—	40	ns
Write time	tE/W	—	—	4	—	—	4	ms

\*1 NOT 100% TESTED

**● AC measurement conditions**

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Load capacity 1	CL1	—	—	100	pF
Load capacity 2	CL2	—	—	30	pF
Input rise time	—	—	—	50	ns
Input fall time	—	—	—	50	ns
Input voltage	—	0.2VCC/0.8VCC			V
Input / Output judgement voltage	—	0.3VCC/0.7VCC			V

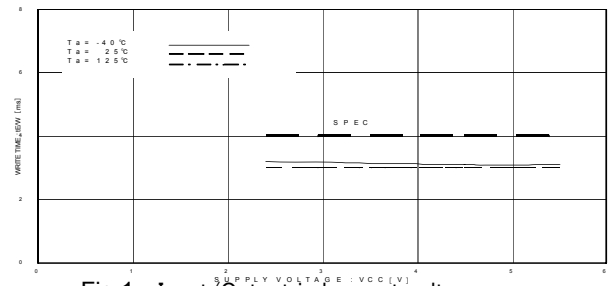


Fig.1 Input/Output judgement voltage

● Sync data input / output timing

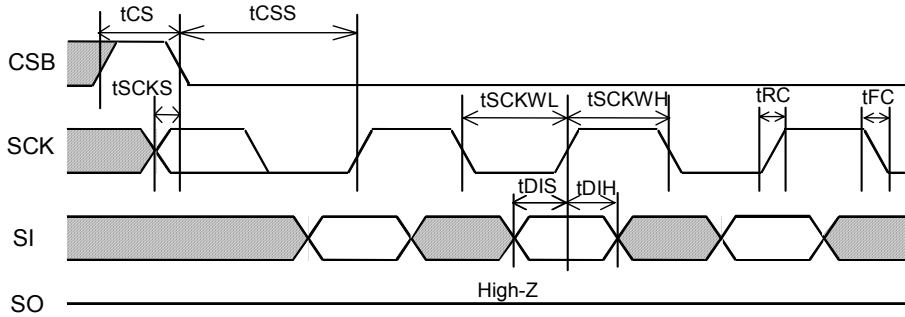


Fig.2 Input timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB.

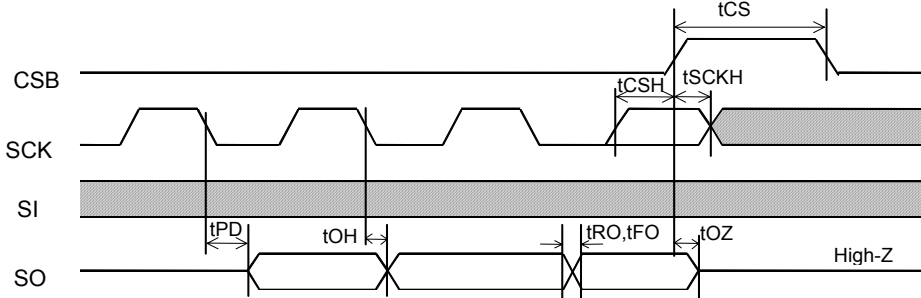


Fig.3 Input / Output timing

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

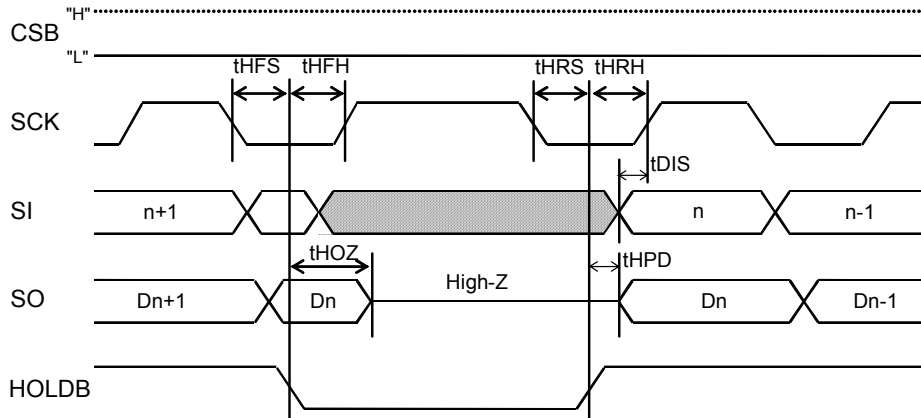


Fig.4 HOLD timing

● Block diagram

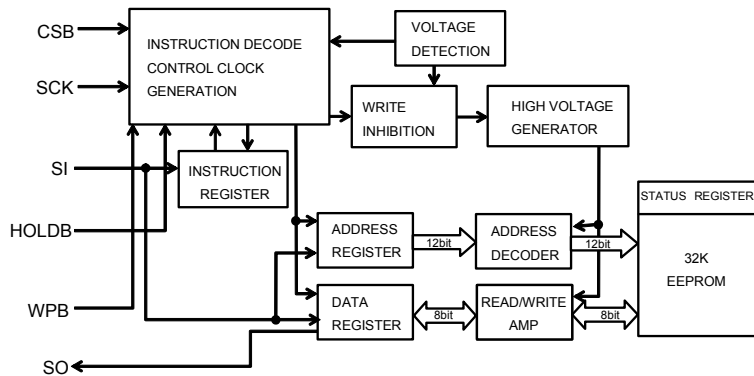


Fig.5 Block diagram

### ● Pin Configuration

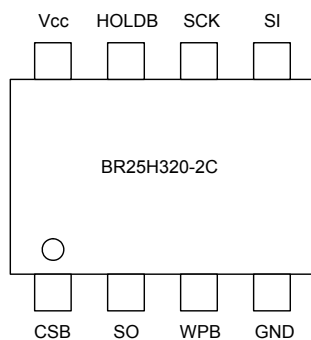


Fig.6 Pin assignment diagram

### ● Pin Descriptions

Terminal number	Terminal name	Input /Output	Function
1	CSB	Input	Chip select input
2	SO	Output	Serial data output
3	WPB	Input	Write protect input Write status register command is prohibited.
4	GND	—	All input / output reference voltage, 0V
5	SI	Input	Start bit, ope code, address, and serial data input
6	SCK	Input	Serial clock input
7	HOLDB	Input	Hold input Command communications may be suspended temporarily (HOLD status)
8	VCC	—	Power source to be connected

● Typical Performance Curves

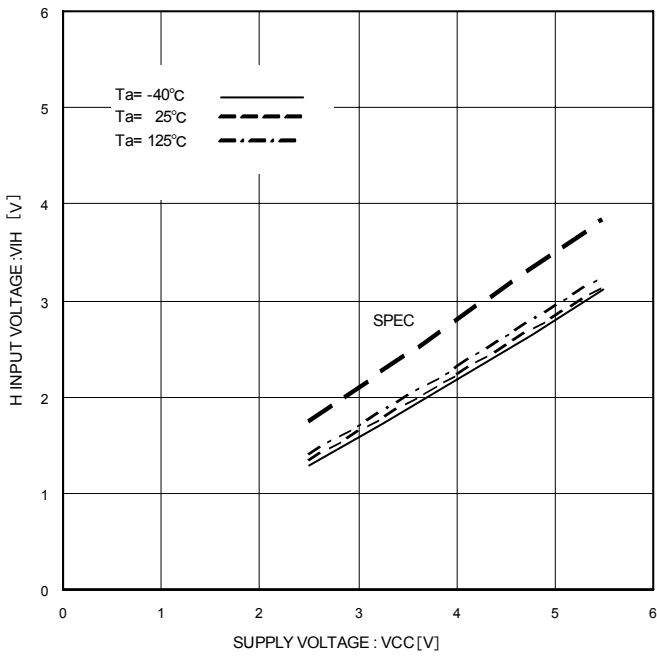


Fig.7 "H" input voltage VIH (CSB,SCK,SI,HOLDB,WPB)

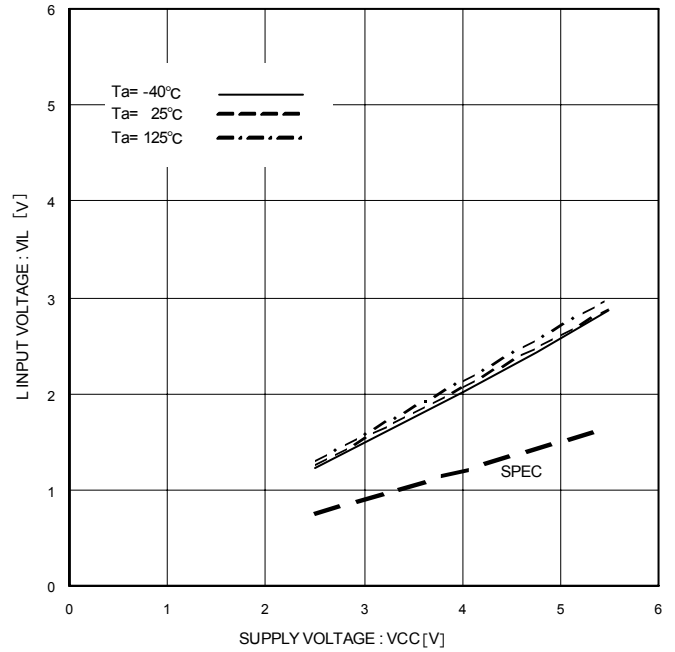


Fig.8 "L" input voltage VIL(CSB,SCK,SI,HOLDB,WPB)

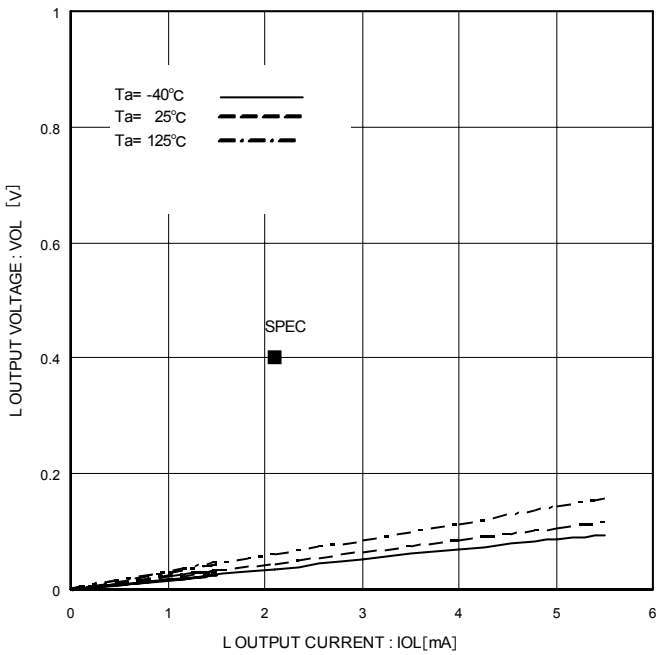


Fig.9 "L" output voltage VOL, IOL (Vcc=2.5V)

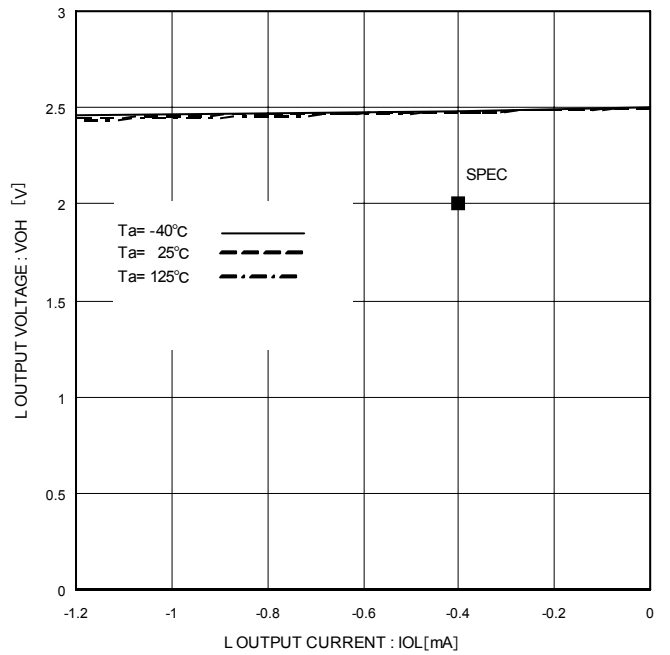


Fig.10 "H" output voltage VOH, IOH (Vcc=2.5V)

● Typical Performance Curves - Continued

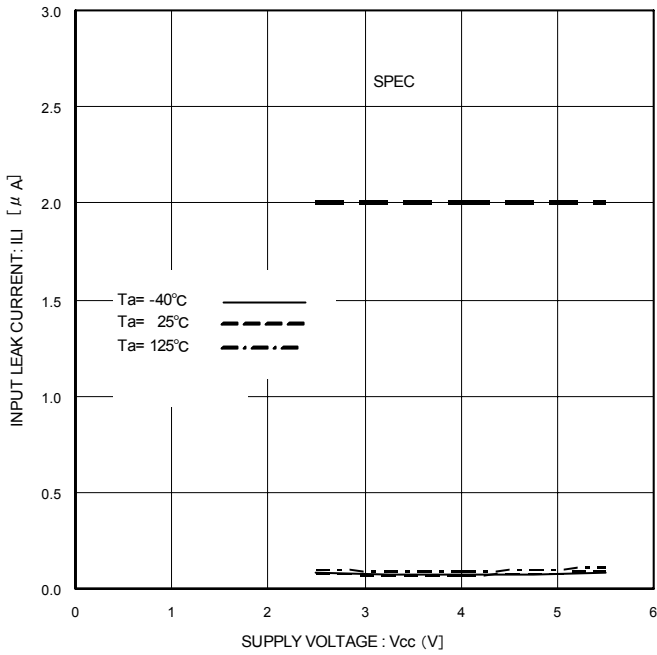


Fig.11 Input leak current ILI(CSB,SCK,SI,HOLDB,WPB)

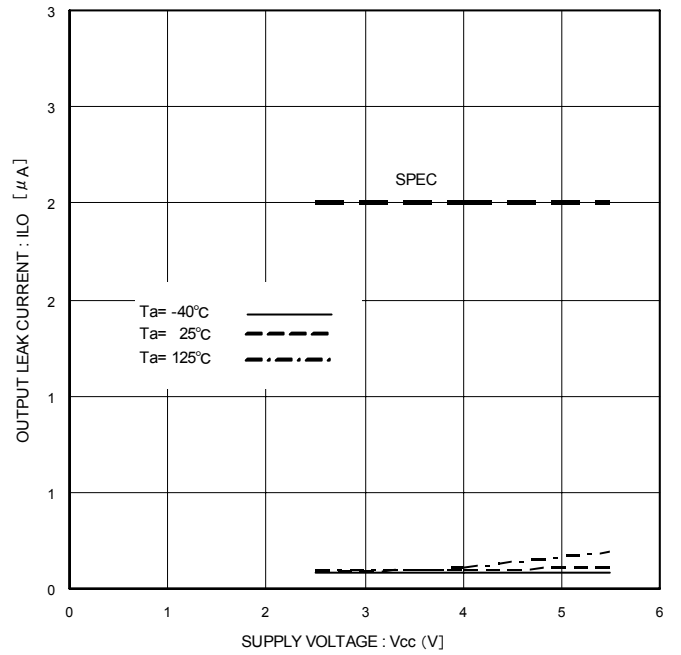


Fig.12 Output leak current ILO(SO)(Vcc=5.5V)

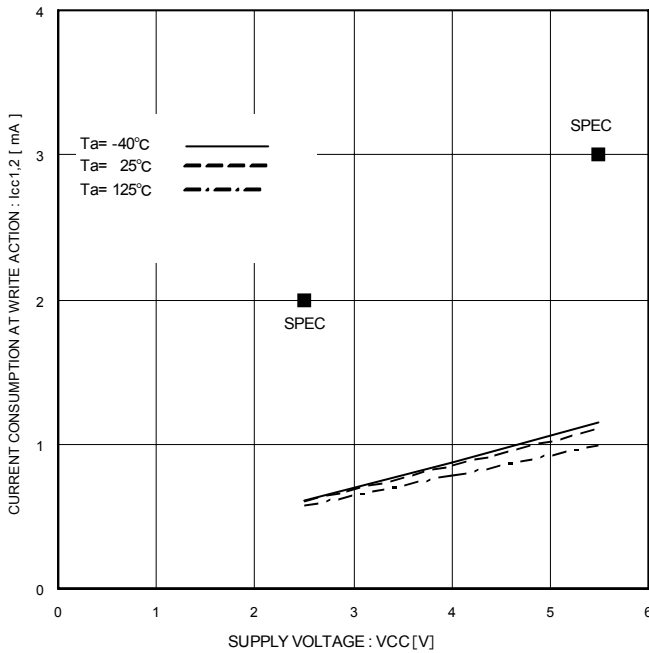


Fig.13 Operating Current (WRITE) ICC1,2

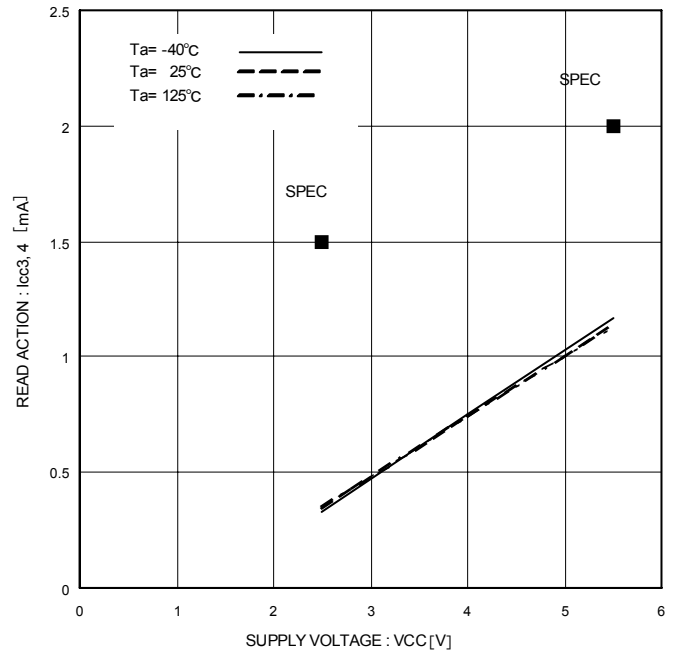


Fig.14 Operating Current (READ) ICC3,4

● Typical Performance Curves - Continued

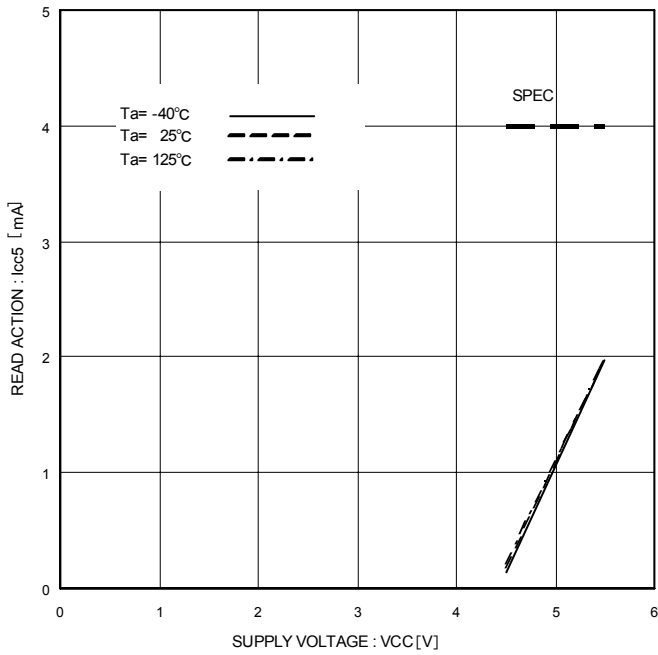


Fig.15 Operating Current (READ) ICC5

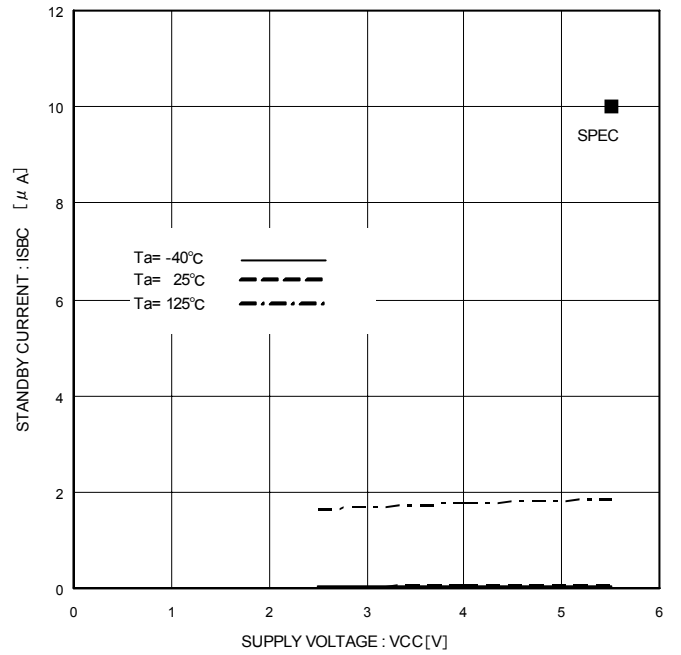


Fig.16 Standby Current ISB

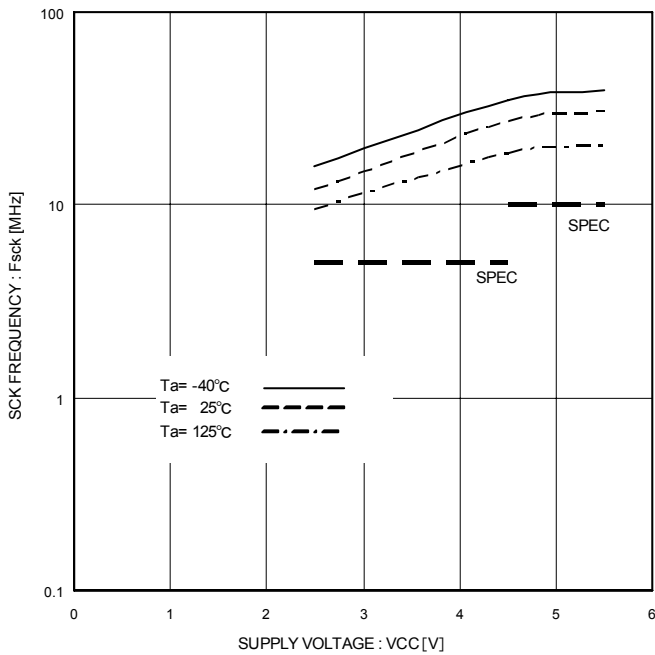


Fig.17 SCK frequency fSCK

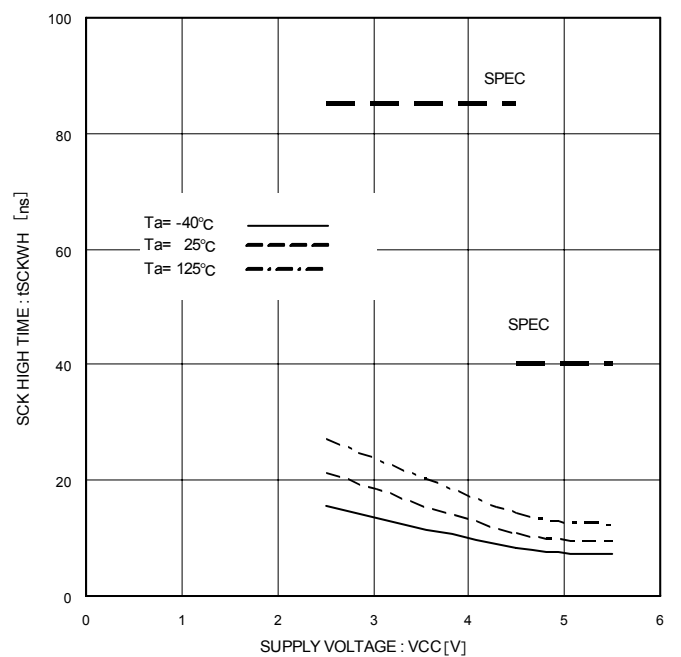


Fig.18 SCK high time tSCKWH

● Typical Performance Curves - Continued

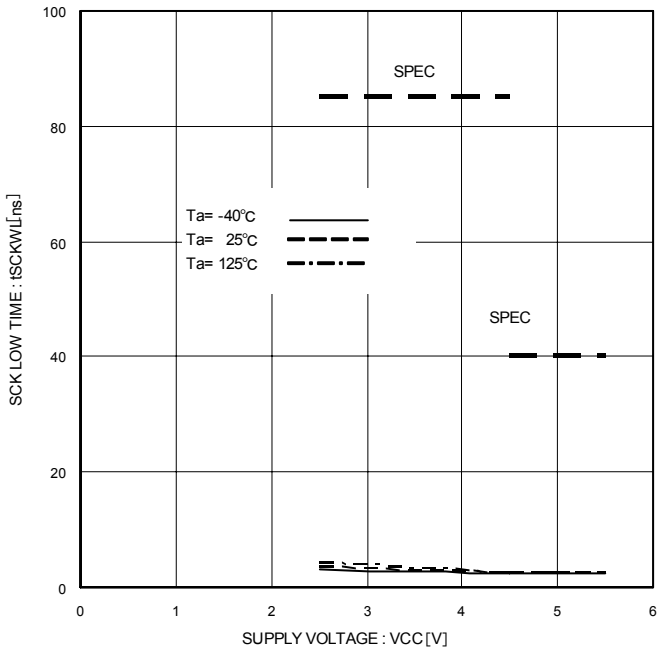


Fig.19 SCK low time t<sub>SCKWL</sub>

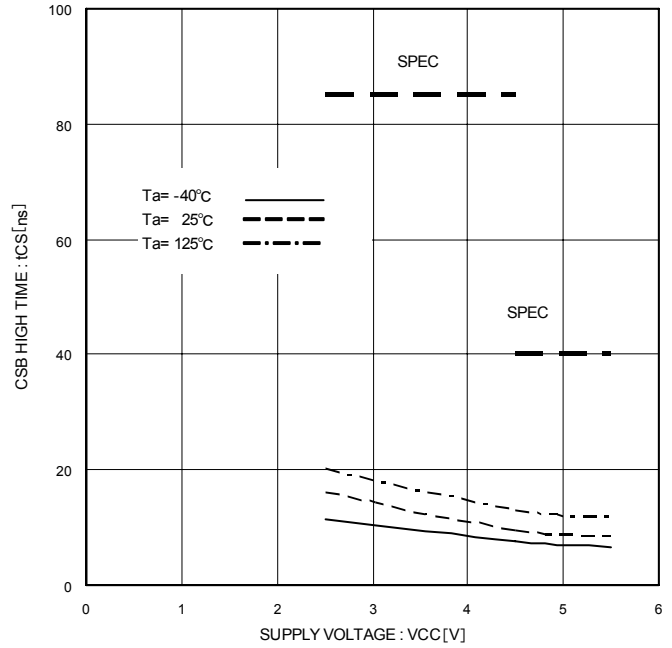


Fig.20 CSB high time t<sub>CS</sub>

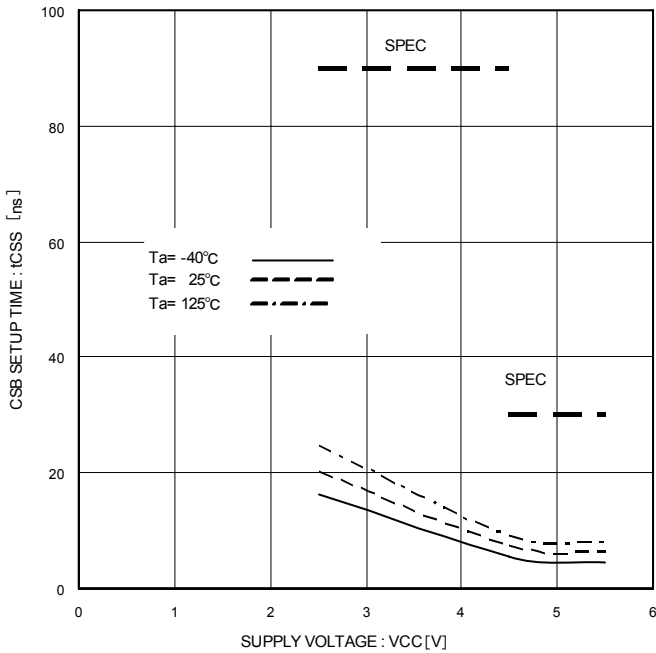


Fig.21 CSB setup time t<sub>CS</sub><sub>SS</sub>

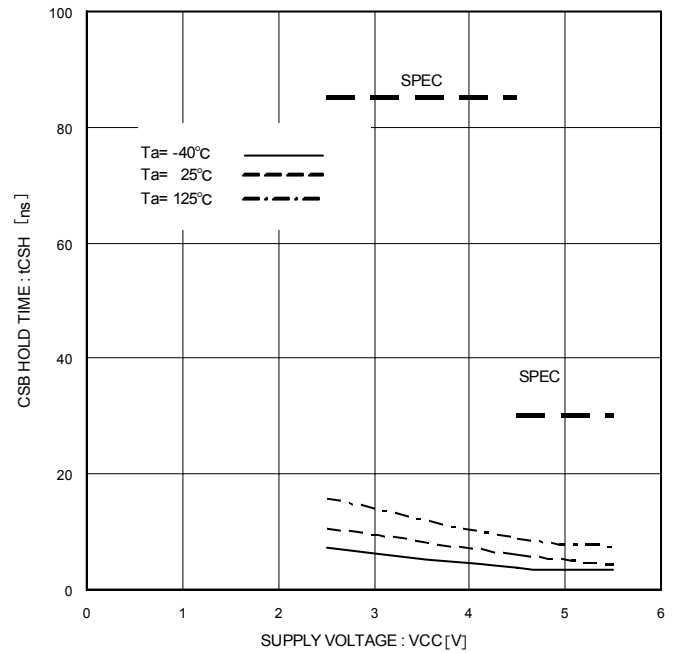


Fig.22 CSB hold time t<sub>CS</sub><sub>H</sub>

● Typical Performance Curves - Continued

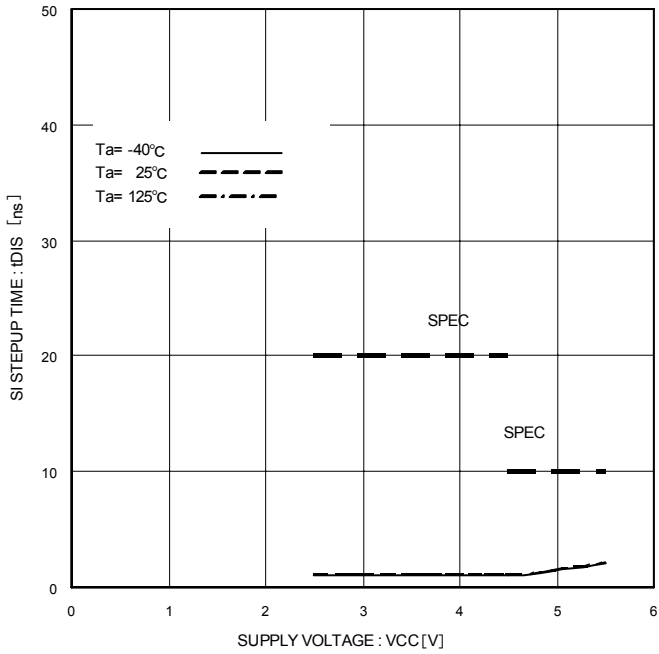


Fig.23 SI setup time  $t_{DIS}$

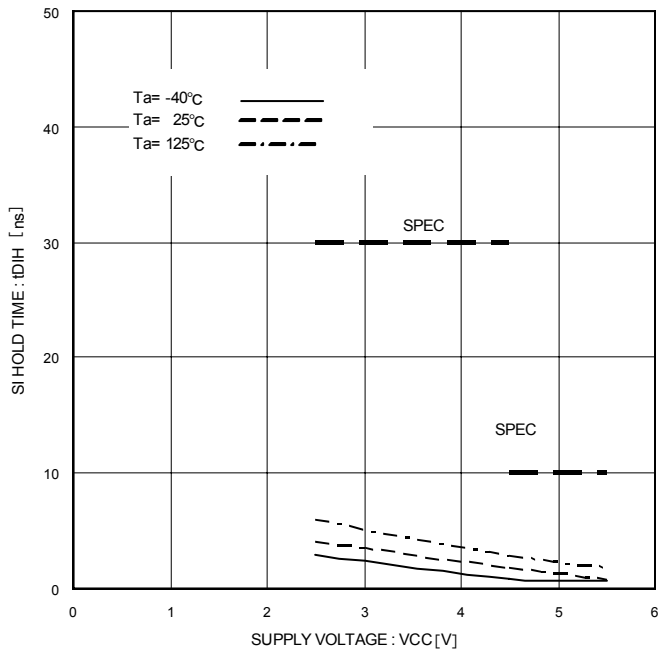


Fig.24 SI hold time  $t_{DIH}$

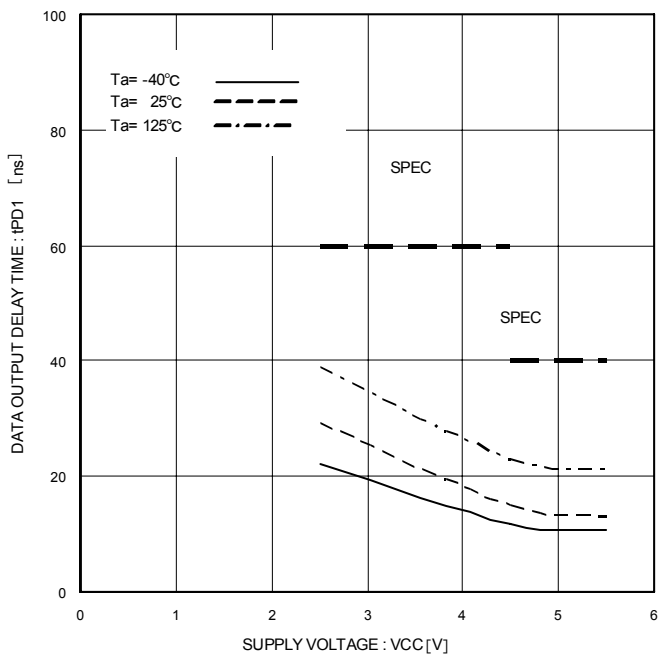


Fig.25 Data output delay time  $t_{PD1}$  (CL=100pF)

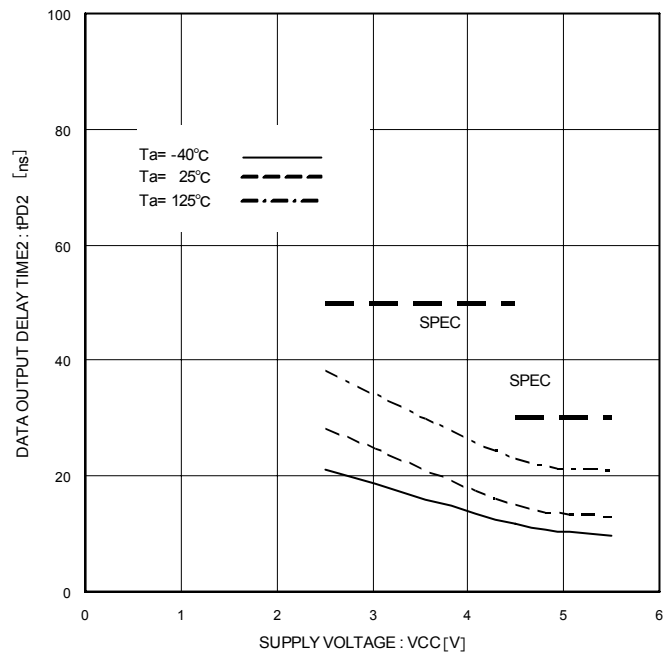


Fig.26 Data output delay time  $t_{PD2}$  (CL=30pF)

● Typical Performance Curves - Continued

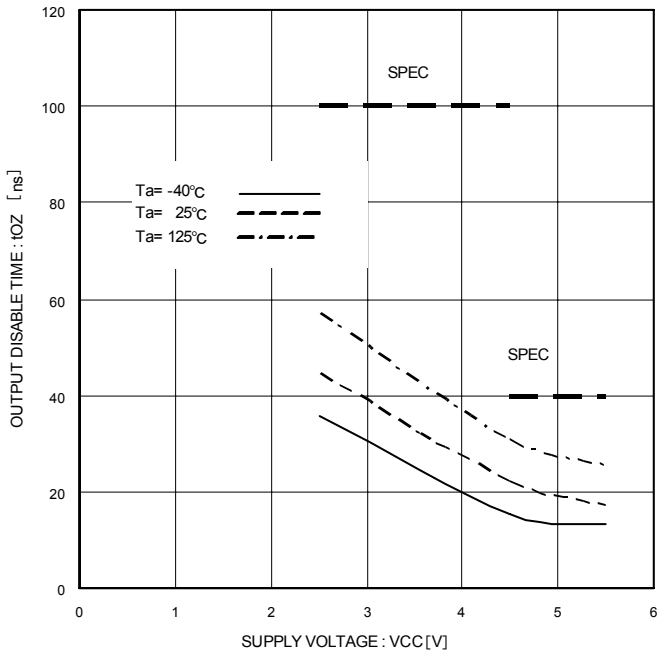


Fig.27 Output disable time tOZ

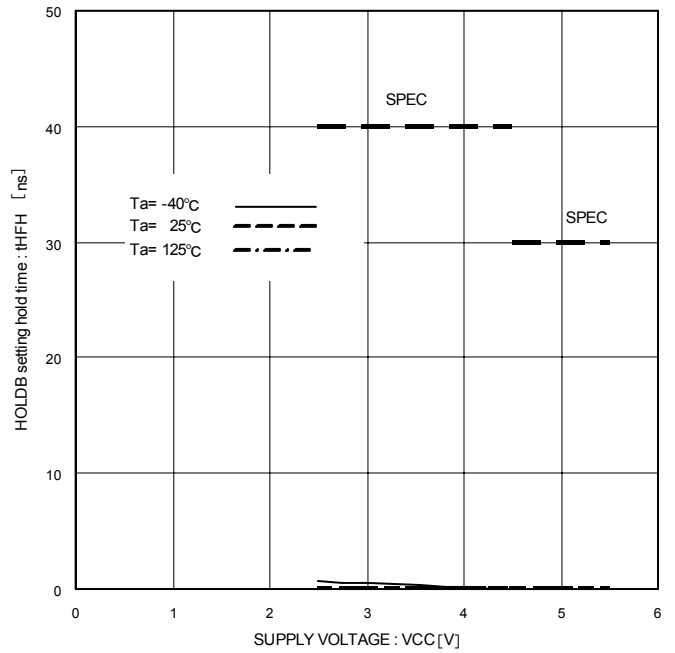


Fig.28 HOLDB setting hold time tHFH

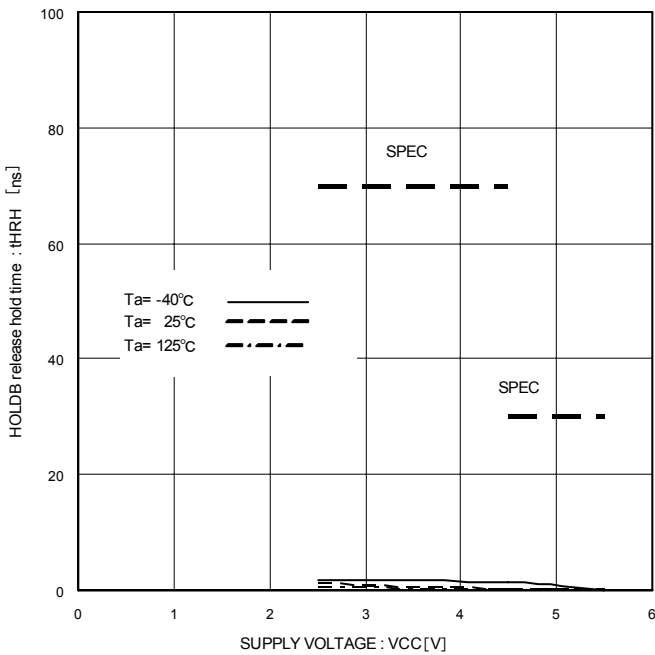


Fig.29 HOLDB release hold time tHRH

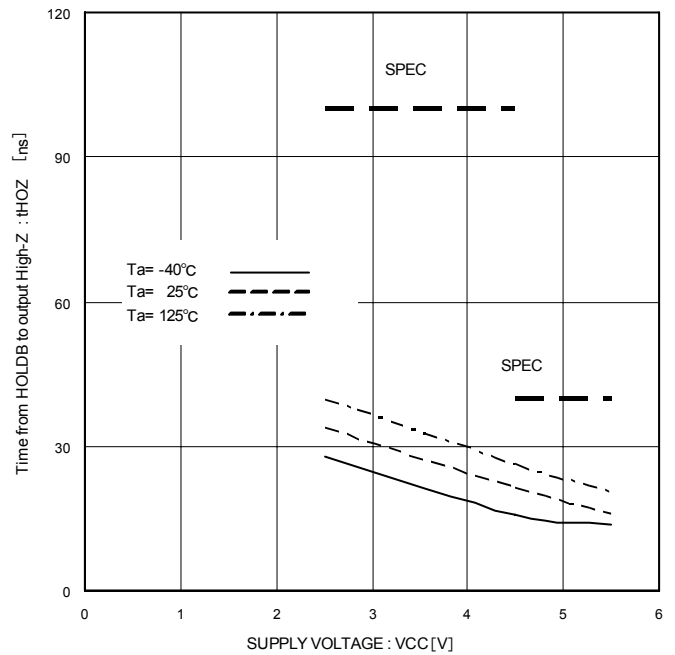


Fig.30 Time from HOLDB to output High-Z tHOZ

● Typical Performance Curves - Continued

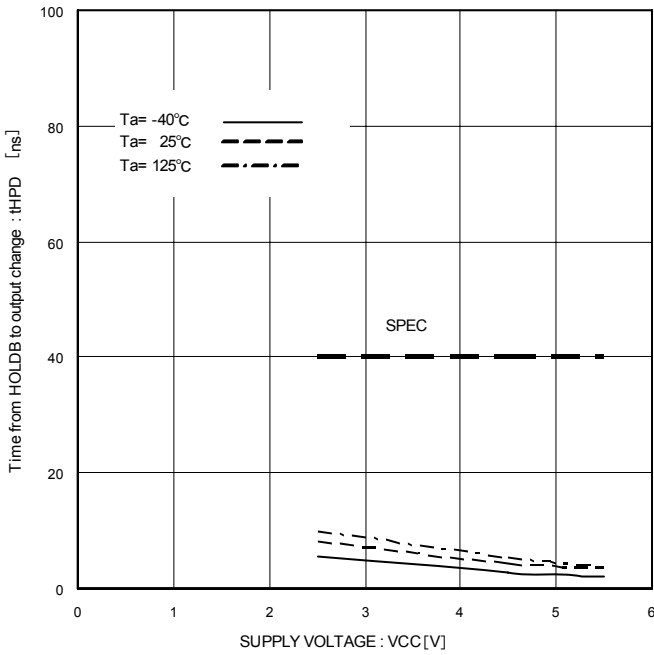


Fig.31 Time from HOLDDB to output change tHPD

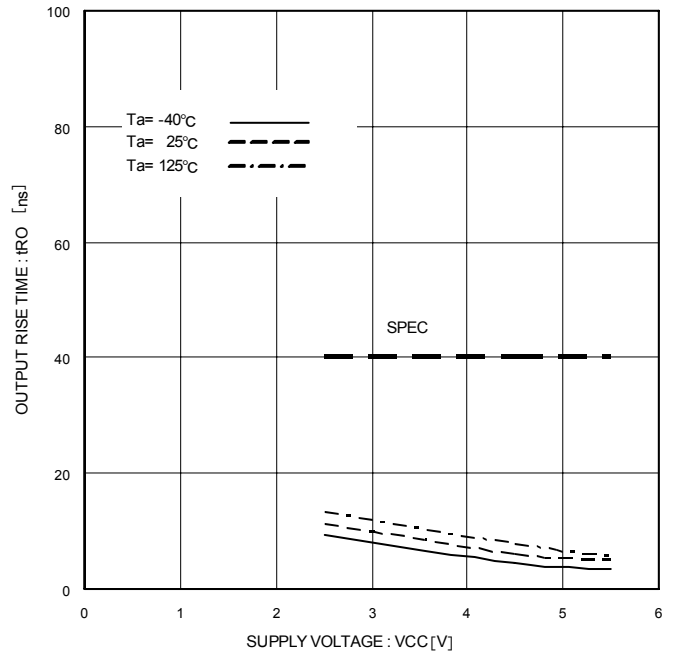


Fig.32 Output rise time tRO

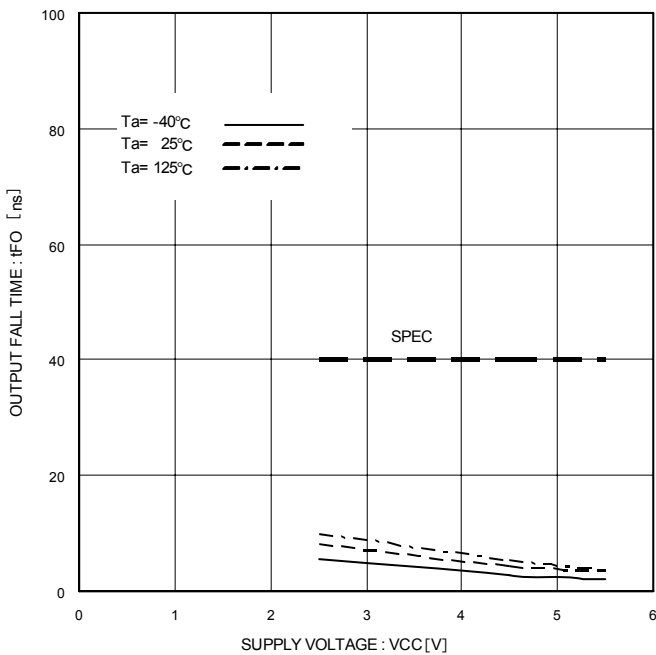


Fig.33 Output fall time tFO

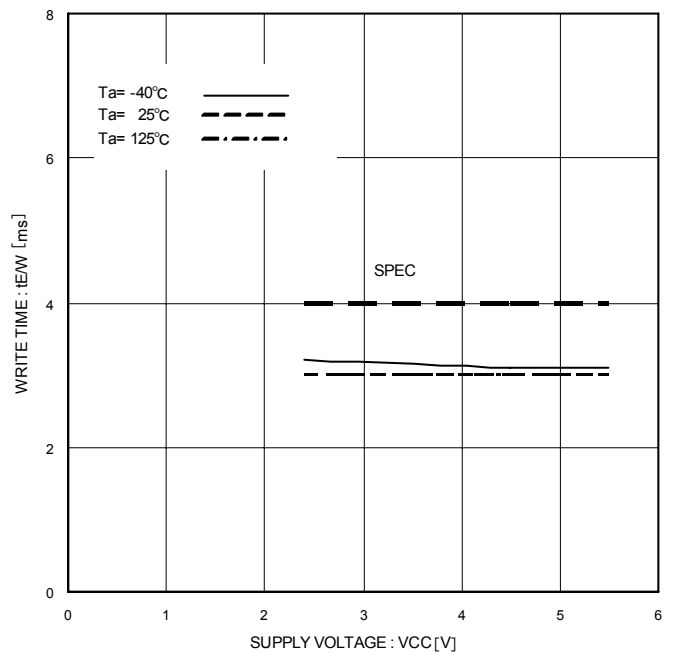


Fig.34 Write cycle time tE/W

## ●Features

### ○Status registers

This IC has status registers. The status registers are of 8 bits and express the following parameters.

BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.

Number of data rewrite times and data hold time are same as characteristics of the EEPROM.

WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off.  $\overline{R/B}$  is for write confirmation, therefore cannot be set externally.

The value of status register can be read by read status command.

## ●Status registers

Product number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR25H320-2C	WPEN	0	0	0	BP1	BP0	WEN	$\overline{R/B}$

bit	Memory location	Function	Contents
WPEN	EEPROM	WPB pin enable / disable designation bit WPEN=0=invalid , WPEN=1=valid	This enables / disables the functions of WPB pin.
BP1 BP0	EEPROM	EEPROM write disable block designation bit	This designates the write disable area of EEPROM. Write designation areas of product numbers are shown below.
WEN	Register	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited , WEN=1=permitted	This confirms prohibited status or permitted status of the write and the write status register.
$\overline{R/B}$	Register	Write cycle status (READY / BUSY) confirmation bit R/B=0=READY , R/B=1=BUSY	This confirms READY status or BUSY status of the write cycle.

## ●Write disable block setting

BP1	BP0	BR25H320-2C
0	0	None
0	1	C00h-FFFh
1	0	800h-FFFh
1	1	000h-FFFh

**OWPB pin**

By setting WPB=LOW, write command is prohibited. As for BR25H320-2C, only when WPEN bit is set "1", the WPB pin functions become valid. And the write command to be disabled at this moment is WRSR. However, when write cycle is in execution, no interruption can be made.

Product number	WRSR	WRITE
BR25H320-2C	Prohibition possible but WPEN bit "1"	Prohibition impossible

**OHOLDB pin**

By HOLDB pin, data transfer can be interrupted. When SCK="0", by making HOLDB from "1" into "0", data transfer to EEPROM is interrupted. When SCK = "0", by making HOLDB from "0" into "1", data transfer is restarted.

**●Command mode**

Command		Contents	Ope codes	
WREN	Write enable	Write enable command	0000	0110
WRDI	Write disable	Write disable command	0000	0100
READ	Read	Read command	0000	0011
WRITE	Write	Write command	0000	0010
RDSR	Read status register	Status register read command	0000	0101
WRSR	Write status register	Status register write command	0000	0001

●Timing chart

1. Write enable (WREN) / disable (WRDI) cycle

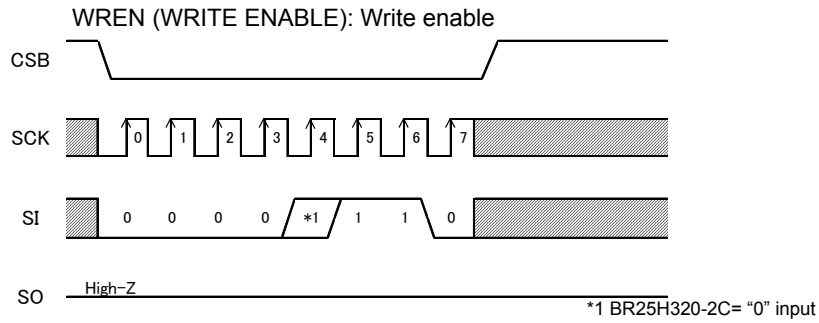


Fig.35 Write enable command

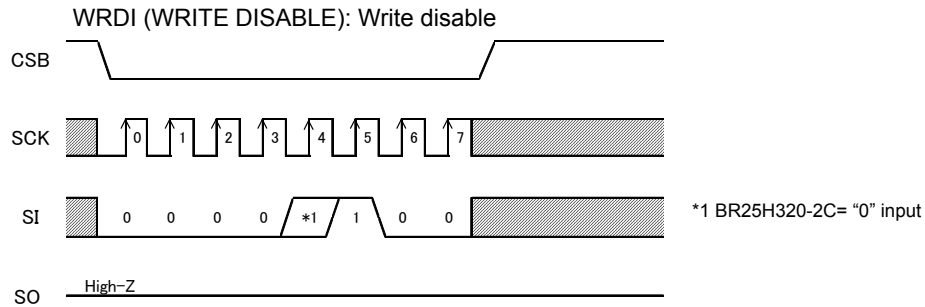
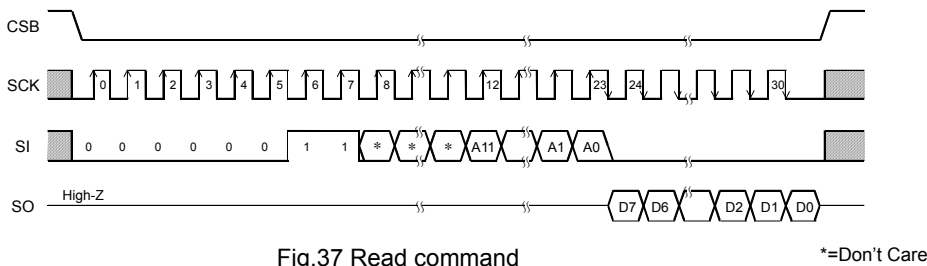


Fig.36 Write disable

○This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CSB LOW, and then input the respective ope codes. The respective commands accept command at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.

When to carry out write and write status register command, it is necessary to set write enable status by the write enable command. If write or write status register command is input in the write disable status, commands are cancelled. And even in the write enable status, once write and write status register command is executed. It gets in the write disable status. After power on, this IC is in write disable status.

2. Read command (READ)



Product number	Address length
BR25H320-2C	A11-A0

By read command, data of EEPROM can be read. As for this command, set CSB LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

3. Write command (WRITE)

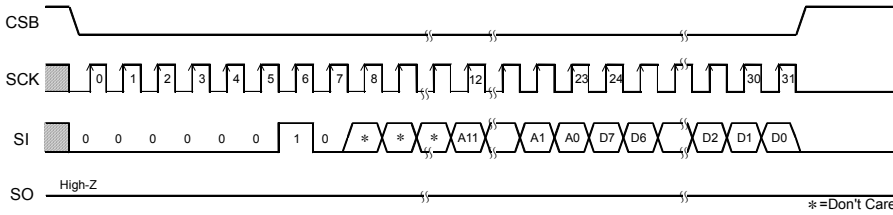


Fig.38 Write command

Product number	Address length
BR25H320-2C	A11-A0

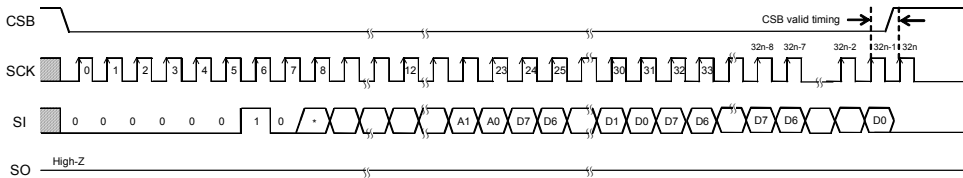
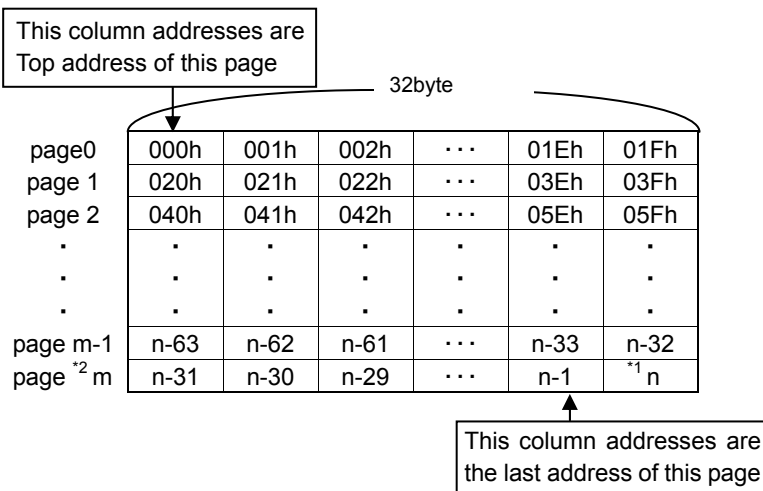


Fig.39 N Byte page write command

By write command, data of EEPROM can be written. As for this command, set CSB LOW, then input address and data after write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of  $t_{E/W}$  (Max 4ms). During  $t_{E/W}$ , other than status read command is not accepted. Start CSB after taking the last data (D0), and before the next SCK clock starts. At other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without starting CSB, data up to 32 bytes can be written for one  $t_{E/W}$ . In page write, the insignificant 5 bit of the designated address is incremented internally at every time when data of 1 byte is input and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

Write command is executed when CSB rises between the SCK clock rising edge to recognize the 8th bits of data input and the next SCK rising edge. At other timings the write command is not executed and cancelled (Fig.48 valid timing c). In page write, the CSB valid timing is every 8 bits. If CSB rises at other timings page write is cancelled together with the write command and the input data is reset.



\*1 n=4095d=FFFh : BR25H320-2C  
 \*2 m=127 : BR25H320-2C

Fig.40 EEPROM physical address for Page write command (32Byte)

## ●Example of Page write command

No.	Addresses of Page0	000h	001h	002h	....	01Eh	01Fh
①	Previous data	00h	01h	02h	....	1Eh	1Fh
②	2 bytes input data	AAh	55h	-	....	-	-
③	After No.②	AAh	55h	02h	....	1Eh	1Fh
④	34 byte input data	AAh	55h	AAh	....	AAh	55h
		FFh	00h	-	....	-	-
⑤	After No.④	FFh	00h	AAh	....	AAh	55h

a : In case of input the data of No.② which is 2 bytes page write command for the data of No.①, EEPROM data changes like No.③.

b : In case of input the data of No.④ which is 34 bytes page write command for the data of No.①, EEPROM data changes like No.⑤.

c : In case of a or b, when write command is cancelled, EEPROM data keep No.①.

In page write command, when data is set to the last address of a page (e.g. address "03Fh" of page 1), the next data will be set to the top address of the same page (e.g. address "020h" of page 1). This is why page write address increment is available in the same page. As a reference, if of 32 bytes, page write command is executed for 2 bytes the data of the other 30 bytes without addresses will not be changed.

## 4. Status register write / read command

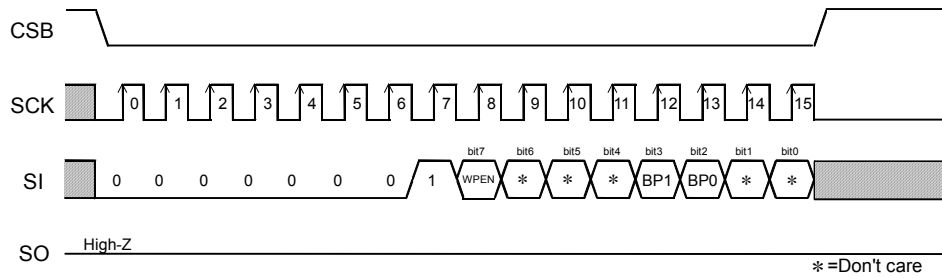


Fig.41 Status register write command

Write status register command can write status register data. The data can be written by this command are 2 bits, that is, WPEN (bit7), BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set CSB LOW, and input ope code of write status register, and input data. Then, by making CSB HIGH, EEPROM starts writing. Write time requires time of  $t_{E/W}$  as same as write. As for CSB rise, start CSB after taking the last data bit (bit0), and before the next SCK clock starts. At other timing, command is cancelled. Write disable block is determined by BP1 and BP0, and the block can be selected from 1/4 of memory array, 1/2, and entire memory array. (Refer to the write disable block setting table.)

To the write disabled block, write cannot be made, and only read can be made.

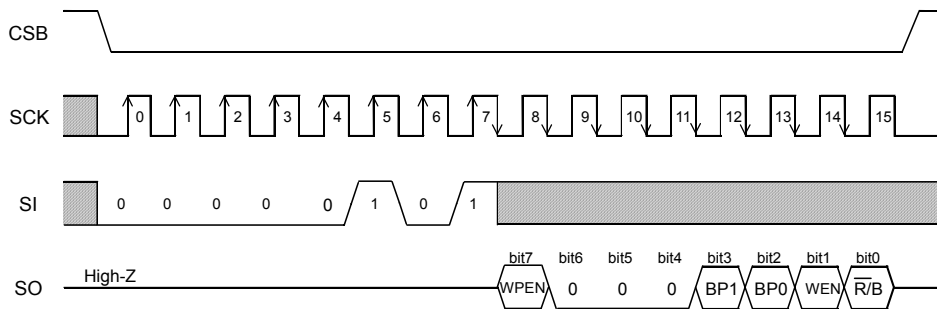


Fig.42 Status register read command

### ●At standby

#### ○Current at standby

Set CSB "H", and be sure to set SCK, SI, WPB, HOLDB input "L" or "H". Do not input intermediate electric potential.

#### ○Timing

As shown in Fig.43, at standby, when SCK is "H", even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB "H" status.

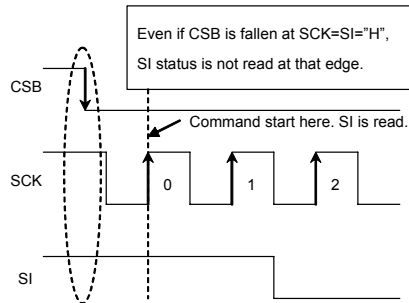


Fig.43 Operating timing

### ●WPB cancel valid area

WPB is normally fixed to "H" or "L" for use, but when WPB is controlled so as to cancel write status register command and write command, pay attention to the following WPB valid timing.

While write or write status register command is executed, by setting WPB = "L" in cancel valid area, command can be cancelled. The areas from command ope code before CSB rise at internal automatic write start becomes the cancel valid area. However, once write is started, any input cannot be cancelled. WPB input becomes Don't Care, and cancellation becomes invalid.

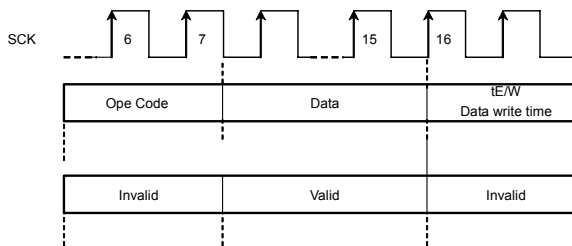


Fig.44 WPB valid timing (WRSR)

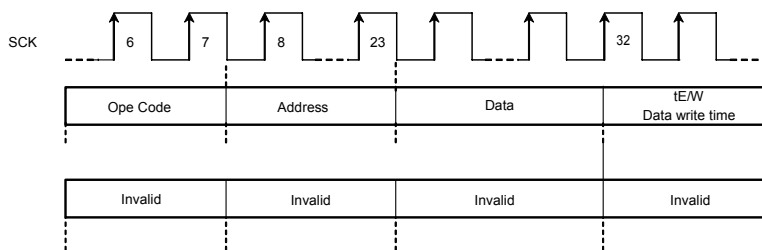


Fig.45 WPB valid timing (WRITE)

### ●HOLDB pin

By HOLDB pin, command communication can be stopped temporarily (HOLD status). The HOLDB pin carries out command communications normally when it is HIGH. To get in HOLD status, at command communication, when SCK=LOW, set the HOLDB pin LOW. At HOLD status, SCK and SI become Don't Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin HIGH when SCK=LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, leave CSB LOW. When it is set CSB=HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

●Method to cancel each command

○READ

- Method to cancel : cancel by CSB = "H"

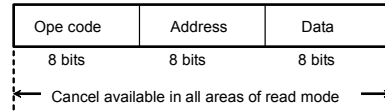


Fig.46 READ cancel valid timing

○RDSR

- Method to cancel : cancel by CSB = "H"

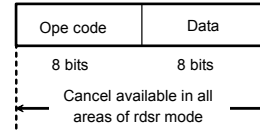


Fig.47 RDSR cancel valid timing

○WRITE, PAGE WRITE

- a : Ope code, address input area.  
Cancellation is available by CSB="H"
- b : Data input area (D7~D1 input area)  
Cancellation is available by CSB="H"
- c : Data input area (D0 area)  
When CSB is started, write starts.  
After CSB rise, cancellation cannot be made by any means.
- d : tE/W area.  
Cancellation is available by CSB = "H". However, when write starts (CSB is started) in the area c, cancellation cannot be made by any means. And by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

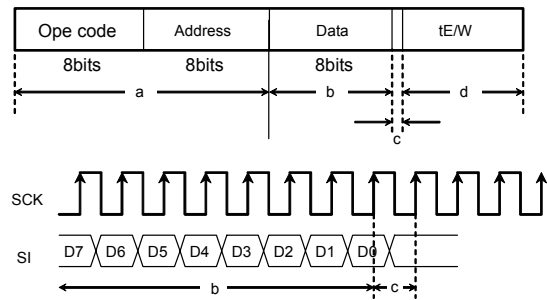


Fig.48 WRITE cancel valid timing

- Note 1) If VCC is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
- Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = "L" area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○WRSR

- a : From ope code to 15 rise.  
Cancel by CSB = "H".
- b : From 15 clock rise to 16 clock rise (write enable area).  
When CSB is started, write starts.  
After CSB rise, cancellation cannot be made by any means.
- c : After 16 clock rise.  
Cancel by CSB="H". However, when write starts (CSB is started) in the area b, cancellation cannot be made by any means.  
And, by inputting on SCK clock, cancellation cannot be made.

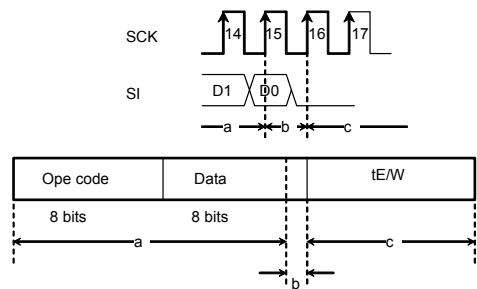


Fig.49 WRSR cancel valid timing

- Note 1) If VCC is made OFF during write execution, designated address data is not guaranteed, therefore write it once again
- Note 2) If CSB is started at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to fall in SCK = "L" area. As for SCK rise, assure timing of tCSS / tCSH or higher.

○WREN/WRDI

- a : From ope code to 7-th clock rise, cancel by CSB = "H".
- b : Cancellation is not available when CSB is started after 7-th clock.

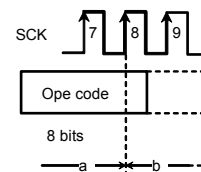


Fig.50 WREN/WRDI cancel valid timing

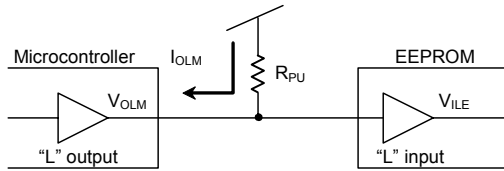
### ●High speed operation

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

#### ○Input terminal pull up, pull down resistance

When to attach pull up, pull down resistance to EEPROM input terminal, select an appropriate value for the microcontroller VOL, IOL from VIL characteristics of this IC.

#### ○Pull up resistance



- $V_{ILE}$  :EEPROM  $V_{IL}$  specifications
- $V_{OLM}$  :Microcontroller  $V_{OL}$  specifications
- $I_{OLM}$  :Microcontroller  $I_{OL}$  specifications

Fig.51 Pull up resistance

$$R_{PU} \geq \frac{V_{CC} - V_{OLM}}{I_{OLM}} \quad \dots \textcircled{1}$$

$$V_{OLM} \leq V_{ILE} \quad \dots \textcircled{2}$$

Example) When  $V_{CC}=5V$ ,  $V_{ILE}=1.5V$ ,  $V_{OLM}=0.4V$ ,  $I_{OLM}=2mA$ , from the equation ①,

$$R_{PU} \geq \frac{5-0.4}{2 \times 10^{-3}}$$

$$\therefore R_{PU} \leq 2.3[k\Omega]$$

With the value of  $R_{pu}$  to satisfy the above equation,  $V_{OLM}$  becomes 0.4V or lower, and with  $V_{ILE}(=1.5V)$ , the equation ② is also satisfied.

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make CSB pull up.

#### ○Pull down resistance

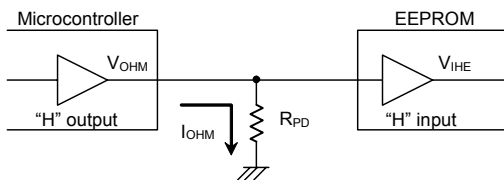


Fig.52 Pull down resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad \dots \textcircled{3}$$

$$V_{OHM} \geq V_{IHE} \quad \dots \textcircled{4}$$

Example) When  $V_{CC}=5V$ ,  $V_{OHM}=V_{CC}-0.5V$ ,  $I_{OHM}=0.4mA$ ,  $V_{IHE}=V_{CC} \times 0.7V$ , from the equation ③,

$$R_{PD} \geq \frac{5-0.5}{0.4 \times 10^{-3}}$$

$$\therefore R_{PD} \geq 11.3[k\Omega]$$

Further, by amplitude  $V_{IHE}$ ,  $V_{ILE}$  of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of  $V_{CC}$  /  $GND$  level to input, more stable high speed operations can be realized. On the contrary, when amplitude of  $0.8V_{CC}$  /  $0.2V_{CC}$  is input, operation speed becomes slow.<sup>\*1</sup>

In order to realize more stable high speed operation, it is recommended to make the values of  $R_{PU}$ ,  $R_{PD}$  as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of  $V_{CC}$  /  $GND$  level.

(\*1 At this moment, operating timing guaranteed value is guaranteed.)

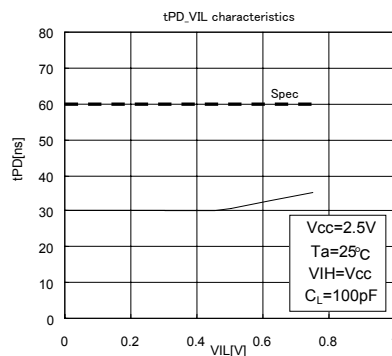


Fig.53 VIL dependency of data output delay time tPD

#### ○SO load capacity condition

Load capacity of SO output terminal affects upon delay characteristic of SO output. (Data output delay time, time from HOLDB to High-Z) In order to make output delay characteristic into higher speed, make SO load capacity small. In concrete, "Do not connect many devices to SO bus", "Make the wire between the controller and EEPROM short", and so forth.

#### ○Other cautions

Make the wire length from the microcontroller to EEPROM input signal same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

● I/O equivalence circuit

○ Output circuit

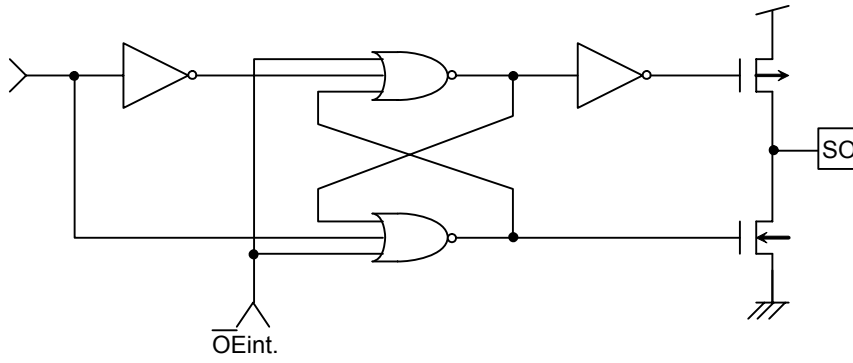


Fig.54 SO output equivalent circuit

○ Input circuit

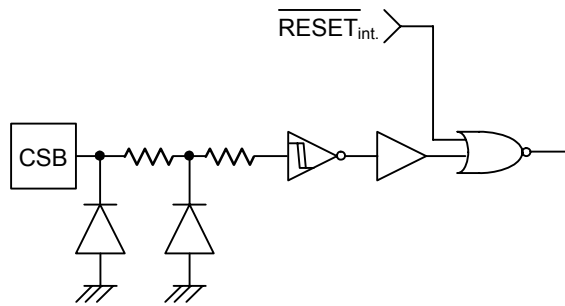


Fig.55 CSB input equivalent circuit

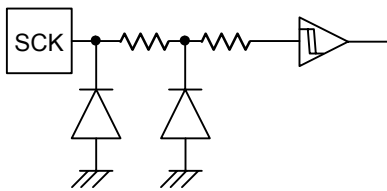


Fig.56 SCK input equivalent circuit

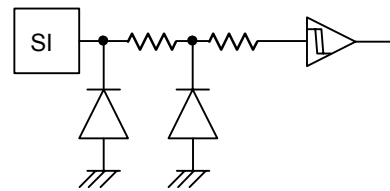


Fig.57 SI input equivalent circuit

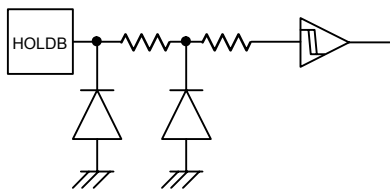


Fig.58 HOLDB input equivalent circuit

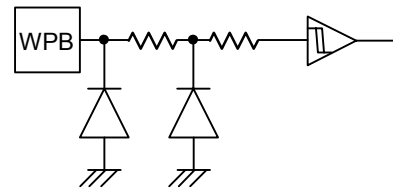


Fig.59 WPB input equivalent circuit

### ●Notes on power ON/OFF

○At power ON/OFF, set CSB "H" (=VCC).

When CSB is "L", this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CSB "H". (When CSB is in "H" status, all inputs are canceled.)

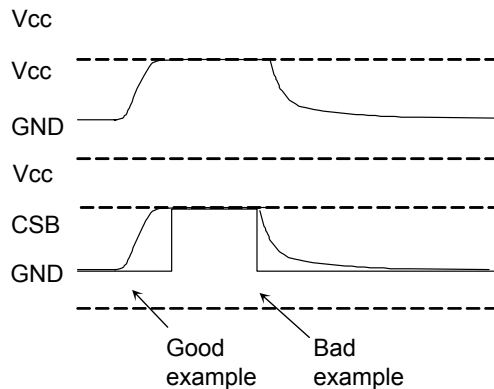


Fig.60 CSB timing at power ON/OFF

(Good example) CSB terminal is pulled up to VCC.

At power OFF, take 10ms or higher before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

(Bad example) CSB terminal is "L" at power ON/OFF.

In this case, CSB always becomes "L" (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.

Even when CSB input is High-Z, the status becomes like this case, which please note.

### ○LVCC circuit

LVCC (VCC-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.

At LVCC voltage (Typ. =1.9V) or below, it prevent data rewrite.

### ○P.O.R. circuit

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following  $t_R$ ,  $t_{OFF}$ , and  $V_{bot}$  are not satisfied, it may become write enable status owing to noises and the likes.

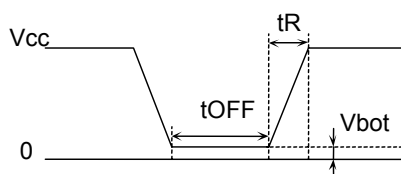


Fig.61 Rise waveform

Recommended conditions of  $t_R$ ,  $t_{OFF}$ ,  $V_{bot}$

$t_R$	$t_{OFF}$	$V_{bot}$
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

### ●Noise countermeasures

#### ○VCC noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1 $\mu$ F) between IC VCC and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board VCC and GND.

#### ○SCK noise

When the rise time ( $t_R$ ) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time ( $t_R$ ) of SCK 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

#### ○WPB noise

During execution of write status register command, if there exist noises on WPB pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

**●Operational Notes**

- (1) Described numeric values and data are design representative values, and the values are not guaranteed.
- (2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.
- (3) Absolute maximum ratings  
If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.
- (4) GND electric potential  
Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.
- (5) Terminal design  
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.
- (6) Terminal to terminal shortcircuit and wrong packaging  
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.
- (7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

**Status of this document**

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

### ●Ordering Information

Product code description

B	R	2	5	H	3	2	0	x	x	x	-	2	C	x	x
<b>BUS type</b> 25: SPI															
<b>Operating temperature</b> H: -40°C to +125°C															
<b>Capacity</b> 320 = 32K															
<b>Package</b> FVM: MSOP8    FVT: TSSOP-B8    F: SOP8    FJ: SOP-J8															
<b>Process Code</b>															

### Packaging and forming specification

E2: Embossed tape and reel

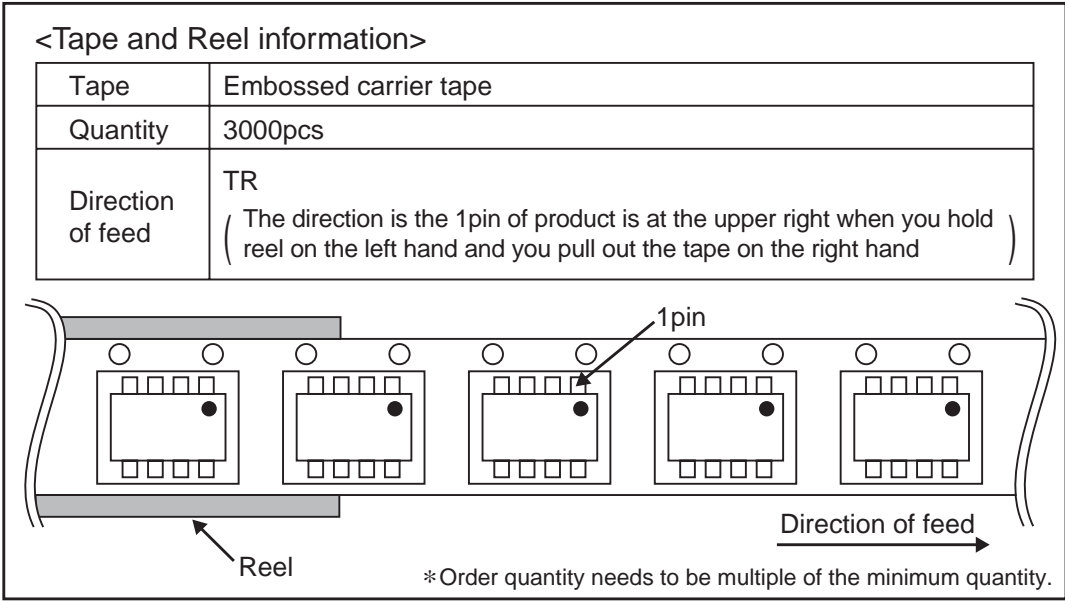
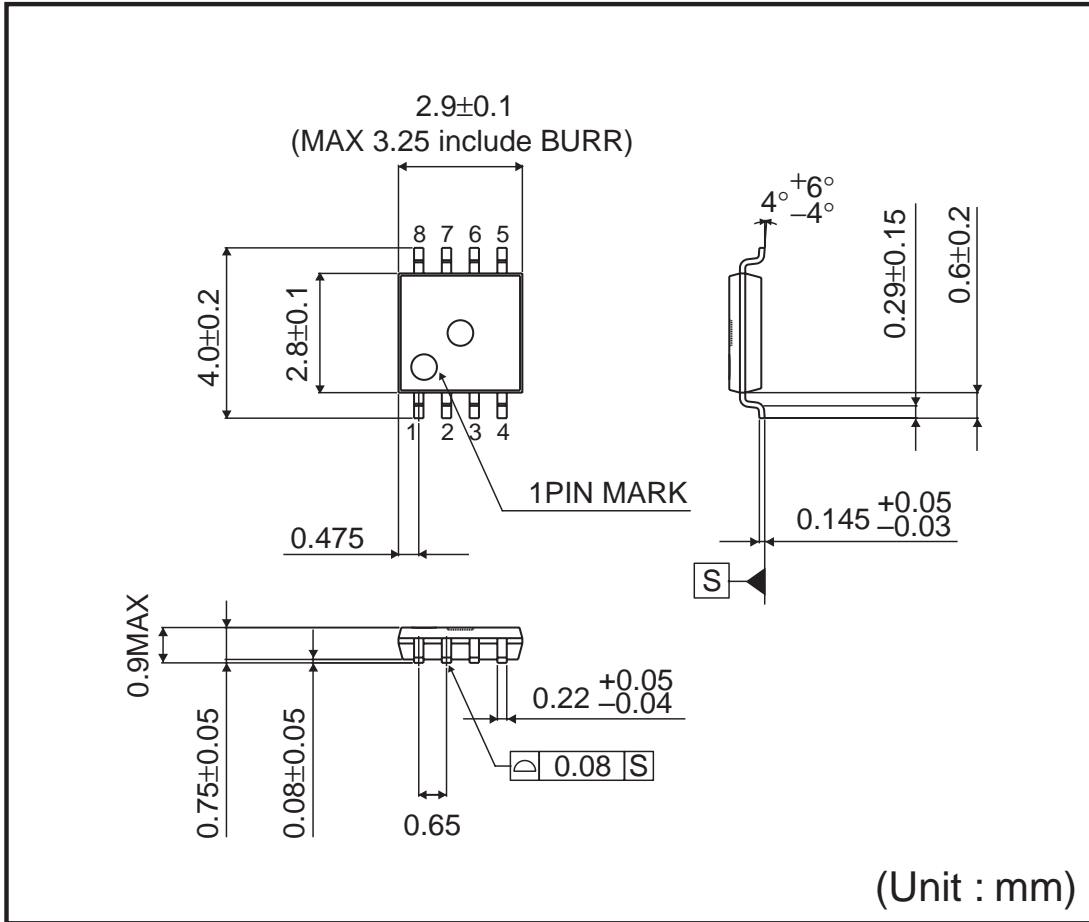
TR: Embossed tape and reel (MSOP8 package only)

### ●Lineup

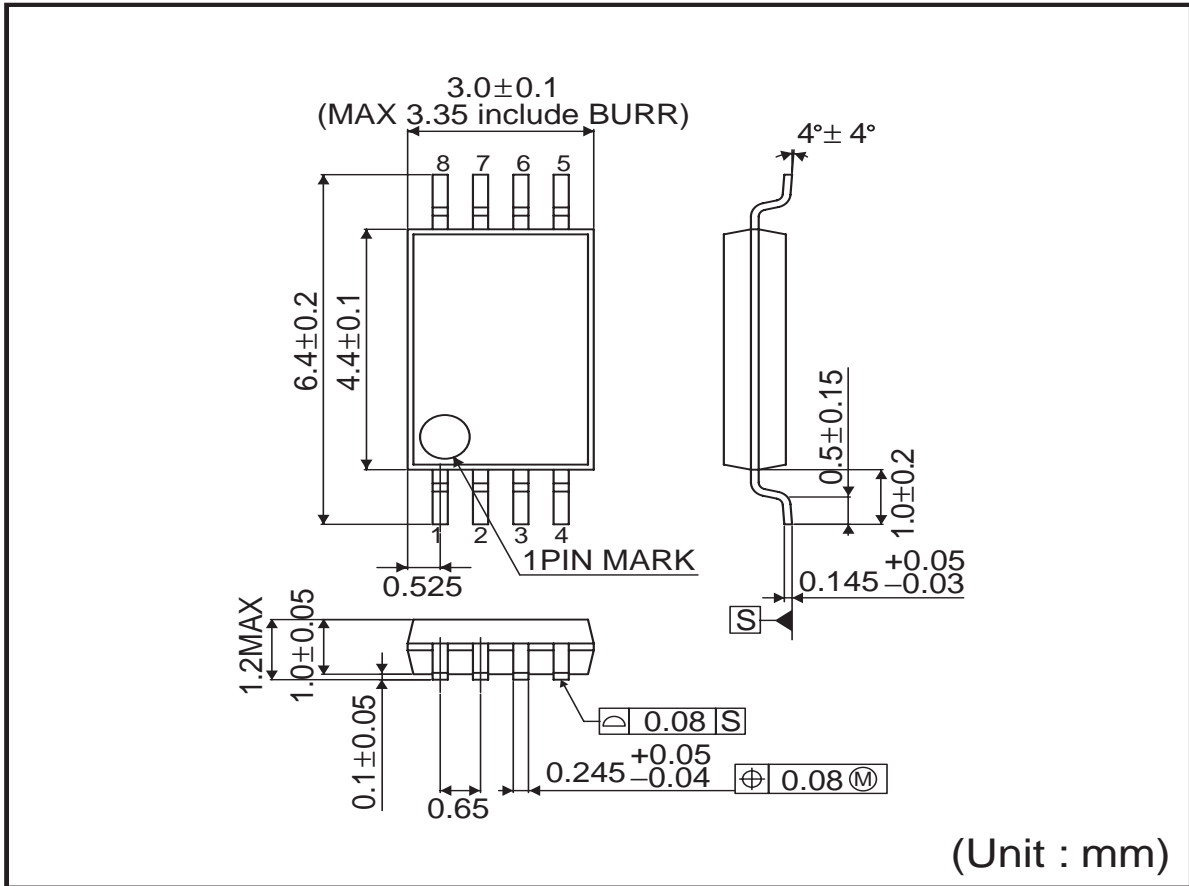
Capacity	Package		Orderable Part Number
	Type	Quantity	
32K	MSOP8	Reel of 3000	BR25H320FVM-2CTR
	TSSOP-B8		BR25H320FVT-2CE2
	SOP8	Reel of 2500	BR25H320F-2CE2
	SOP-J8		BR25H320FJ-2CE2

●Physical Dimension Tape and Reel Information

MSOP8

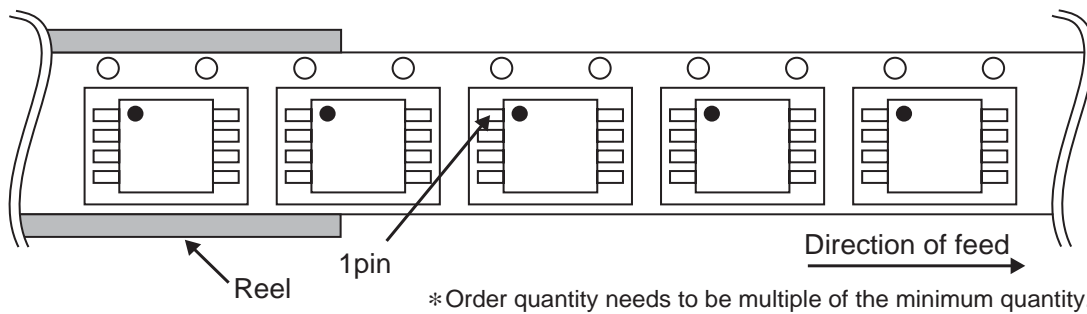


TSSOP-B8

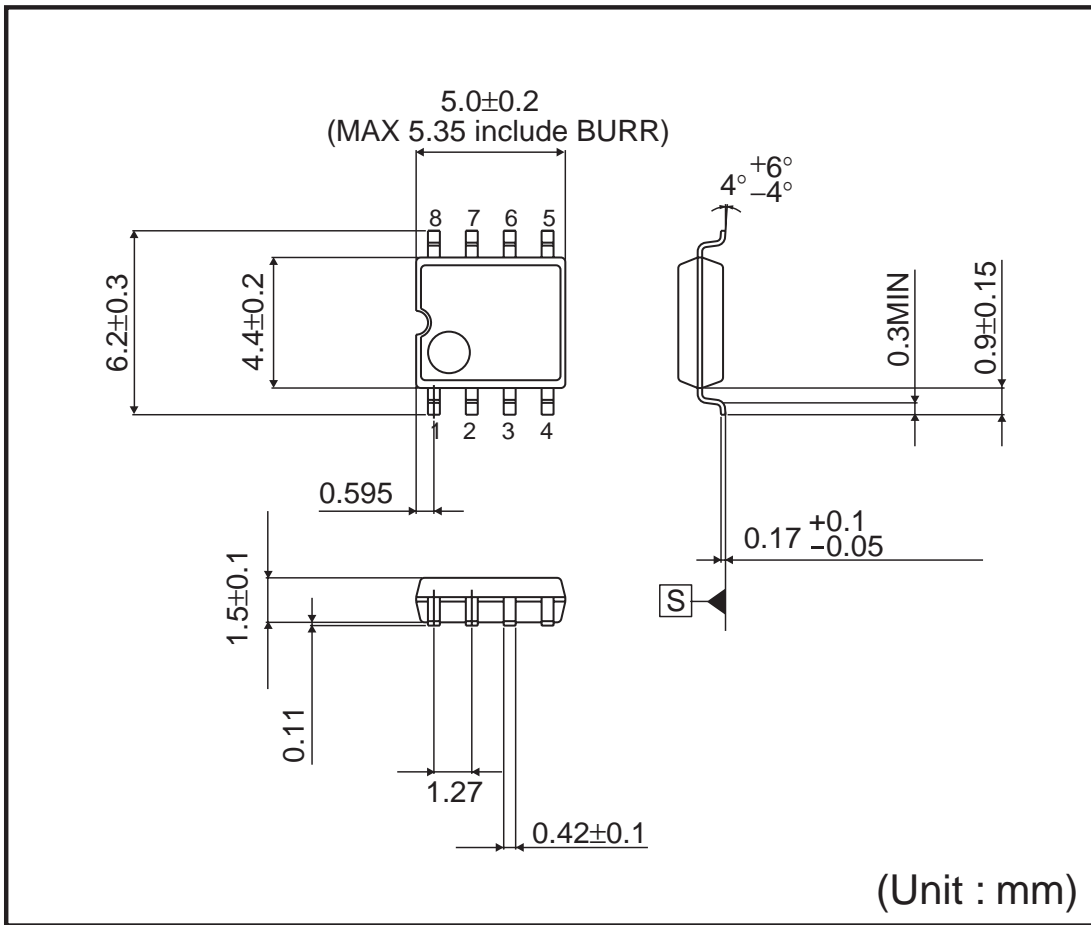


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand )

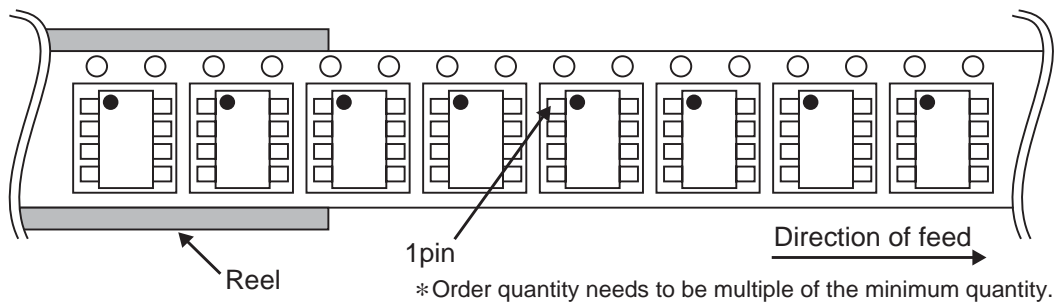


SOP8

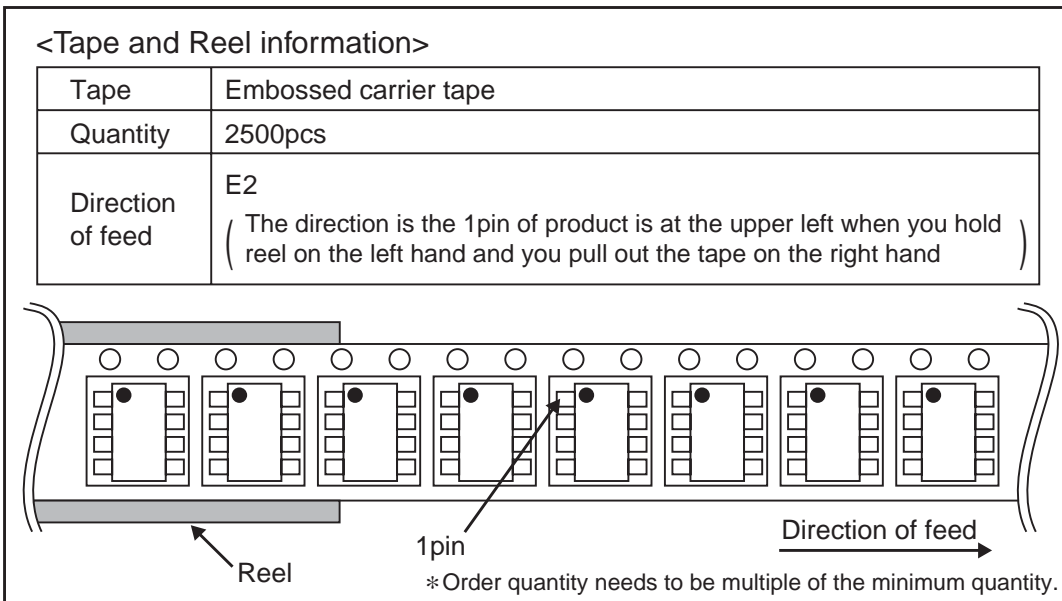
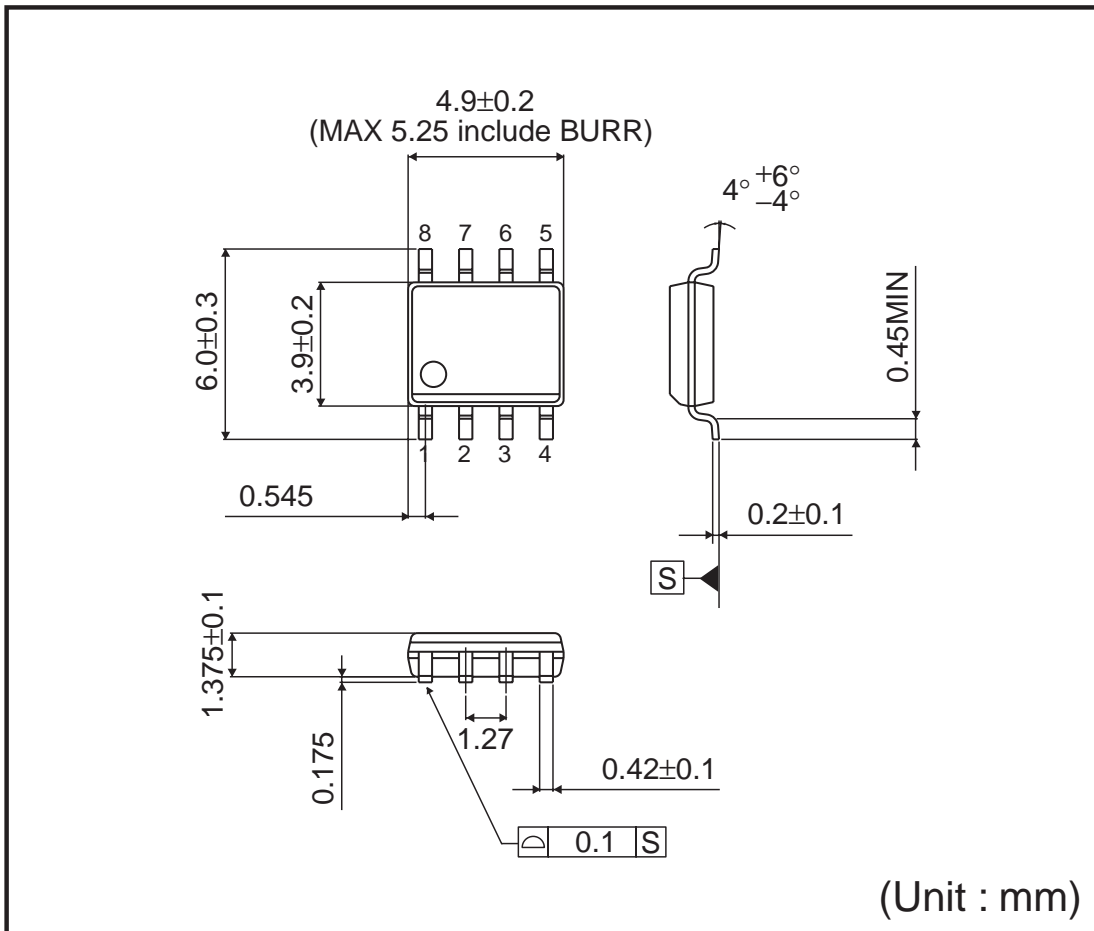


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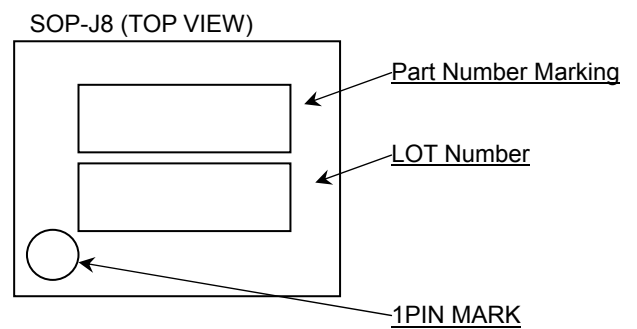
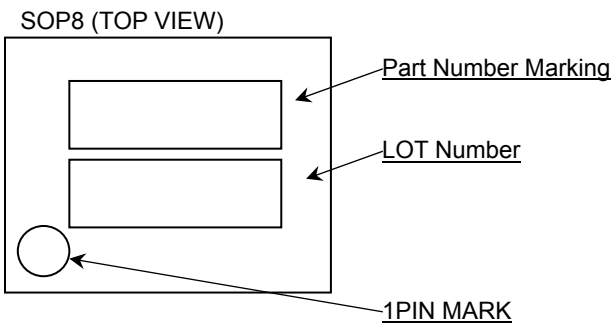
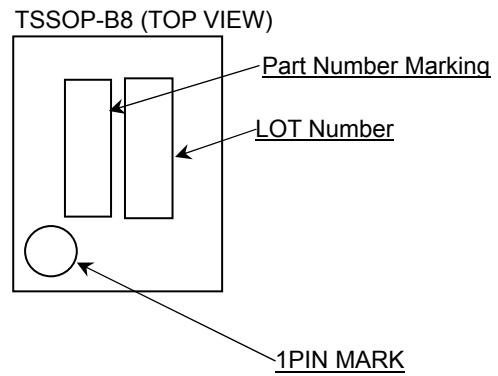
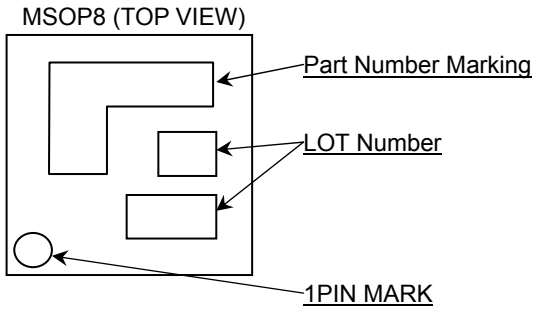
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 ( The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand )



SOP-J8



●Marking Diagrams(TOP VIEW)



Capacity	Product Name Marking	Package
32K	H320	MSOP8
		TSSOP-B8
		SOP8
		SOP-J8

●Revision History

Date	Revision	Changes
27. Apr. 2012	001	New Release

# Notice

## ●General Precaution

- 1) Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.
- 2) All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

## ●Precaution on using ROHM Products

- 1) Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment, transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.
- 2) ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
  - [a] Installation of protection circuits or other protective devices to improve system safety
  - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- 3) Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
  - [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
  - [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
  - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - [f] Sealing or coating our Products with resin or other coating materials
  - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - [h] Use of the Products in places subject to dew condensation
- 4) The Products are not subject to radiation-proof design.
- 5) Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- 8) Confirm that operation temperature is within the specified range described in the product specification.
- 9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

**●Precaution for Mounting / Circuit board design**

- 1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- 2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

**●Precautions Regarding Application Examples and External Circuits**

- 1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
- 2) You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

**●Precaution for Electrostatic**

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

**●Precaution for Storage / Transportation**

- 1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
- 2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
- 4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

**●Precaution for Product Label**

QR code printed on ROHM Products label is for ROHM's internal use only.

**●Precaution for Disposition**

When disposing Products please dispose them properly using an authorized industry waste company.

**●Precaution for Foreign Exchange and Foreign Trade act**

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

**●Precaution Regarding Intellectual Property Rights**

- 1) All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:
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●Other Precaution

- 1) The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.
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