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HyperTransport 3 Solution

Data Sheet

The HyperTransport analysis probes enable designers to debug, test, and verify compliance of 8 and 16 bit HyperTransport links. The analysis probe provides a mechanical, electrical and software interface between your 5.2 GT/s HyperTransport bus and an Agilent logic analyzer. The probe provides quick and reliable connections to your system under test and has internal termination networks that minimize the effects of loading and reflections on your HyperTransport bus during probing. The protocol decode software decodes and displays incoming data on your logic analyzer to make it easy for you to debug your design problems.

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Features

- Analysis of HyperTransport bus up to 5.2 GT/s. Scalable high speed integrity architecture.
- Support configuration for 8 bit and 16 bit operation
- Full duplex mode (T_x and R_x) – DC coupled probe architecture with interposer probe for both single and dual lane measurement
- Non-intrusive probing of midbus using unique soft touch connectorless probing technology
- Logic analysis triggering and decoding of HyperTransport buses at the packet level with Packet Viewer software
- Triggering capability with raw 36-bit pattern matching and menu driven command triggering
- NOOP filtering with or without flow control

Complete system

Use a 16900 Series logic analyzer with the analysis probe in your development lab for design and functional validation of HyperTransport architectures. The analysis probe provides low-intrusion probing of the bus, packet analysis and packet triggering to help you pinpoint your problem areas quickly. The probe supports data scrambling and flexible lane widths so you can make sure your design is consistent with HyperTransport standards. The interposer and midbus probing option make it easy for you to reliably connect to your device.

Figure 1. Ensure non-intrusive connection to an embedded system with a midbus probe using soft touch connectorless probing technology.

Probe connections

HT3-Only Footprint

Figure 2 below shows HT3 footprint which utilizes the same mechanical footprint as Agilent's PCIe2 probe. Note that this footprint is not backward compatible with the HT1 tools available today.

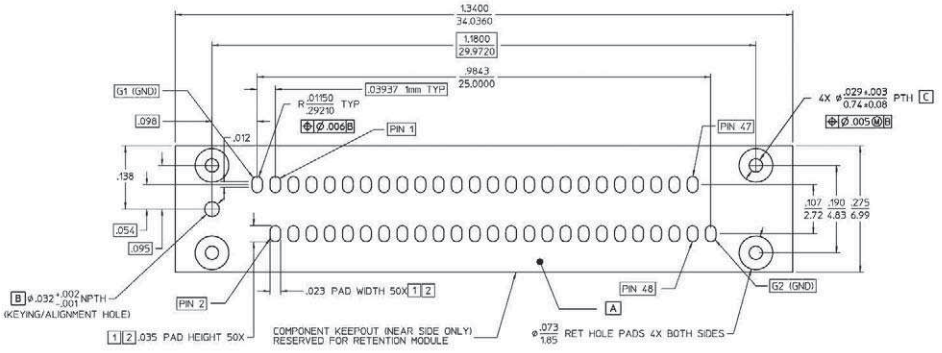


Figure 2. HT3 footprint

HT3 Midbus Pin	HT3 Signal	HT3 Midbus Pin	HT3 Signal
—	* No Pad *	G1	GND
2	GND	1	NC
4	NC	3	NC
6	NC	5	GND
8	GND	7	CAD[0]_H
10	CAD[1]_H	9	CAD[0]_L
12	CAD[1]_L	11	GND
14	GND	13	CAD[2]_H
16	CAD[3]_H	15	CAD[2]_L
18	CAD[3]_L	17	GND
20	GND	19	PWROK_H
22	NC	21	PWROK_L
24	NC	23	GND
26	GND	25	CLK[0]_H
28	CAD[4]_H	27	CLK[0]_L
30	CAD[4]_L	29	GND
32	GND	31	CAD[5]_H
34	CAD[6]_H	33	CAD[5]_L
36	CAD[6]_L	35	GND
38	GND	37	CAD[7]_H
40	CTL[0]_H	39	CAD[7]_L
42	CTL[0]_L	41	GND
44	GND	43	RESET_H
46	LDT_STOP_H	45	RESET_L
48	LDT_STOP_L	47	GND
G2	GND	—	* No Pad *

Table 1. Pinout for CAD[7:0] (Lower)

HT3 Midbus Pin	HT3 Signal	HT3 Midbus Pin	HT3 Signal
—	* No Pad *	G1	GND
2	GND	1	NC
4	NC	3	NC
6	NC	5	GND
8	GND	7	CAD[8]_H
10	CAD[9]_H	9	CAD[8]_L
12	CAD[9]_L	11	GND
14	GND	13	CAD[10]_H
16	CAD[11]_H	15	CAD[10]_L
18	CAD[11]_L	17	GND
20	GND	19	PWROK_H
22	NC	21	PWROK_L
24	NC	23	GND
26	GND	25	CLK[1]_H
28	CAD[12]_H	27	CLK[1]_L
30	CAD[12]_L	29	GND
32	GND	31	CAD[13]_H
34	CAD[14]_H	33	CAD[13]_L
36	CAD[14]_L	35	GND
38	GND	37	CAD[15]_H
40	CTL[1]_H	39	CAD[15]_L
42	CTL[1]_L	41	GND
44	GND	43	RESET_H
46	LDT_STOP_H	45	RESET_L
48	LDT_STOP_L	47	GND
G2	GND	—	* No Pad *

Table 2. Pinout for CAD[15:8] (Upper)

Probe connections

Soft Touch Twin Footprint

Figure 3 below shows Agilent Technologies Soft Touch Twin footprint with today's HT1 tools utilizing the Industry Standard Connectorless Probe and with Agilent's HT3 tools of the future. If you want to design a midbus footprint into your system that will accommodate both today's HT1 tools and Agilent's HT3 tool, you should design in the "Soft Touch Twin" footprint.

There is one minor change to the Industry Standard Connectorless Probe footprint: pin A27 must be tied to GND in the Soft Touch Twin pinout, rather than to ID[0] as in the original Industry Standard pinout. In addition to this change, the other pinout requirement to make special note of is that the PWROK pair is routed to pins C12 and C13 in addition to pins B26 and B27 in the Industry Standard footprint. Finally, please note that positions C1 and C27 have no pads in the Soft Touch Twin footprint. A red font is used for these pads numbers and signal names in the tables below to highlight their unique handling in the Soft Touch Twin pinout for HT3. Note also that the differential signals in rows B and C are essentially "double probed."

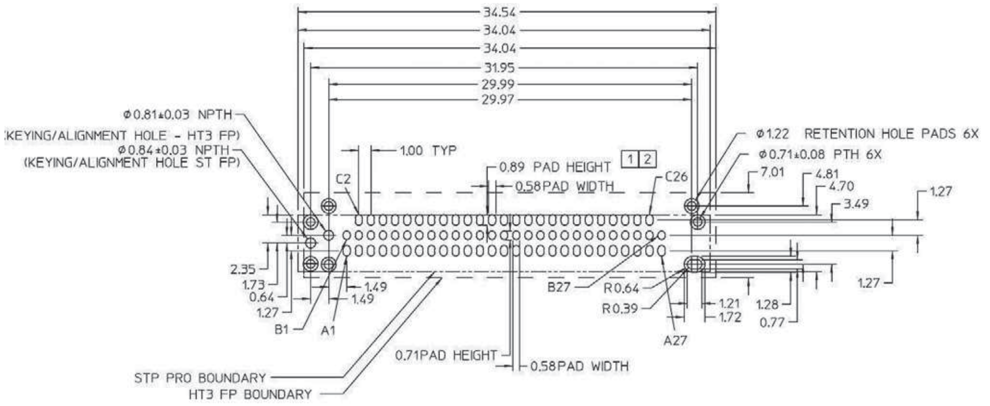


Figure 3. "Soft Touch Twin" footprint for HT1 and HT3 tool

Soft Touch Twin Pin	HT3 Signal	Soft Touch Twin Pin	HT3 Signal	Soft Touch Twin Pin	HT3 Signal
A1	NC	B1	ID[2]	C1	* No Pad *
A2	NC	B2	NC	C2	GND
A3	GND	B3	NC	C3	NC
A4	NC	B4	GND	C4	NC
A5	NC	B5	CAD[0]_H	C5	GND
A6	GND	B6	CAD[0]_L	C6	CAD[0]_H
A7	CAD[1]_H	B7	GND	C7	CAD[0]_L
A8	CAD[1]_L	B8	CAD[2]_H	C8	GND
A9	GND	B9	CAD[2]_L	C9	CAD[2]_H
A10	CAD[3]_H	B10	GND	C10	CAD[2]_L
A11	CAD[3]_L	B11	NC	C11	GND
A12	GND	B12	NC	C12	PWROK_H
A13	NC	B13	GND	C13	PWROK_L
A14	NC	B14	CLK[0]_H	C14	GND
A15	GND	B15	CLK[0]_L	C15	CLK[0]_H
A16	CAD[4]_H	B16	GND	C16	CLK[0]_L
A17	CAD[4]_L	B17	CAD[5]_H	C17	GND
A18	GND	B18	CAD[5]_L	C18	CAD[5]_H
A19	CAD[6]_H	B19	GND	C19	CAD[5]_L
A20	CAD[6]_L	B20	CAD[7]_H	C20	GND
A21	GND	B21	CAD[7]_L	C21	CAD[7]_H
A22	CTL[0]_H	B22	GND	C22	CAD[7]_L
A23	CTL[0]_L	B23	RESET_H	C23	GND
A24	GND	B24	RESET_L	C24	RESET_H
A25	LDT_STOP_H	B25	ID[1]	C25	RESET_L
A26	LDT_STOP_L	B26	PWROK_H	C26	GND
A27	GND	B27	PWROK_L	C27	* No Pad *

Table 3. Soft Touch Twin pinout for CAD[7:0] (Lower)

Soft Touch Twin Pin	HT3 Signal	Soft Touch Twin Pin	HT3 Signal	Soft Touch Twin Pin	HT3 Signal
A1	NC	B1	ID[2]	C1	* No Pad *
A2	NC	B2	NC	C2	GND
A3	GND	B3	NC	C3	NC
A4	NC	B4	GND	C4	NC
A5	NC	B5	CAD[8]_H	C5	GND
A6	GND	B6	CAD[8]_L	C6	CAD[8]_H
A7	CAD[9]_H	B7	GND	C7	CAD[8]_L
A8	CAD[9]_L	B8	CAD[10]_H	C8	GND
A9	GND	B9	CAD[10]_L	C9	CAD[10]_H
A10	CAD[11]_H	B10	GND	C10	CAD[10]_L
A11	CAD[11]_L	B11	NC	C11	GND
A12	GND	B12	NC	C12	PWROK_H
A13	NC	B13	GND	C13	PWROK_L
A14	NC	B14	CLK[1]_H	C14	GND
A15	GND	B15	CLK[1]_L	C15	CLK[1]_H
A16	CAD[12]_H	B16	GND	C16	CLK[1]_L
A17	CAD[12]_L	B17	CAD[13]_H	C17	GND
A18	GND	B18	CAD[13]_L	C18	CAD[13]_H
A19	CAD[14]_H	B19	GND	C19	CAD[13]_L
A20	CAD[14]_L	B20	CAD[15]_H	C20	GND
A21	GND	B21	CAD[15]_L	C21	CAD[15]_H
A22	CTL[1]_H	B22	GND	C22	CAD[15]_L
A23	CTL[1]_L	B23	RESET_H	C23	GND
A24	GND	B24	RESET_L	C24	RESET_H
A25	LDT_STOP_H	B25	ID[1]	C25	RESET_L
A26	LDT_STOP_L	B26	PWROK_H	C26	GND
A27	GND	B27	PWROK_L	C27	* No Pad *

Table 4. Soft Touch Twin pinout for CAD[15:8] (Upper)

Interposer probe

The high-speed signals along with DC level startup conditions have made it almost impossible to use typical AC coupled probe architectures (snooping probe) without significantly effecting the measurement. The Interposer probe is a DC coupled probe that acts as a "man-in-the middle" between the CPU and the downstream device and sends a buffered copy of the link data to the HT3 logic analysis probe for analysis. The end result is full eyes at probe and target since the signals are buffered and sent back out to the target and the probe.

HT3 Interposer

HT3 logic analysis probe

Figure 4. DC coupled interposer probe sends buffered copy of the link data from the target to the HT3 logic analysis probe.

The Interposer probe has configurations for both single lane (L1) and dual lane (L1L0) applications. The dual lane socket can be used in single lane mode (L1 or L0) if desired. The Interposer solution along with LAI can be ordered from Astek Corporation as a single unit. The table below gives the configurations allowed with the current HT3 LAI and Interposer probe system for various applications.

	Number of LAIs required	Number of single lane Interposers required	Number of Dual Lane Interposers required (use one or two lanes)
x8 US/DS*	1	1	1
x16 US or DS**	1	1	1
x16 US/DS	2	1	1
2 lanes x16 US/DS	4	N/A	1***

* *US/DS corresponds to full-duplex upstream and downstream.*

** *US or DS corresponds to either upstream or downstream.*

*** *Dual lane measurements require some additional hardware over single lane.*

HyperTransport 3 analysis probe

The HyperTransport analysis probe is capable of probing at a serial data rate of 5.2 Gb/s – it's the speed of standard HyperTransport 3 bus so you can be confident your bus works at HyperTransport 3 speeds. The probe monitors two directions of x8 and x16 links so you can accurately capture the packet of interest. The probe is designed to handle a single, unidirectional link or a bidirectional link.

Protocol decode software

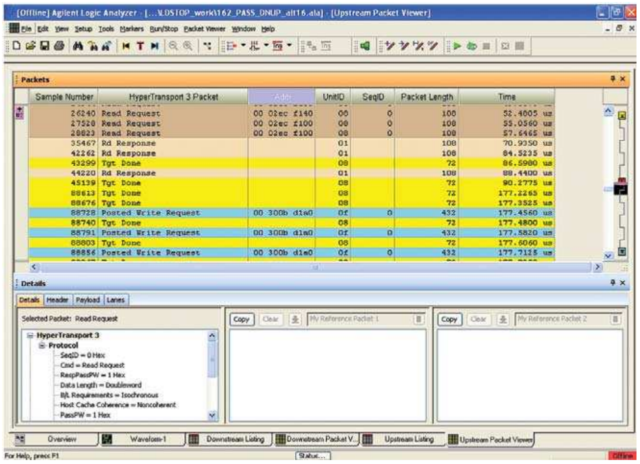
The analysis probe, which includes protocol decode software for 16900 Series logic analyzers, acquires serial data, converts it to parallel form, recognizes and filters packets, and clocks the information into the analyzer. Data sent to the logic analyzer includes:

- Captured data
- Packet type and state information
- Packet recognizers and error indicators

This data is processed by the protocol decoder for display of packets, transactions and errors. You can view the packet decode data with the Packet Viewer tool. Although the probe hardware has the ability to filter and trigger, the software interface provides bits arranged to support the use of logic-analyzer-based trigger functions, even on packet-based data. The decoder detects packet types and checks packet delimiters (minimal protocol checking).

Packet Viewer software

Packet Viewer software is a powerful tool for easy analysis of protocol traffic. Packet viewer provides bidirectional information in a single display. Packet viewer allows packet-to-packet comparisons and detailed information on each lane, header format and payload.



Sample Number	HyperTransport 3 Packet	Addr	UnitID	SeqID	Packet Length	Time
26240	Read Request	00 02ec f140	08	0	108	52.4005 us
27528	Read Request	00 02ec f100	08	0	108	55.0560 us
28823	Read Request	00 02ec f100	08	0	108	57.6465 us
35467	Rd Response		01		108	70.9350 us
42262	Rd Response		01		108	84.5235 us
43299	Tgt Done		08		72	86.5980 us
44220	Rd Response		01		108	88.4400 us
45139	Tgt Done		08		72	90.2775 us
88613	Tgt Done		08		72	177.2265 us
88676	Tgt Done		08		72	177.3525 us
88728	Posted Write Request	00 300b d1a0	0f	0	432	177.4560 us
88740	Tgt Done		08		72	177.4800 us
88791	Posted Write Request	00 300b d1a0	0f	0	432	177.5820 us
88803	Tgt Done		08		72	177.6060 us
88856	Posted Write Request	00 300b d1a0	0f	0	432	177.7125 us

Selected Packet: Read Request

- HyperTransport 3
  - Protocol
    - SeqID = 0 Hex
    - Cmd = Read Request
    - RespPassPW = 1 Hex
    - Data Length = Doubleword
    - B/L Requirements = Isochronous
    - Host Cache Coherence = Noncoherent
    - PassPW = 1 Hex

Figure 5. Packet Viewer – see packet and lane decode in an intuitive format.

Configuration guide

Bidirectional x8 lane width or one directional x16 lane width – Midbus probe

Product	Description	Quantity
AHT3-LAI-01	HyperTransport 3 analysis probe	1
One of the following 16900 Series logic analyzers:		
16902B	6-slot mainframe with 15-in touch display	1
One of the following modules:		
16950B	68-channel 4 GHz timing, 667 MHz state logic analysis module	3
16951B	68-channel 4 GHz timing, 667 MHz state/deep logic analysis module	3
N4246A	Midbus probe bi-directional X8 for HT3 5.2GB/s	2
E5378A	34-ch single-ended SAMTEC connector probe, connects to 90-pin LA cable	5

Bidirectional x8 lane width or one bidirectional x16 lane width – Interposer probe

Product	Description	Quantity
AHT3-LAI-01	HyperTransport 3 analysis probe	1
16902B	6-slot mainframe with 15-in touch display	1
One of the following modules:		
16950B	68-channel 4 GHz timing, 667 MHz state logic analysis module	3
16951B	68-channel 4 GHz timing, 667 MHz state/deep logic analysis module	3
One of the following interposer:		
Single lane AHT3-INT-01	RHL1 Single Lane Interposer	1
Dual lane AHT3-INT-02	L1L0 Dual Lane Interposer	1
Dual lane AHT3-ADP-01	Dual lane additional adapter kit (Only needed for Dual Lane measurements using the L0L1 Dual Lane Interposer, AHT3-INT-02)	1
E5378A	34-ch single-ended SAMTEC connector probe, connects to 90-pin LA cable	6

Ordering information

Model number	Product
AHT3-LAI-01	HyperTransport 3 Analysis Probe
AHT3-INT-01	RHL1 Single Lane Interposer
AHT3-INT-02	L1L0 Dual Lane Interposer
AHT3-ADP-01	Dual Lane additional adapter kit

Contact information:
5055 Corporate Plaza Drive,
Colorado Springs, CO 80919
Phone: 1-(866)-427-8351
Fax: 1-(719)-260-1668
Company URL: **www.astekcorp.com**

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Revised: October 6, 2008

Related literature

Publication title	Publication type	Publication number
Agilent Technologies 16900 Series logic analyzer	Color brochure	5989-0420EN

Printed in USA, December 17, 2008
5989-6652EN

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