

Agilent Technologies System Protocol Tester E2980A Protocol Exerciser and Analyzer for Advanced Switching Interconnect (ASI)

Data Sheet



- Faster, easier and more effective ASI turn-on, debug, validation and compliance testing
- Combined traffic generation and protocol analysis dramatically increase your test coverage to reduce the risk of costly redesigns and recalls
- Large probing portfolio with ATCA interposer, PCI Express interposer and midbus probing for flexible connection
- Universal hardware platform reduces expenditures for test equipment – use it for ASI and PCI Express today; upgrade to cover selected future serial protocols up to 3.125 Gbps



Agilent Technologies

E2980A protocol exerciser and analyzer for ASI offers the features and capabilities you need to test your ASI design quickly, easily and thoroughly

Applications

- Turn-on and debug ASI systems, cards, chips, software, drivers and BIOS
- Validate ASI chips and backplane based systems – stress testing, worst-case-scenario testing, and error-behavior testing
- ASI compliance testing

Key features

- True bidirectional analyzer/exerciser for ASI x1, x2, x4 and x8
- Use the exerciser/protocol analyzer capabilities in combination to analyze root causes of problems with ease
- For easier validation, capture traffic conditions, then drag and drop to reproduce system problems
- Multiport testing allows you to stress all paths with the same load conditions and synchronize the tests
- External trigger in/out to synchronize with other devices
- Connect to your device with an ATCA or PCI Express non-intrusive passive or active slot/interposer probe or a soft touch midbus probe
- Multiprotocol test/cross bus analysis for semiconductors, cards and systems – simultaneously record PCI Express, Fibre Channel and Advanced Switching Interconnect traffic and transactions and time-correlate them within the same test setup and graphical user interface
- Intuitive GUI lets you view and set up tests with ease
- LAN interface enables remote control and resource sharing
- FPGA-based tool permits easy upgrades
- Flexible and extendable platform protects your hardware investment

Protocol exerciser: stress your system to the max in the shortest period of time

- Generates and responds to ASI packets and packet sequences
- GUI, DCOM application programming interface and TCL interfaces
- Error insertion lets you test corner cases and failure behavior
- Emulate active ASI devices or large ASI topologies
- Performance counters
- Fabric manager testing/emulation
- Guarantee QoS with the support of 20 virtual channels
- Supports tunneling with flexible packet generation/receiving including all PIs
- 2 MB packet memory to emulate any real ASI end node or device

Protocol analyzer: turn on and debug ASI designs faster and more easily

- ASI protocol representation of all PIs and decoding of PI0, PI1, PI2, PI4, PI5, PI97
- Root cause and performance analysis
- GUI with graphical trigger setup, search and filter capabilities
- Sophisticated trigger capability with storage qualifications
- 1 GB trace memory
- Traffic overview
- Packet decode view
- Performance counters

An intuitive tool for every stage of ASI development

The E2980A protocol analyzer and exerciser makes it easier than ever before to turn on, debug and validate your ASI systems and devices and allows you to check them for compliance.

To thoroughly test your ASI systems and devices, you may need to create system conditions that are difficult to reproduce with existing ASI equipment. The E2980A protocol exerciser and analyzer lets you quickly and easily simulate traffic or capture traffic conditions and recreate them. The protocol exerciser lets you stress all data paths in a system and test corner cases and behavior by inserting errors and protocol violations on each layer (physical, data-link, and transaction layer).

The protocol analyzer, including Agilent's sophisticated trigger capabilities, is the core debug and turn-on test tool for root cause analysis, troubleshooting and performance analysis. It provides non-intrusive monitoring of ASI traffic between a card and a system or between a protocol exerciser and a system.

Versatile system architecture

To reduce your expenditures for test equipment, the E2980A uses the same hardware whether you are using it as an exerciser or an analyzer or both. To further protect your hardware investment, the scalable System Protocol Tester platform allows you to expand your test capabilities and upgrade as your needs change and as serial protocols evolve.

Platform features and benefits

- Universal and flexible hardware – use it for ASI, PCI Express and Fibre Channel (with a separate plug-in module) today, then upgrade to cover selected future serial protocols
- Flexible large probing portfolio with ATCA or PCI Express non-intrusive passive or active slot/interposer probes or a soft touch midbus probe
- Multiprotocol test/cross bus analysis for semiconductors, cards and systems – simultaneously record PCI Express, Fibre Channel and Advanced Switching Interconnect traffic and transactions and time-correlate them
- Familiar and consistent set up for future protocols shortens your learning curve
- Easy to upgrade and interchange software and hardware elements (for example, front-end probes and plug-in modules)

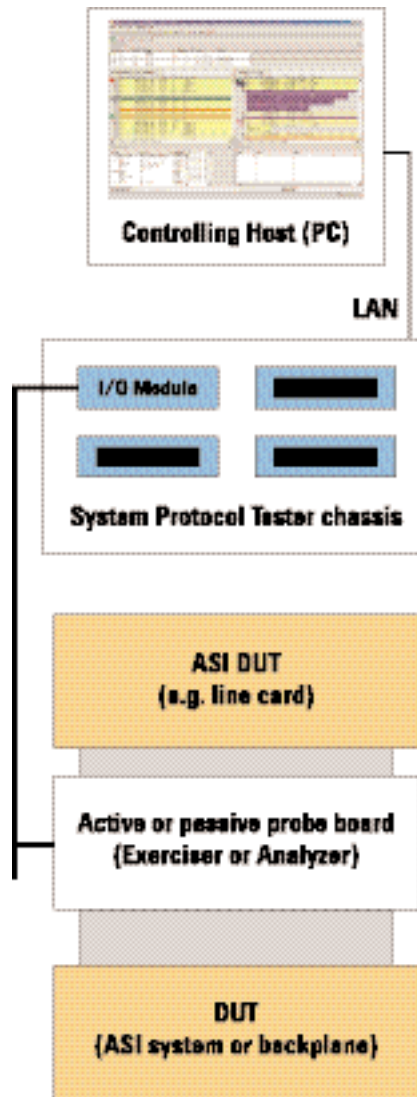


Figure 1. Typical test setup.

E2980A platform components

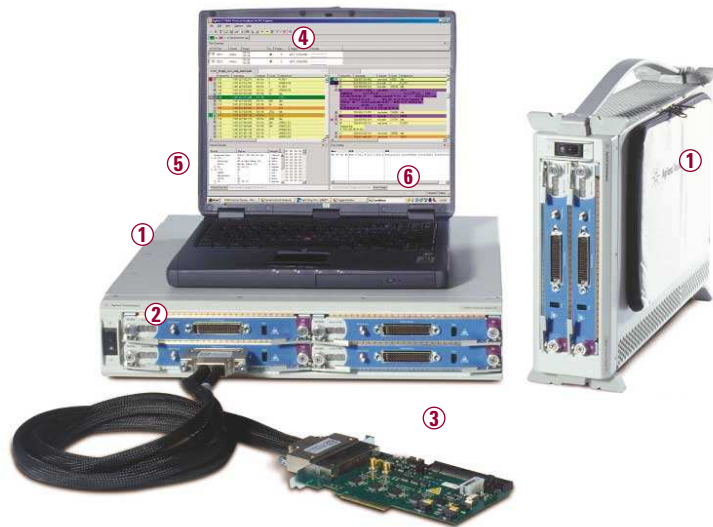


Figure 2. Platform components

- ① Chassis (2 slot or 4 slot)
- ② I/O module
- ③ PCIe Slot/interposer probe board or alternative ATCA interposer probe board
- ④ Protocol analyzer/exerciser software
- ⑤ LAN interface
- ⑥ PC for local control of the system (not included)

Choose a 2-slot or 4-slot chassis

You can monitor/test from one to four ASI links with the 2- and 4-slot chassis. The 2-slot chassis accommodates up to two serial I/O modules, and you can use it in either a vertical or horizontal orientation. This lightweight chassis has a built-in handle and soft carry bag with room for accessories. Use it for testing in scenarios where portability and small size are important.

The 4-slot chassis houses up to four serial I/O modules. Use it on your bench top or mount it in a rack. It is ideal for validation applications where you need multiple exercisers to stress and load system paths. You can connect multiple chassis and control/synchronize them from a single host.

Upgradeable serial I/O module

Every serial I/O module has an internal LAN interface that is connected to an Ethernet hub inside the chassis.

Flexible connectivity: slot/interposer probe board or midbus probe

A slot/interposer probe board provides the interface to your device under test (connected via a cable from the I/O module). A midbus probe is also available for the protocol analyzer. There are passive and active slot/interposer probe boards available. Go to page 13 to learn more.

Easy-to-use software

Use the intuitive E2980A analyzer and exerciser software packages to set up basic ASI packet tests quickly and easily. The various software packages enable you to access different applications. You can use the software in off-line mode to view captured traffic.

Controller

The chassis is connected via LAN to a controller PC that manages the behavior of the System Protocol Tester platform. The software runs on a remote client or on the controller PC itself.

E2980A protocol exerciser for ASI lets you test and validate your system's performance under varied conditions

With its fully adjustable parameters, the E2980A protocol exerciser lets you emulate any ASI devices and ASI topologies (star and dual). Additionally it is able to generate and respond to any ASI packets. It is an intelligent I/O communication tool that can react as an ASI end node or device. The E2980A exerciser's functionality extends far beyond the capabilities of a simple packet generator. It is tailored to validate corner cases and emulate stress conditions for components on system boards and cards. The protocol exerciser is the ideal tool to test and validate x1, x2, x4 or x8 ASI designs.

Perform worst-case-scenario tests

The E2980A exerciser lets you stress all parts of the ASI topology and test corner cases in your system so you can force it to fail. You can also insert errors and test the behavior of designs in response to these errors to enable worst-case-scenario testing.

Use the E2980A protocol exerciser to:

- Effective turn-on and debug ASI systems – Easily simulate the transaction layer and test the data link layer capabilities of a ASI device
- Validate ASI chips, cards and systems – Ensure the interoperability and stability of all data paths and get the largest possible test coverage with links to root cause analysis of problems
- Develop your design according to the specification – Support for checking your system for compliance

Flexible control

To set up basic ASI packets quickly and easily, use the intuitive E2980A exerciser graphical user interface (GUI). The GUI offers a menu display of the exerciser's capabilities. The GUI further increases flexibility by allowing you to set up single packets or sequences of packets. For more comprehensive automated tests, you can control the exerciser programmatically (the host software running on the system controller provides the protocol exerciser API). This means the exerciser can receive and react programmatically to incoming requests. The protocol exerciser API allows you to access all functions of the protocol exerciser via DCOM programming or TCL script. The API is implemented into the system as a DCOM interface, which can be shared between multiple applications. The protocol exerciser also has fully configurable ASI configuration space. In addition, the exerciser comes with a 2 MB packet receive memory, which is used to store received packets prior to handling them in the software. This means the exerciser reacts as a real ASI device.

Protocol exerciser capabilities and benefits

Generate ASI traffic quickly using the graphical user interface

- Set up general exerciser parameters (desired link width, lane skew, etc.) easily
- Easily record packets from the protocol analyzer and replay with the exerciser as many times as you want. Use drag and drop or copy and paste functionality or export files from the protocol analyzer.
- Easily see and edit to-be-transmitted ASI packets; decode and display received and transmitted packets
- Display and edit capabilities of emulated devices easily

Perform realistic tests with device emulation

- Simulate various test scenarios by setting exerciser parameters the way you want
- Minimize the number of real devices needed to create a large-scale test environment
- Large probing portfolio with ATCA interposer, PCIe interposer and midbus probing for flexible connection to the devices under test
- Turn on your fabric easily with basic fabric manager capabilities
- Connect your own fabric manager to the topology using the packet send/receive API of the exerciser
- Emulate your ASI topology with end nodes and switches to test your fabric management software
- Real-time data compare of incoming payload against algorithmically generated data
- 2 MB packet memory allows you to emulate any real ASI device

Increase test coverage with configurable traffic generation

- Transmit and receive ASI traffic at full bandwidth of x1, x2, x4 and x8 link widths with 2.5 Gbps
- Customize the traffic you send: Generate real-world requests with parameters and behaviors you define
- Validate the boundary conditions of your system
- Generate any combination of ASI packets for multiple ports and correlate the test results across time for comprehensive system testing
- Stress your system to the max: test your system under worst-case conditions and see how devices act during error conditions
- Algorithmic data generation for stress testing at line speed and unidirectional data verification

Real-time statistics help you see immediate changes in your system's performance

- Real-time performance counters
- Easily see performance statistics (bar graphs/textual)

Customize your measurements with test automation and scripting capabilities

- Control software via the programming interface through DCOM or TCL interfaces
- Create and automate your test procedure to eliminate tedious manual testing
- Repeat tests for subsequent product builds
- Automatic handling of PHY and DLL features-lane/link training, flow control and retry management

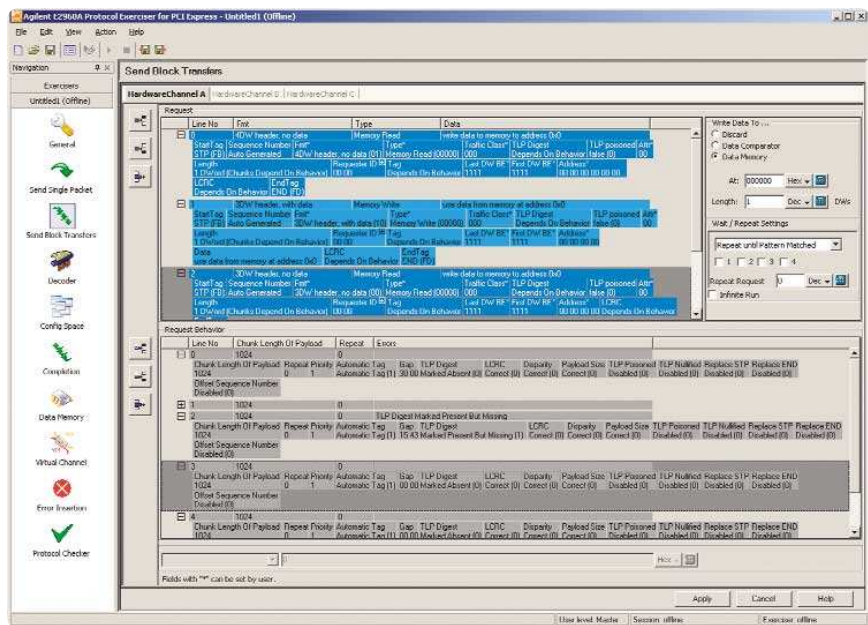


Figure 3. Protocol exerciser graphical user interface (e.g. PCI Express GUI)

Technical specifications for the protocol exerciser

E2980A exerciser features

Real-time performance counters	Several perform counters that gather data on various sent and receive DLLPs and TLPs
Data link layer features	Fully implemented data link control and management state machine Automatic flow control initialization; programmable credits and flow control update rate Autonomous generation of data link layer packets (DLLPs) Automatic generation and checking of LCRC and sequence numbers; allows the insertion of incorrect LCRCs into TLPs for testing purposes; automatic retry management Sending and receiving arbitrary DLLPs from user program
Physical layer features	Fully automated symbol encoding/decoding, and generation and validation of packet framing; ability to report framing errors to user Automatic scrambling can be turned off Configurable, automatic link initialization and training: <ul style="list-style-type: none"> • Automatic Lane Polarity Detection (RX), separate for each lane • Programmable Lane Polarity Inversion (TX), separate for each lane • Automatic link width negotiation; all link widths x1, x2, x4, and x8 supported; user can configure which widths will be negotiated during link training • Programmable Lane Reversal (TX+RX) • Programmable Lane Skew: (± 7 symbols, resolution: 1 symbol time) Link Training and Status State Machine: Full support for states Detect Configuration, Recovery, and L0, L1 Link states can be forced for testing purposes Programmable skip rate
Transaction layer features	Send and receive any single ASI packet User software can define arbitrary sequences of packets for sending Receive packets can be stored into HW receive buffer or algorithmically checked and discarded 6 hardware channels that map to any virtual channel (BVC, OVC, MVC) for sending and receiving packets <ul style="list-style-type: none"> • Full support for 20 virtual channels (VCs) during link training • Pattern matcher supporting trigger out, performance counter and conditional start • Conditional start on RX pattern matcher, external trigger in/out or through API or other TX HW channels • Generation and receiving of packets at maximum band width (stress testing) • Real time data compare of incoming data against algorithmically generated data • Infinite loop
Error generation and analysis features	Error insertion capabilities on the physical layer, data link layer and transaction layer Physical layer: <ul style="list-style-type: none"> • Transmitter polarity inversion • Transmitter lane reversal • Deterministic lane skew up to 7 symbols • Link width and lane sequence negotiation emulation x1, x2, x4 or x8 device • Sending packet with incorrect "running disparity" • Count 8b/10b coding errors, per lane Data link layer: <ul style="list-style-type: none"> • Programmatically answer NAK instead of ACK • Send packets with incorrect LCRC and DLLPs with incorrect CRCs Transaction layer: <ul style="list-style-type: none"> • Arbitrary header field contents (this allows you to send illegally formed packets) • The transmitter ignores flow control credits
Configuration space features	User can define Config space of all emulated devices (useful default configurations are available)
PI emulation	Topology emulation support PIO:0 packets. All other PI specific handling of packets can be done in user software
Power management	Meets "ASI Core Architecture Specification, Revision 1.0" Encapsulated PCIe Base PM capabilities as described in the PI-8 specification is not supported
External trigger in/out	For cross triggering, event triggering and triggering another device/instrument
Fabric Manager	Software-emulated Owner Election State Machine Software-emulated Owner Election Status Update State Machine Assignment of maximum packet size values for the fabric Brings all links in active state
Pattern matcher	4 pattern matchers available and each compares 8 dwords, starting at the ASI route header. Decide whether incoming packets are sent to the receive buffer for software handling or sent to the algorithmic payload check in hardware or discarded. The same set of pattern matchers is also used as a delay or repeat condition in the transmit memory.

Flexible exerciser use models help you characterize and test your design under real conditions

Verification of the data link layer involves packet-level testing of individual requests and responses and packet sequence numbering. The main layer tested with the exerciser is the transaction layer. It tests and generates transaction layer packets and allows for emulation of a real, operational device.

Functional mode

In functional mode all incoming and outgoing packets are handled by software. This gives the tester maximum flexibility. The exerciser can emulate a topology and generate PI specific response.

Performance mode

In performance mode the maximum packet throughput is much higher. The exerciser can transmit packets at full line rate (Flow Control credits permitting). On the receive side, the exerciser can handle incoming packets at line rate. Performance tests follow the setup/execute/verify paradigm. The user programs vectors (packets) during the setup phase. In general, PI specific responses and topology emulation are not available in performance mode. It is still possible to handle selected incoming packets in software. However, this reduces the packet throughput.

Topology emulation

In addition, the exerciser supports tunneling with flexible packet generation/receiving, including all possible PIs. Topology emulation is a function, which emulates a virtual fabric behind the exerciser's physical port. It is used to test fabric management software with corner case scenarios, simulate fabric topology changes, simulate hot plug, link up/down situations and proper event handling in the device under test.

Virtual channels

The exerciser can show up to 20 virtual channels (VCs) during link training, and it supports all legal combinations of OVCs, BVCs and MVCs. With these capabilities, you can exercise VC negotiation and FC initialization with different settings. VC negotiation and FC initialization are implemented according to the Advanced Switching Core Architecture Specification. The exerciser has hardware resources for up to 6 VCs. It can be mapped to all 20 VCs and can send TLPs on up to 6 VCs, to give you the flexibility you need.

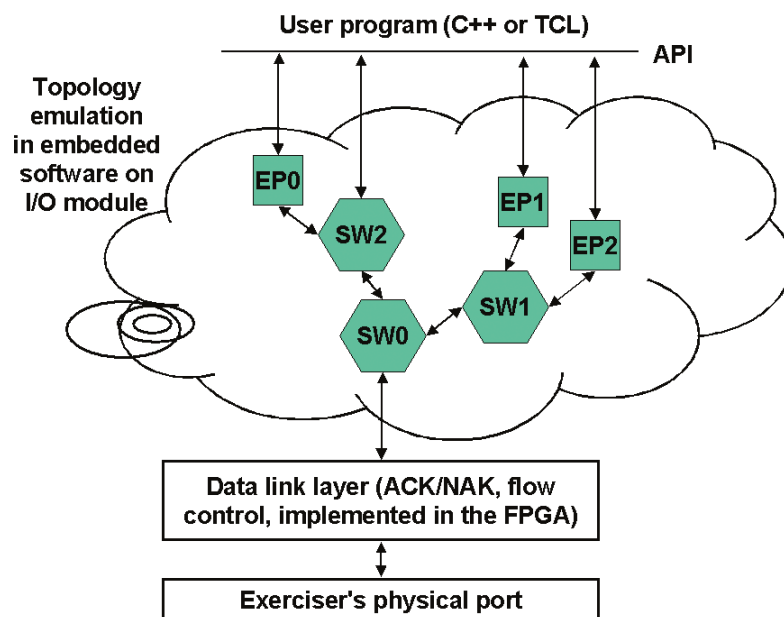


Figure 4. Block diagram of the topology emulation

E2980A protocol analyzer for ASI gives you fast access to understandable data

The E2980A protocol analyzer for ASI captures the traffic or transactions on a ASI link and allows you to analyze it and troubleshoot problems to find the root cause. The protocol analyzer provides non-intrusive monitoring of traffic between two ASI end nodes (either a system talking to an ASI card or the exerciser talking to an add-in card or system). With its capabilities in analyzing generated ASI traffic, the

analyzer is perfectly suited for turn-on and debug of ASI systems and designs. It captures and analyzes data-link-layer and transaction-layer packets as well as training sequences and ordered sets.

An easy-to-use GUI offers graphical trigger setup, search and filter capabilities to help you intuitively interpret ASI transactions.

Powerful triggering, easy setup

The protocol analyzer's sophisticated trigger capabilities are based on a trigger sequencer. It offers an easy-to-use set up and graphical representation of the trigger sequence. Examples and listed predefined conditions reduce time-consuming trigger set-ups. You can define up to 8 states, 8 patterns and 2 counters with various actions store, increment counter, trigger out and so on.

Define the trigger and sequences in the main window pane

Get a clear overview of complex trigger set-ups. The sequencer overview pane graphically displays the trigger setup with defined states, conditions and actions.

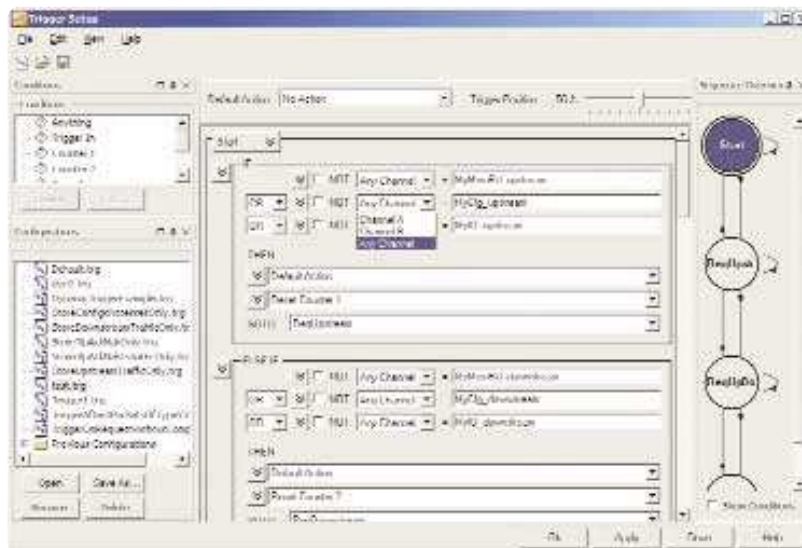


Figure 5.

The condition window offers a list of pre-defined trigger conditions Just "drag and drop" to create your own trigger configurations. You also can create customized conditions.

Create customized configurations using the "drag and drop" list in the configuration window. All customized configurations can be saved.

Protocol analyzer capabilities and benefits

All-in-one window gives you easy visibility into ASI transactions

- Traffic activity, port link status, and trace content are simultaneously displayed
- Sophisticated, fast screen-based traffic upload

Tabular traffic display speeds your debug process

- Traffic representations and protocol decoding enable fast debug, detailed root-cause analysis and device-performance analysis – Skip ordered sets, training sequences, all DLLPs and TLPs visualizing all PIs (decodes PI0, PI1, PI2, PI4, PI5, PI97)
- Avoid constant scrolling with the tabular display that maximizes information density on the screen
- See packet details by zooming on multiple lines
- Easily retrieve information with embedded markers
- Quickly find problems with automatic error detection

Multiport display for better insight into your system

- Packets captured from multiple ports are displayed with common time stamps and common markers
- Multiple analyzers can share events for sophisticated cross triggering

Quickly find and examine sequences of interest

- Powerful search, filter and error detection functionality

Customize your measurements with test automation and scripting capabilities

- TCL script capabilities for test automation and customized test development

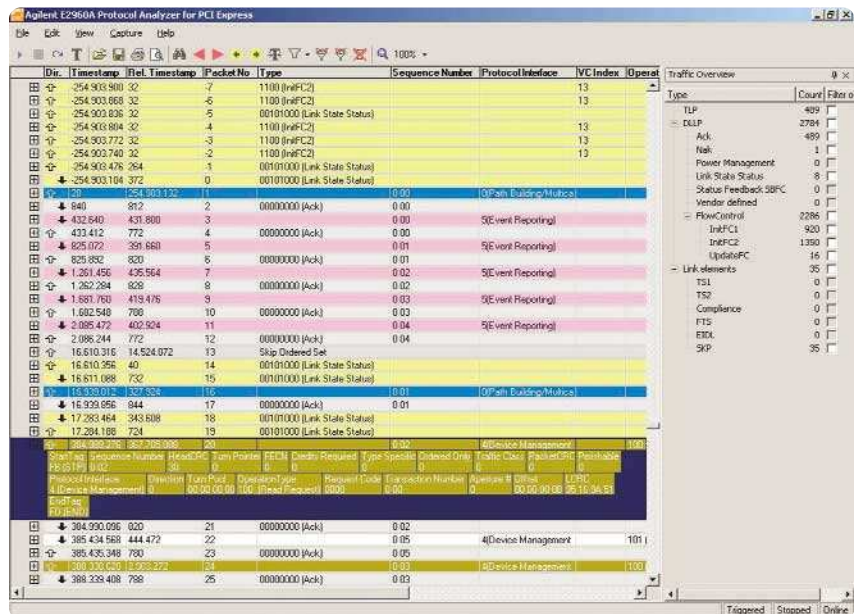


Figure 6. Protocol analyzer graphical user interface

Technical specifications for the protocol analyzer

E2980A analyzer features

Display features	Separate, cross-correlated packet view Customizable view of captured packets Traffic overview (post capture) Hex display Expand and collapse packets in order to obtain more information Context-sensitive field decoding Easy navigation within captured trace Tool tips for each field provide more information as needed Packets with errors are highlighted Tabular view with configurable columns Color-coded transaction types allow easy recognition of various types of traffic Markers Interleaved display, including time-stamps
Trigger features	Graphical trigger setup Trigger sequencer with up to: <ul style="list-style-type: none">• 8 states• 2 counters/timers• 8 pattern terms• External trigger in and out• Protocol error trigger (disparity error invalid 10b symbols) Multi-way branching Filtering (real time): <ul style="list-style-type: none">• Idles• On a per-packet basis controlled by the trigger sequencer Filter conditions can be defined individually for each trigger sequencer state Trigger on payload (first 3 or 4 dwords)
Traffic capture features	Supports capturing in x1, x2, x4, x8 link width with 2.5 Gbps Non-intrusive traffic capturing via the passive ATCA and passive PCI Express interposer probe as well as the midbus probe Captures training sequences, ordered sets, data-link-layer packets and transaction-layer packets in both directions simultaneously Supports data rates of 1.25 - 2.5 GT/s
Error detection	Disparity errors, TLP/DLLP LCRC, EBD, framing, idle data and invalid 10b symbols in hardware
Other features	Analyzer to exerciser traffic record and replay Example traces + triggers settings + programming examples Timestamps with 8 ns resolution (absolute, relative, idle time, packet duration) Automatic lane polarity detection 1 GB trace memory Real-time statistics counters Latency measurements (using markers) External trigger in/out

Use the best possible test setup connection for a fast turn-on

The card use model

The device under test is either a PCI Express form factor card or an ATCA form factor card working in ASI mode. This card is plugged into the top of the analyzer probe board. The analyzer probe board is plugged into the top of the exerciser probe board for PCI Express applications or into the ATCA backplane. The exerciser emulates an ASI device, which is communicating with the device under test and the analyzer in between displays the communication.

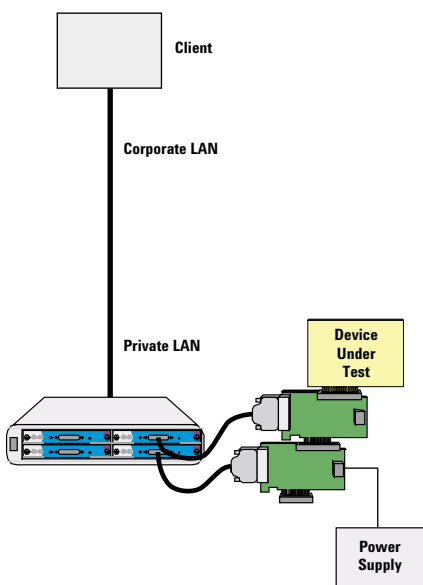


Figure 7. Testing an add-in card together with analyzer

The system test use model

The system under test has a PCI Express form factor slot to plug into and works in ASI mode. In this case the protocol analyzer probe board is inserted between the system and the protocol exerciser probe board. The protocol analyzer captures the traffic generated and sent by the protocol exerciser to the system under test. The fully controllable protocol exerciser generates various transactions including error conditions to the system. Additionally the protocol exerciser reacts as an ASI device in order to respond to the system.

The protocol analyzer captures the transactions and displays the behavior of the protocol exerciser and system communicating with each other. You can stress the system and perform worst-case-scenario tests with the protocol exerciser being used to help troubleshoot potential problems with the protocol analyzer.

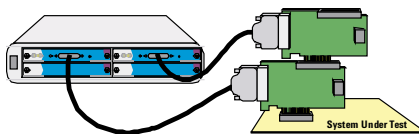


Figure 8. Protocol analyzer use model with exerciser

The chip-to-chip test use model

With the E2941A-ASI soft touch midbus probe, you can connect the protocol analyzer to a device under test without an available slot. The midbus probe can be connected to the standard footprint integrated on the individual device under test. It can be used to analyze links on a board from one chip to the other. The footprint must be implemented in the design phase of the board.

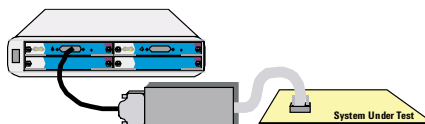


Figure 9. Protocol analyzer use model with soft touch midbus probe

Use the best possible test setup connection for a fast turn-on (continued)

ATCA backplane use model

The Agilent E2943A active probe board is the key probing solution for the exerciser to be plugged into the ATCA backplane to emulate real ASI designs or topologies. The active probe board also offers analyzer and exerciser support for the new Advanced Mezzanine Cards (AMC) standard. With the active probe the exerciser can communicate with other cards in the backplane fabric by acting as a real ASI design. The Agilent

E2944A passive probe board enables non-intrusive capturing of ASI transactions between two line cards in the ATCA-based backplane. The DUT is plugged into the top of the passive ATCA probe fixed with a special mechanical card test extender. Alternatively, the exerciser can be used to emulate one of the line cards of the test setup. In this case the active exerciser probe is plugged into one of the other available slots of the backplane.

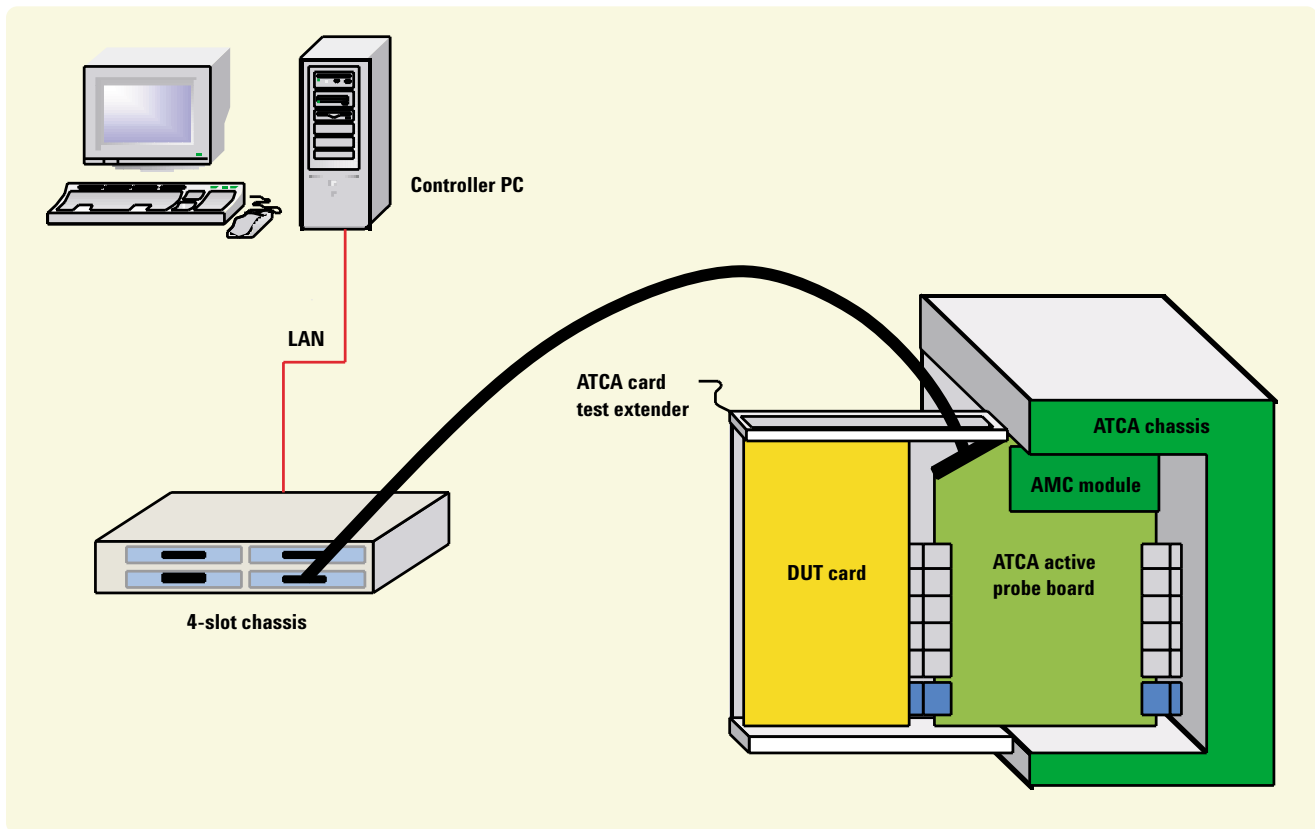


Figure 10. Test setup with ATCA probe

Flexible probing alternatives solve possible connection issues

Active and passive ATCA interposer probe boards

There are two types of ATCA probe boards available. The E2944A passive probe board is for non-intrusive capturing of ASI transactions with the protocol analyzer. The E2944A connects to the platform via a midbus connection and the included E2941A-ASI midbus probe to the E2980A platform. The E2943A active probe board is used for the exerciser to emulate any real ASI device. The active probe board can also be used for the analyzer setup. Furthermore, the E2943A allows you to test the Advanced Mezzanine Cards (AMC) standard with a connector to plug in any AMC form factor card. The E2943A is connected to the platform with the standard I/O cable.

PCI Express Slot interposer probe boards for passive and active probing

Two types of probe boards are available for the E2980A. The passive probe boards allow non-intrusive probing for the protocol analyzer. The active probe boards are intended for the exerciser; they give you the flexibility to send PCI Express packets upstream to a system under test or downstream to an add-in card under test and receive packets back. Each probe board can accept a PCI Express x1, x4, x8 or x16 add-in card, which is inserted into the x16

connector on the top of the probe board. This will operate up to ASI x8 for the x8 probe card. The boards are standard size short PCI cards.

One probe board is required per I/O module, except when using the E2942A single probe Y-cable.

E2942A single probe Y-cable where space is limited

This cable allows the use of one active probe board for both exerciser and analyzer simultaneously (using two I/O modules).

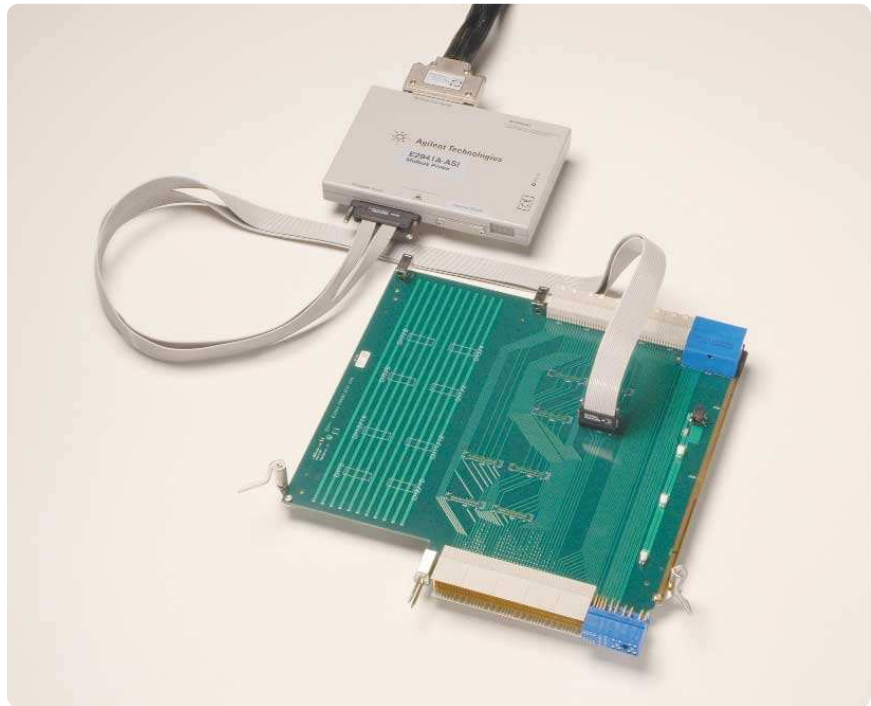


Figure 11. ATCA passive interposer probe board via midbus probe

Flexible probing alternatives solve possible connection issues (continued)

Connect directly to your circuit with the soft touch midbus probe

Now you can simplify the debug and turn on of high-speed digital designs that are tight on space or that require minimal disruption of signal routing. The E2941A and the E2941A-ASI soft touch midbus probes increases the flexibility of the protocol analyzer by enabling a direct connection to the circuit board using a standard midbus footprint. With the E2941A and E2941A-ASI soft touch midbus probe, you can analyze high-speed ASI and PCI Express chip-to-chip communications without interfering with the signals. The soft touch probe uses micro spring-pin technology to provide a reliable connection to the signal pads without the need for special cleaning or special surface finishes. The E2941A is the midbus probe for PCI Express applications supporting Spread Spectrum Clocking (SSC) with the external reference clock. The E2941A-ASI is the special ASI version also included in the E2944A passive ATCA probe. This version does not offer the external clock and SSC support, which is not required for ASI.

Footprint design integration information for the midbus probe can be found in the ASI Logic Analyzer Probing Design Guide (publication number 5989-1172EN) at:
www.agilent.com/find/E2960_series

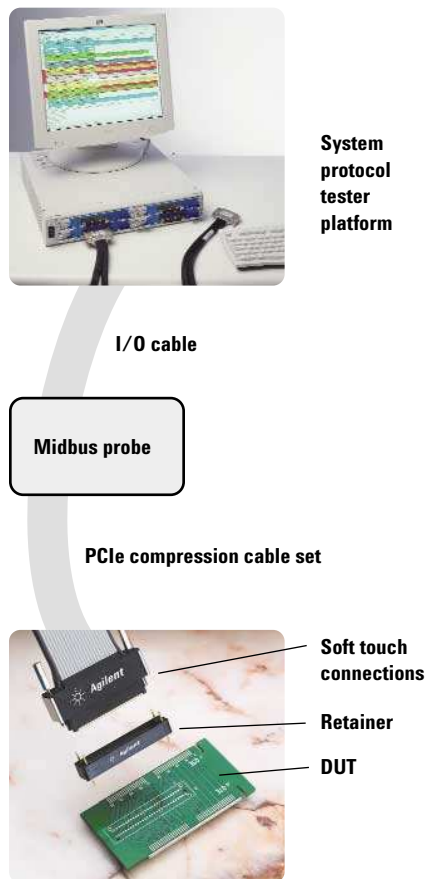


Figure 12. Soft touch midbus probe

Key features of the soft touch midbus probe

- Supports ASI x1, x2, x4, x8
- Agilent soft touch technology
- No slot connector required
- Reduced electrical load
- Eases routing of board traces
- Easy to use – can be tightened manually
- Very reliable probing
- Passive probing runs cool
- Adjusts to uneven board surfaces

General technical specifications

System requirements

Hardware	Pentium® processor 1 GHz or equivalent 512 MB available RAM 8 x CD-ROM driver or higher VGA resolution 1024 x 768
Operating system	Windows® 2000 or Windows XP

General characteristics

Power requirements	100 - 120 V _{ac} 200 - 250 V _{ac} 550 VA max 47 to 63 Hz
Memory	Analyzer: 1 GB trace memory Exerciser: 2 MB packet memory
Display	4-character LED display on the I/O module and probe board for status information

Environment

Temperature (AT-ETM757)	Operating: 0 °C to + 55 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15% - 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

Physical characteristics

2-slot chassis	Width: 30 cm (11.81 in); Depth: 49.0 cm (19.29 in); Height: 11 cm (4.33 in) Weight (empty): 5.1 kg (112 lbs)
4-slot chassis	Width: 45.4 cm (17.87 in) Mounts in EIA-standard 48.3 cm (19 in) rack; Depth: 49.0 cm (19.29 in) Height: 2U - 8.89 cm (3.5 in) Weight (empty): 5.1 kg (112 lbs)
Probe cable	Length: 1.5 m (59.06 in)
Single probe Y-cable	Length of black segment: 1.5 m (59.06 in) probe board to analyzer Length of white segment: 0.5 m (19.69) analyzer to exerciser

Connectors

MDI	RJ-45; 100 Mb/s Ethernet (to PC controller)
MDI-X	RJ-45; 100 Mb/s Ethernet (to next chassis)
External clock in/out	SMA connector on probe board
AT hard drive power	Connector on probe board (uses 12 V only)
External trigger in	Female BNC; Trigger input from external device
External trigger out	Female BNC; Trigger output from external device

General technical specifications (continued)

Midbus probe

Electrical specifications			
Absolute maximum ratings	Amplitude data signal: $2 V_{ppdiff}$	Amplitude ref. CLK: $5 V_{ppdiff}$	
Operating conditions			
Data signals	Amplitude (at eye width of 0.85 UI)	Min: $450 mV_{ppdiff}$	Max: $1600 mV_{ppdiff}$
	Frequency: Internal CLK mode	Min: $2.5 GHz - 50 ppm$	Max: $2.5 GHz + 50 ppm$
	External CLK mode	Min: $2.5 GHz - 300 ppm$	Max: $2.5 GHz + 300 ppm$
Ref. CLK	Amplitude	Min: $800 mV_{ppdiff}$	Max: $2000 mV_{ppdiff}$
	DC offset	Min: $0 mV$	Max: $500 mV$
	Frequency: Internal CLK mode	Min: $100 MHz - 50 ppm$	Max: $100 MHz + 50 ppm$
	External CLK mode	Min: $100 MHz - 300 ppm$	Max: $100 MHz + 300 ppm$
Environment	Operating temperature: $+5^{\circ}C$ to $+55^{\circ}C$		Storage temperature: $-40^{\circ}C$ to $+70^{\circ}C$
Physical characteristics	Width: 19.70 cm (7.76 in); Depth: 14.50 cm (5.70 in); Height: 2.80 cm (1.10 in); Weight: 0.75 kg / 1.65 lbs		

All specifications are valid for room temperature. Footprint design integration information for the midbus probe can be found in the ASI Logic Analyzer Probing Design Guide (Publication # 5989-1172EN) at: www.agilent.com/find/E2960_series

Sot/interposer probe board¹

Active probe board for PCI Express electrical specifications			
Transmitter path	Eye opening amplitude ²	$550 mV_{ppdiff}$	
	Transition bit emphasis	2.8 dB	
	Emphasis time	1.1 ns	
	Eye opening time	290 ps ³	
Receiver path	Eye opening amplitude	Min: $220 mV_{ppdiff}$ (from PCIe spec)	Max: $1200 mV_{ppdiff}$ (from PCIe spec)
	Eye opening time	260 ps (measured on one lane)	
	Frequency	$2.5 Gb/s \pm 50 ppm^4$	$2.5 Gb/s \pm 300 ppm^5$
Passive probe board for PCI Express electrical specifications			
Absolute maximum ratings	Amplitude data signal	2 ppdiff	
	Amplitude ref CLK	2.5 ppdiff	
Recommended operating conditions	Data signals		
	Amplitude	Min: $175 mV_{ppdiff}$	Max: $1600 mV_{ppdiff}$
	Eye width	Min: $250 ps^6$	Max: 400 ps
	Frequency	$2.5 Gb/s \pm 50 ppm^4$	$2.5 Gb/s \pm 300 ppm^5$
	System startup lock time	Typ. 400 μs (in normal operation mode) Typ. 3 μs (in fast sync operation mode ⁷)	
Ref. CLK	Amplitude	Min: 800 ppdiff	Max: 2000 ppdiff
	DC offset	Min: 0 mV	Max: 500 mV
	Frequency	$100 MHz \pm 50 ppm^4$	$100 MHz \pm 300 ppm^5$
Active/passive probe board for PCI Express physical characteristics	Size: Standard half-length cards, as defined by the ASI Electrical Mechanical Specification 1.0A Length: 17.3 cm (6.81 in) including I/O connector Height: 12.6 cm (4.96 in) including metal bracket; 11.1 cm (4.37 in) excluding metal bracket		
Device under test (DUT) position	Horizontal setback 2.7 cm (1.06 in); Elevated vertically 12.5 cm (4.92 in)		

¹ Specifications are valid at room temperature

² Measured using PRBS2⁵⁻¹ pattern

³ When signals come from I/O module

⁴ When I/O module is operated in internal CLK mode

⁵ When I/O module is operated in external CLK mode

⁶ Not for fast sync mode

⁷ Fast sync capture mode: This mode is optimized to analyze around power-up, link-training or L0s states, where faster analyzer reaction times are needed and you are less concerned about signal integrity. The analyzer will take less time to resume capturing after break of electrical idle, but you will probably record false errors.

General technical specifications (continued)

Electrical specification of E2943A ATCA active probe

Transmitter path (channels 1-4, 14, 15)	TYP
Eye opening amplitude ¹	460 mV _{ppdiff}
Transition bit emphasis	2.9 dB
Emphasis time	1.1 ns
Eye opening time	>250 ps ²

1 Measured using PRBS2⁵⁻¹ pattern

2 Measured with diff. scope probe at connector when signal comes from IO-module

Receiver path(channels 1-4, 14, 15)	Min	Max
Eye opening amplitude	220 mV _{ppdiff} (from PCIe spec)	1200 mV _{ppdiff} (from PCIe spec)
Eye opening time	240 ps (measured on one lane)	
Frequency	2.5 Gb/s ± 50 ppm ³ 2.5 Gb/s ± 300 ppm ⁴	2.5 Gb/s ± 50 ppm ³ 2.5 Gb/s ± 300 ppm ⁴

3 When IO-module is operated in internal CLK mode

4 When IO-module is operated in external CLK mode

Pass-through channels (5-13)	TYP
<attenuation>	6 dB

Specifications are valid at room temperature

How to configure a system

1. Choose the application:

- Protocol exerciser E2980A-E08
- Protocol analyzer E2980A-A08
- Protocol analyzer and protocol exerciser with two I/O modules to use in parallel in the same application E2980A-B08
- Validation station fully populated with protocol exerciser modules used for validation purposes like stress testing (E2980A-V02 two exercisers in the 2-slot chassis)

2. Decide whether you need a 2-slot chassis or a 4-slot chassis. Chose the 4-slot chassis if you plan to depends if you want to extend the platform later

3. Decide which type of probing you need within the E2980AU (ATCA, PCI Express interposer or midbus probing. This must be added to the pre-defined E2980A configuration.

Each corresponding E2980A configuration (E2980A-A08, E2980A-E08, E2980A-B08 and E2980A-V02) includes the following as minimum:

- One 2- or 4-slot chassis (selectable)
- One serial I/O module
- Analyzer Software Package or Exerciser Software Package

Optional accessories:

E2941A and E2941A-ASI soft touch midbus probe for the protocol analyzer (N4221A PCIe compression cable set is required to complete the E2941A or E2941A-ASI). The complete soft touch midbus probe solution contains of the amplifier box, five standard retainers, the N4221A PCI Express compression cable set (needs to be ordered separate) and a reference clock cable (for the E2941A only). If you use this you don't need an interposer probe to complete the configuration.

E2942A single probe Y-cable (included in E2980A-B08).

A protocol analyzer/exerciser with one I/O module can be used interchangeably for analyzing or exercising your device. It is not possible to run the protocol analyzer and the protocol exerciser simultaneously on one module. A protocol analyzer/exerciser with two I/O modules can be used simultaneously as an analyzer and exerciser and includes a single probe Y-cable.

The E2980AU for upgrade and extensions show the required probing solutions (required to be added to the configuration separately), the additional hardware and software available to adapt your solution to changing requirements at a later date.

Typical pre-defined configuration e.g. E2980A-B08:

1 x E2960A-FR2	2-slot chassis
2 x N5305A	Serial I/O module with cable
1 x E2962A	Analyzer Software Package for PCIe x8
1 x E2964A	Exerciser Software Package for PCIe x8
1x E2942A	Single probe Y-cable
1 x E2981A	Analyzer Software Package for ASI x1, x2, x4 and x8
1 x E2982A	Exerciser Software Package for ASI x1, x2, x4 and x8

Probing needs to be selected within the E2980AU separately.

Ordering information

Complete configurations

Protocol analyzer for ASI x1, x2, x4 and x8	E2980A-A08
Protocol exerciser for ASI x1, x2, x4 and x8	E2980A-E08
Analyzer/exerciser bundle for ASI x1, x2, x4 and x8	E2980A-B08
Exerciser validation station for ASI x1, x2, x4 and x8	E2980A-V02

Upgrades/extensions

Protocol analyzer software package for ASI x1, x2, x4 and x8	E2981A
Protocol exerciser software package for ASI x1, x2, x4 and x8	E2982A
Active probe board for PCI Express x1	E2938A
Active probe board for PCI Express x4	E2939A
Active probe board for PCI Express x8	E2968A
Passive probe board for PCI Express x1	E2945A
Passive probe board for PCI Express x4	E2946A
Passive probe board for PCI Express x8	E2947A
Single probe Y-Cable	E2942A
Soft touch midbus probe+ PCIe compression cable set	E2941A + N4221A
ATCA active interposer probe board with AdvancedMC	E2943A
ATCA passive interposer probe board via midbus probe (includes E2941A-ASI midbus probe; N4221A is an additional requirement)	E2944A + N4221A
Soft Touch midbus probe for ASI (internal clock only - no SSC; N4221A is an additional requirement)	E2941A-ASI + N4221A

Agilent offers a variety of service options to support you in getting the most from your E2980A analyzer/exerciser

Start-up assistance

Recommended for new users of the E2980A. This service focuses on speeding your time to measurement in your environment. You will learn to navigate the capabilities of the E2980A and focus on applying the measurements you need to make for your application.

Productivity assistance

Aimed at experienced users who may have a unique problem they are trying to solve and are

looking for ways to enhance the use of the product. Examples of productivity assistance might include automating the test suite, avoiding common measurement errors and improving accuracy or understanding and analyzing a measurement with your device.

Training and education

Agilent offers several classes related to the exerciser/analyzer.

Warranty options

All models include a standard 1-year warranty. Contact your local sales office for prices of extended options:

Option number	Description
	3-years of return-to-Agilent
	5-years of return-to-Agilent

Related Literature

Publication Title	Publication Type	Publication Number
<i>Serial Protocol Tester</i>	Brochure	5989-2526EN

Product Web site

For the most up-to-date and complete application and product information, please visit our product Web site at:

www.agilent.com/find/ASI

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