

Agilent Technologies System Protocol Tester E2960A Protocol Exerciser and Analyzer for PCI Express®

Data Sheet



- Faster, easier and more effective PCI Express® turn-on, debug, validation and compliance testing
- Combined traffic generation and protocol analysis dramatically increase your test coverage to reduce the risk of costly redesigns and recalls
- Universal hardware platform reduces expenditures for test equipment – use it for PCI Express today; upgrade to cover selected future serial protocols up to 3.125 Gbps



Agilent Technologies

E2960A protocol exerciser and analyzer for PCI Express offers the features and capabilities you need to test your PCI Express design quickly, easily and thoroughly

Applications

- Turn-on and debug of PCI Express systems, add-in cards, motherboards, software, drivers and BIOS
- Validate PCI Express chipsets and systems – stress testing, worst-case-scenario testing, and error-behavior testing
- PCI Express compliance testing

Key features

- True bidirectional analyzer/exerciser for PCI Express x1, x2, x4 and x8
- Use the exerciser/protocol analyzer capabilities in combination to analyze root causes of problems with ease
- For easier validation, capture traffic conditions, then drag and drop to reproduce system problems
- Multiport testing allows you to stress all slots with the same load conditions and synchronize the tests
- External trigger in/out to synchronize with other devices
- Connect to your device with a non-intrusive passive or active slot/interposer probe or a soft touch midbus probe
- Multiprotocol test/cross bus analysis for semiconductors, cards and systems – simultaneously record PCI Express, Fibre Channel and Advanced Switching Interconnect traffic and transactions and time-correlate them within the same test setup and graphical user interface
- Intuitive GUI lets you view and set up tests with ease
- LAN interface enables remote control and resource sharing
- FPGA-based tool permits easy upgrades
- Flexible and extendable platform protects your hardware investment

Protocol exerciser: stress your system to the max in the shortest period of time

- Generates and responds to arbitrary bus traffic
- Generates and responds to PCI Express packets and packet sequences
- GUI, DCOM application programming interface, TCL interfaces and in-system port control
- Protocol checker with 23 preprogrammed protocol rules
- Error insertion lets you test corner cases and failure behavior
- Simulate or emulate an PCI Express end node
- 2 MB data memory to emulate any real PCI Express end node or device

Protocol analyzer: turn on and debug PCI Express designs faster and more easily

- Root cause and performance analysis
- API and GUI with graphical trigger setup, search and filter capabilities
- Sophisticated trigger capability with patented dynamic triggering and storage qualifications
- Automatic error detection
- 1 GB trace memory
- Traffic overview
- Packet decode view
- Performance counters

An intuitive tool for every stage of PCI Express development

The E2960A protocol analyzer and exerciser makes it easier than ever before to turn on, debug and validate your PCI Express systems and devices and allows you to check them for compliance.

To thoroughly test your PCI Express systems and devices, you may need to create system conditions that are difficult to reproduce with existing PCI Express equipment. The E2960A protocol exerciser and analyzer lets you quickly and easily simulate traffic or capture traffic conditions and recreate them. The protocol exerciser lets you stress all data paths in a system and test corner cases and behavior by inserting errors and protocol violations on each layer (physical, data link and transactional).

The protocol analyzer, including Agilent's patented dynamic trigger conditions, is the core debug and turn-on test tool for root cause analysis, troubleshooting and performance analysis. It provides non-intrusive monitoring of PCI Express traffic between an add-in card and a system or between a protocol exerciser and a system.

Versatile system architecture

To reduce your expenditures for test equipment, the E2960A uses the same hardware whether you are using it as an exerciser or an analyzer or a combination of the two. To further protect your hardware investment, the scalable System Protocol Tester platform allows you to expand your test capabilities and upgrade as your needs change and as serial protocols evolve.

Platform features and benefits

- Universal and flexible hardware – use it for PCI Express, Fibre Channel (with a separate plug-in module) and Advanced Switching Interconnect today, then upgrade to cover selected future serial protocols
- Multiprotocol test/cross bus analysis for semiconductors, cards and systems – simultaneously record PCI Express, Fibre Channel and Advanced Switching Interconnect traffic and transactions and time-correlate them
- Familiar and consistent set up for future protocols shortens your learning curve
- Easy to upgrade and interchange software and hardware elements (for example, front-end probes and plug-in modules)

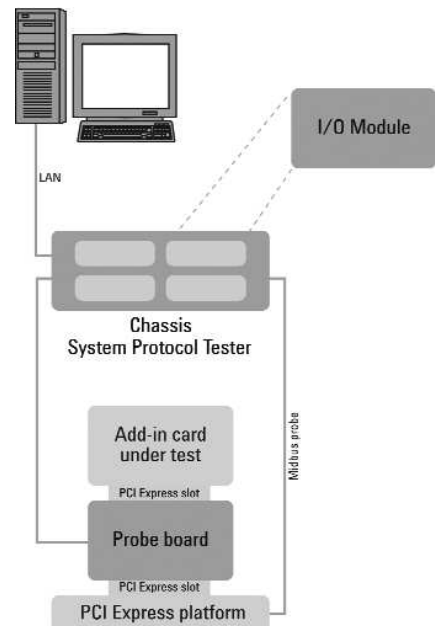


Figure 1. Insert the probe board into your computer's PCI Express slot, attach your PCI Express device to the card, and connect the card to the protocol analyzer chassis to monitor and analyze packets traveling over the link.

E2960A platform components



Figure 2.

- ① Chassis (2 slot or 4 slot)
- ② I/O module
- ③ Slot/interposer probe board
- ④ Protocol analyzer/exerciser software
- ⑤ E2969A protocol test card (must be ordered separately)
- ⑥ LAN interface
- ⑦ PC for local control of the system (not included)

Choose a 2-slot or 4-slot chassis

You can monitor/test from one to four PCI Express links with the 2- and 4-slot chassis. The 2-slot chassis accommodates up to two serial I/O modules, and you can use it in either a vertical or horizontal orientation. This lightweight chassis has a built-in handle and soft carry bag with room for accessories. Use it for testing in scenarios where portability and small size are important.

The 4-slot chassis houses up to four serial I/O modules. Use it on your bench top or mount it in a rack. It is ideal for validation applications where you need multiple exercisers to stress and load system slots. You can connect multiple chassis and control/synchronize them from a single host.

Upgradeable serial I/O module

The versatile serial I/O module provides the intelligence to handle specific protocols. Its FPGA-based design allows you to upgrade it as needed and to use it as either a

protocol exerciser or analyzer. Every serial I/O module has a LAN interface that is connected to an Ethernet hub inside the chassis. A custom cable connects the module to a probe board. An LED display shows status information and diagnostic messages.

Flexible connectivity: slot/interposer probe board or midbus probe

A slot/interposer probe board provides the interface to your device under test (connected via a cable from the I/O module). A midbus probe is also available for the protocol analyzer. There are three passive and active slot/interposer probe boards available for the three different PCI Express link widths (x1, x4 and x8). Go to page 14 to learn more.

Easy-to-use software

Use the intuitive E2960A analyzer and exerciser software packages to set up basic PCI Express packet tests quickly and easily. The various software packages enable you to access different link widths. Each option is backwardly

compatible – the x8 software package also covers x4, x2 and x1. You can use the software in off-line mode to view captured traffic. To download the latest version, go to www.agilent.com/find/E2960_series

Protocol test card

Accelerate your time to market with the E2969A protocol test card for automated compliance testing. It offers two kinds of connections (Agilent connector or midbus footprint) that allow you to use it with the analyzer so you can debug and trace problems to their root cause. Use the preprogrammed tests to speed your compliance testing. Connect the E2969A PTC to the protocol analyzer and troubleshoot potential out-of-compliance behavior. Learn more about the E2969A at www.agilent.com/find/E2969A_PTC

Controller

The chassis is connected via LAN to a controller PC that manages the behavior of the System Protocol Tester platform. The software runs on a remote client or on the controller PC itself.

E2960A protocol exerciser for PCI Express lets you test and validate your system's performance under varied conditions

With its fully adjustable parameters, the E2960A protocol exerciser lets you simulate or generate and respond to any PCI Express traffic or transactions. It is an intelligent I/O communication tool that can react as a PCI Express end node or device. The E2960A exerciser's functionality extends far beyond the capabilities of a simple packet generator. It is tailored to validate corner cases and emulate stress conditions for components on system boards and add-in cards. The protocol exerciser is the ideal tool to test and validate x1, x2, x4 or x8 PCI Express designs.

Perform worst-case-scenario tests

The E2960A exerciser lets you stress all data paths and test corner cases in your system so you can force it to fail. You can also insert errors and test the behavior of designs in response to these errors to enable worst-case-scenario testing.

Flexible control

To set up basic PCI Express packets quickly and easily, use the intuitive E2960A exerciser graphical user interface (GUI). The GUI offers a menu display of the exerciser's capabilities, and allows you to select an experience level that limits the number of capabilities displayed. The GUI further increases flexibility by allowing you to set up single packets or sequences or blocks of packets, I/O memory reads and writes, configuration reads and writes and any type of message.

The exerciser can receive and react programmatically on incoming requests. You can easily program the configuration space with the GUI, and you can view the six programmable memory or I/O decoders.

For more comprehensive automated tests, you can control the exerciser via a DCOM or TCL programming interface. For example, you can validate designs by repeatedly stressing all data paths of a system simultaneously. The host software running on the system controller provides the protocol exerciser API, which allows it to be controlled programmatically. The protocol exerciser API allows you to access all functions of the protocol exerciser via DCOM programming or TCL script. The API is implemented into the system as a DCOM interface, which can be shared between multiple applications.

In addition, you can control the exerciser through the PCI Express port of the system under test. The protocol exerciser also has fully configurable PCI Express configuration space. Furthermore, the exerciser comes with a fully functioning 2 MB data memory, which allows the exerciser to emulate any real PCI Express device/end node. This means the exerciser is able to do write/read compare, memory read and write, etc. as with a real PCI Express device.

Use the E2960A protocol exerciser to:

- **Effective turn-on and debug PCI Express systems** – Easily simulate the transaction layer and test the data link layer capabilities of a PCI Express device
- **Validate PCI Express chipsets and systems** – Ensure the interoperability and stability of all data paths and get the largest possible test coverage with links to root cause analysis of problems
- **Check your system for compliance**

Protocol exerciser capabilities and benefits

Perform realistic tests with device emulation

- Simulate various test scenarios by setting exerciser parameters the way you want
- Minimize the number of real devices needed to create a large-scale test environment
- Full functioning 2 MB data memory allows you to emulate and simulate any real PCI Express device/end node
- Easily record packets from the protocol analyzer and replay with the exerciser as many times as you want. Use drag and drop or copy and paste functionality or export files from the protocol analyzer.
- Use external trigger in/out for cross triggering, event triggering and triggering another device/instrument for more thorough troubleshooting
- Real-time data compare feature allows you to check the integrity of your data to give you more confidence in your results

Increase test coverage with configurable traffic generation

- Transmit and receive PCI Express traffic at full bandwidth of x1, x2, x4 and x8 link widths with 2.5 Gbps
- Customize the traffic you send: Generate real-world requests with parameters and behaviors you define

- Validate the boundary conditions of your system
- Generate any combination of PCI Express packets for multiple ports and correlate the test results across time for comprehensive system testing
- Algorithmic data generation/checking feature allows you to compare incoming packet payload against algorithmically generated reference data
- Fully configurable configuration space, including PCI Express extended capabilities

Real-time statistics help you see immediate changes in your system's performance

- Real-time performance counters

Customize your measurements with test automation and scripting capabilities

- Control software via the easy-to-use graphical user interface, programmatically through DCOM or TCL interfaces and via an in-system port (via system under test)
- Self-test with extensive diagnostic information
- Repeat tests for subsequent product builds
- Protocol checker automatically checks 23 protocol rules based on the PCI Express specification
- Automatic handling of PHY and DLL features-lane/link training, flow control and retry management
- Perform regression tests

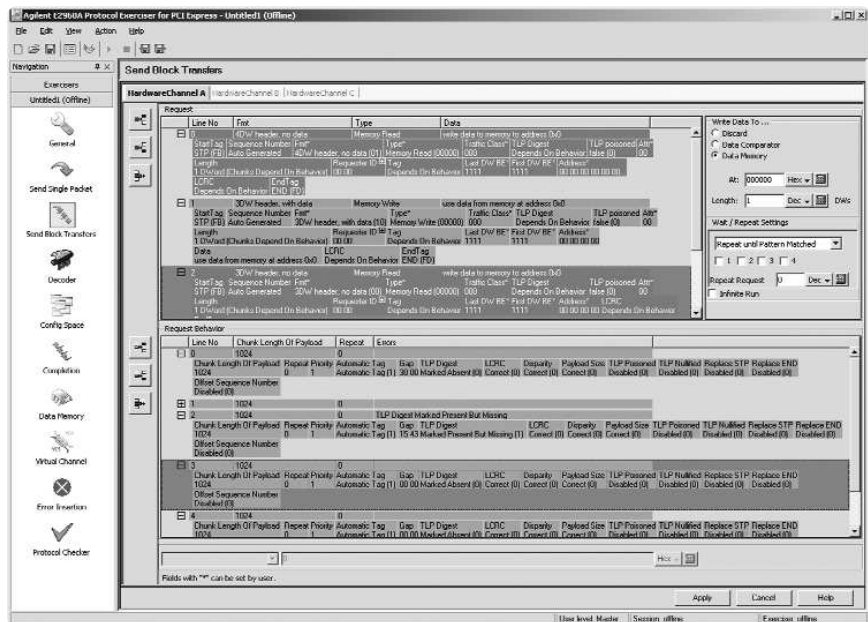


Figure 3. Protocol exerciser graphical user interface

Technical specifications for the protocol exerciser

E2960A exerciser features

Real-time performance counters	Number of TLPs, DWords, coding errors, disparity errors, successful link trainings, DLLPs, ACK DLLPs, NACK DLLPs, power management DLLPs, InitFC 1/2 DLLPs, updated FC DLLPs, TX DWords, TX TLPs, RX patterns, more
Data link layer features	Fully implemented data link control and management state machine Automatic flow control initialization; programmable credits and flow control update rate Automated generation of data link layer packets (DLLPs): ACK/NAK, Init/Update-FC Automatic generation and checking of LCRC and sequence numbers; allows the insertion of incorrect LCRCs into TLPs for testing purposes; automatic retry management
Physical layer features	Fully automated symbol encoding/decoding, and generation and validation of packet framing; ability to report framing errors to user Scrambling can be turned on or off by user Configurable, automatic link initialization and training: <ul style="list-style-type: none"> • Automatic Lane Polarity Detection (RX), separate for each lane • Programmable Lane Polarity Inversion (TX), separate for each lane • Automatic link width negotiation; all link widths x1, x2, x4, and x8 supported; user can configure which widths will be negotiated during link training • Programmable Lane Reversal (TX+RX) • Programmable Lane Skew: (± 7 symbols, resolution: 1 symbol time) Link Training and Status State Machine: Full support for states Detect, Polling, Configuration, Recovery, and L0 <ul style="list-style-type: none"> • Link states can be forced for testing purposes Programmable skip rate
Transaction layer features	User software can define arbitrary sequences of request transactions "Send Immediate" for simple packet transmission 3 hardware channels to send block transfers <ul style="list-style-type: none"> • Full support for two virtual channels (VCs) using two separate hardware channels and additional VCs with unlimited credits through third hardware channels • Pattern matcher supporting trigger out, performance counter and conditional start • Conditional start on RX pattern matcher, external trigger in/out and completion status • Generation and receiving of packets at maximum band width (stress testing) • Real time data compare of incoming data (through write requests or read completions) against data memory • Infinite loop 2 completer queues define the way completion packets are sent out (e.g., lengths, errors inserted, partitioning, etc) <ul style="list-style-type: none"> • Completions can be split into individual packets • Completions of multiple requests can be interleaved Up to 32 outstanding requests can be "pending" (256 in extended mode) Decoders (6 BARS + Expansion ROM decoder) Payload generation and reception from/into data memory Automatic or manual tag generation
Error generation and analysis features	Error insertion capabilities on the physical layer, data link layer and transaction layer Physical layer: <ul style="list-style-type: none"> • Transmitter polarity inversion • Transmitter lane reversal • Deterministic lane skew up to 7 symbols • Link width and lane sequence negotiation emulating an x1, x2, x4 or x8 device • Sending packet with incorrect "running disparity" • TX framing errors on TLPs Data link layer: <ul style="list-style-type: none"> • Programmatically answers NAK instead of ACK, for retry buffer test • Wrong sequence numbers Transaction layer: <ul style="list-style-type: none"> • Arbitrary header field contents (e.g. this enables unexpected completions and undefined message types to be sent) • Sending packets with incorrect LCRC • Sending "nullified TLPs" • Sending "poisoned TLPs" • Advertised packet length (in TLP header) larger than actual packet length (by one Dword) • The transmitter ignores flow control credits • Completion loss/delay
Configuration space features	Fully user-defined Can emulate the configuration of different types of PCI Express devices Supports up to 6 base address registers and expansion ROM decoder Device configuration space (no special root/switch registers) Full support for PCI Header type 0 configuration space Software support for PCI 2.3 extended capabilities (PME, MSI, PCI E...) Software support for PCI Express extended configuration space (registers 0x100 - 0xffc)

Flexible exerciser use models help you characterize and test your design under real conditions

Verification of the data link layer involves packet-level testing of individual requests and responses and packet sequence numbering. The main layer tested with the exerciser is the transaction layer. It tests and generates transaction layer packets and allows for emulation of a real, operational device.

Upstream use model to test the system

The protocol exerciser for PCI Express can simulate any communication via the PCI Express interface. It can stimulate the end point and react on the signals from the end point. This means the protocol exerciser interfaces with a system under test emulating an end-node by sending packets to the upstream port of the probe board.

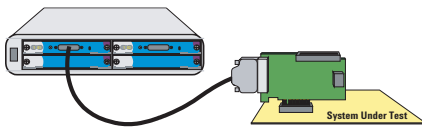


Figure 4. Protocol exerciser setup for testing a system (to upstream)

Downstream use model to test an add-in card

The protocol exerciser interfaces with an add-in card by emulating a root complex or the downstream port of a switch. This means it can be used to test the behavior of a device. In this case, you need to connect an external power supply to the probe board to power the device under test.

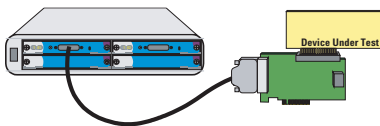


Figure 5. Protocol exerciser setup for testing a device (to downstream)

Requester capabilities

The exerciser features three hardware channels: A, B and C. Each hardware channel can handle up to 512 requests, plus 512 request behaviors to provide a stream of transactions. The request determines the transfer intention, i.e. format/type (for example, memory read) and size; the request behavior determines the behavior of an individual packet, i.e. packet size and error insertion (for example, correct or incorrect LCRC). Specified requests can be repeated up to 255 times or until a certain pattern is received by the exerciser. Hardware channel A and B support full flow control. Hardware channel A is mapped to virtual channel (VC) 0 by default. Hardware channel B can be mapped to another virtual channel between 0 and 7. Hardware channel C can be mapped to all other virtual channels between 0 and 7 not covered by hardware channel A or B. It therefore features unlimited “flow control credits.”

Completer capabilities

The exerciser features two completer queues (0,1). Each queue can handle up to 512 completion behaviors, which determine the behavior of an individual completion packet, i.e. size and error insertion (for example correct or incorrect LCRC). The two queues can be used to generate test cases to control the ordering of the completions.

Programming model

- Requester transactions are set up using “block” and “behavior” memories
- Block memory entries define blocks of read or write requests
- Behavior memory defines how individual request/completion packets are generated and behave
- This allows arbitrary sequences of TLPs and messages to be generated
- Data for the transactions is read from or written to data memory
- Sends immediate requests for configurations/messages

E2960A protocol analyzer for PCI Express gives you fast access to understandable data

The E2960A protocol analyzer for PCI Express captures the traffic or transactions on a PCI Express link and allows you to analyze it and troubleshoot problems to find the root cause. The protocol analyzer provides non-intrusive monitoring of traffic between two PCI Express end nodes (either a system talking to an add-in card or the exerciser talking to an add-in card or system). With its capabilities in analyzing generated PCI Express traffic, the analyzer is perfectly suited for turn-on and debug of PCI Express systems and designs. It captures and analyzes data-link-layer and

transaction-layer packets as well as training sequences and ordered sets.

An easy-to-use GUI offers graphical trigger setup, search and filter capabilities to help you intuitively interpret PCI Express transactions.

Powerful triggering, easy setup

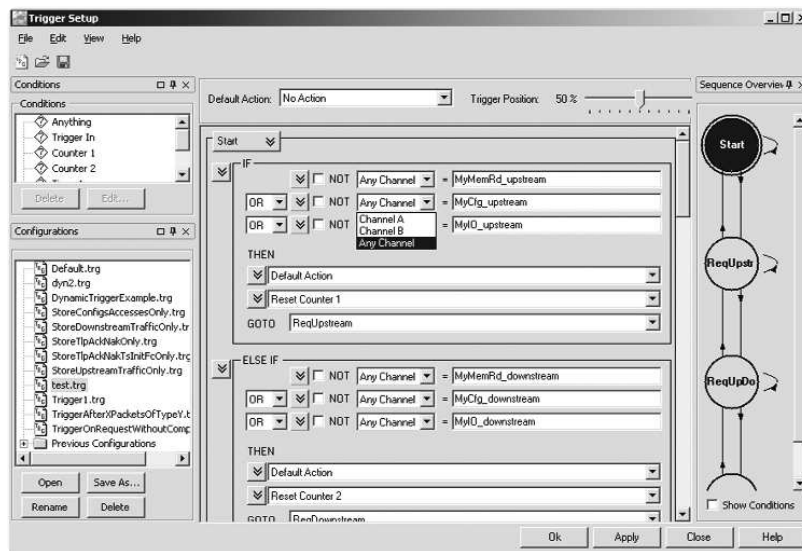
One of the key features of the protocol analyzer trigger is the Agilent patented dynamic pattern term technology. It allows you to trigger on packets that cannot be “caught” with static pattern terms, as parts of the packet content are determined

dynamically during run time (e.g. trigger on a completion that belongs to a request with the same tag value).

The protocol analyzer’s sophisticated trigger capabilities are based on a trigger sequencer. It offers an easy-to-use set up and graphical representation of the trigger sequence. Examples and listed predefined conditions reduce time-consuming trigger set-ups. You can define up to 8 states, 8 patterns and 2 counters with various actions store, increment counter, trigger out and so on.

Define the trigger and sequences in the main window pane

Get a clear overview of complex trigger set-ups. The sequencer overview pane graphically displays the trigger setup with defined states, conditions and actions.



The condition window offers a list of pre-defined trigger conditions. Just “drag and drop” to create your own trigger configurations. You also can create customized conditions.

Create customized configurations using the “drag and drop” list in the configuration window. All customized configurations can be saved.

Figure 6. Protocol analyzer trigger setup window

Protocol analyzer capabilities and benefits

All-in-one window gives you easy visibility into PCI Express transactions

- Traffic activity, port link status, and trace content are simultaneously displayed
- Sophisticated, fast screen-based traffic upload

Tabular traffic display speeds your debug process

- Avoid constant scrolling with the tabular display that maximizes information density on the screen
- See packet details by zooming on multiple lines
- Easily retrieve information with embedded markers
- Quickly find problems with automatic error detection

Multiport display for better insight into your system

- Transaction captured from multiple ports are displayed with common time stamps and common markers
- Multiple analyzers can share events for sophisticated cross triggering

Quickly find and examine sequences of interest

- Powerful search, filter and error detection functionality

Customize your measurements with test automation and scripting capabilities

- TCL script capabilities for test automation and customized test development



Figure 7. Protocol analyzer graphical user interface

Technical specifications for the protocol analyzer

E2960A analyzer features

Display features	<p>Separate, cross-correlated packet view Customizable view of captured transaction Traffic overview (post capture) Hex display Expand and collapse packets in order to obtain more information Context-sensitive field decoding Easy navigation within captured trace Tool tips for each field provide more information as needed Packets with errors are highlighted Tabular view with configurable columns Color-coded transaction types allow easy recognition of various types of traffic Markers Interleaved display, including time-stamps</p>
Trigger features	<p>Graphical trigger setup Trigger sequencer with up to:</p> <ul style="list-style-type: none">• 8 states• 2 counters/timers• 8 pattern terms• External trigger in and out• Protocol error trigger (disparity error and invalid 10b symbols) <p>Multi-way branching Filtering (real time):</p> <ul style="list-style-type: none">• Idles• On a per-packet basis controlled by the trigger sequencer <p>Filter conditions can be defined individually for each trigger sequencer state Patented dynamic triggering and storage qualification Trigger on payload (first 3 or 4 dwords)</p>
Traffic capture features	<p>Supports capturing in x1, x2, x4, x8 link width with 2.5 Gbps Non-intrusive traffic capturing Captures training sequences, ordered sets, data-link-layer packets and transaction-layer packets in both directions simultaneously Supports data rates 1.25 - 2.5 GT/s</p>
Error detection	<p>Disparity errors and invalid 10b symbols in hardware LCRC, symbol, disparity, EDB, framing, idle data Malformed packet check (CRC error, invalid field contents, length mismatch)</p>
Other features	<p>Analyzer to exerciser traffic record and replay Example traces + triggers settings + programming examples Timestamps with 8 ns resolution (absolute, relative, idle time, packet duration) Automatic lane polarity detection 1 GB trace memory Real-time statistics counters Latency measurements (using markers) External trigger in/out</p>

Use the best possible test setup for a fast turn-on

Protocol analyzer use models

There are two ways to use the protocol analyzer: You can use it standalone to analyze PCI Express transactions between two PCI Express end nodes, and you can use it with the Agilent E2969A protocol test card for PCI Express. The push button protocol test card is a standalone PCI Express test card with a graphical user interface and pre-programmed compliance tests. If any compliance test fails, it is possible to connect the analyzer to the protocol test card to do root cause analysis. The protocol test card offers a standard midbus probe footprint and the Agilent analyzer connector.

Learn more about the E2969A at www.agilent.com/find/E2969A_PTC

The add-in card use model

The protocol analyzer probe board is inserted into the system to analyze the transactions between the add-in card and the system. This means the communication between the system and the add-in card is uploaded non-intrusively through the probe board and the I/O module. The protocol analyzer simply listens to the communication. Power is provided to the probe board and the add-in card by the PCI Express connector on the system motherboard or via an external power supply connected to the probe board.

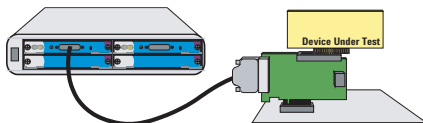


Figure 8. Protocol analyzer add-in card use model

The system test use module

The protocol analyzer probe board is inserted between the system and the protocol exerciser probe board. The protocol analyzer captures the traffic generated and sent by the protocol exerciser to the system. The fully controllable protocol exerciser generates various transactions including error conditions to the system. Additionally the protocol exerciser reacts as an end node in order to respond to the system.

The protocol analyzer captures the transactions and displays the behavior of the protocol exerciser and system communicating with each other. You can stress the system and perform worst-case-scenario tests with the protocol exerciser being used to help troubleshoot potential problems with the protocol analyzer.

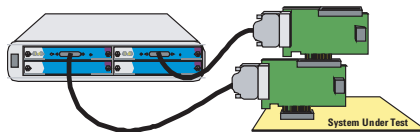


Figure 9. Protocol analyzer use model with exerciser

The chip-to-chip test use model

With the E2941A soft touch midbus probe, you can connect the protocol analyzer to a device under test without an available slot. The midbus probe can be connected to the standard footprint integrated on the individual device under test. It can be used to analyze links on a board from one chip to the other. The footprint must be implemented in the design phase of the board.

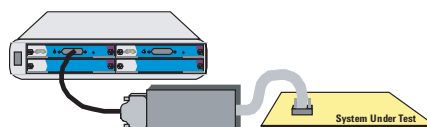


Figure 10. Protocol analyzer use model with soft touch midbus probe

Flexible probing alternatives solve possible connection issues

Slot interposer probe boards for passive and active probing

Two types of probe boards are available for the E2960A. The passive probe boards allow non-intrusive probing for the protocol analyzer. The active probe boards are intended for the exerciser; they give you the flexibility to send PCI Express packets upstream to a system under test or downstream to an add-in card under test and receive packets back.

Each probe board can accept a x1, x4, x8 or x16 add-in card, which is inserted into the x16 connector on the top of the probe board. This will operate up to PCI Express x8 for the x8 probe card. The boards are standard size short PCI cards.

One probe board is required per I/O module, except when using the E2942A single probe Y-cable. This connects two modules to one active probe board, to allow the use of the exerciser and analyzer through one active probe board. When the probe board is plugged into a motherboard, the add-in card (when using the E2960A analyzer mode) can be powered either by the motherboard or by an external AT/ATX power supply. When the E2960A is being used as an exerciser for testing an add-in card and is not plugged into a motherboard, you need a standard AT/ATX PC power supply to operate an add-in card plugged into the connector on top of the probe board.

E2942A single probe Y-cable where space is limited

This cable allows the use of one active probe board for both exerciser and analyzer simultaneously (using two I/O modules). It is a standard part of the bundle configuration with two I/O modules and is available in addition as a separate item.

Connect directly to your circuit with the E2941A soft touch midbus probe

Now you can simplify the debug and turn on of high-speed digital designs that are tight on space or that require minimal disruption of signal routing. The E2941A soft touch midbus probe increases the flexibility of the protocol analyzer by enabling a direct connection to the circuit board using a standard midbus footprint. With the E2941A soft touch midbus probe for PCI Express, you can analyze high-speed PCI Express chip-to-chip communications without interfering with the signals. The soft touch probe uses micro spring-pin technology to provide a reliable connection to the signal pads without the need for special cleaning or special surface finishes.

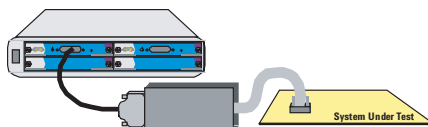


Figure 11. Soft touch midbus probe for PCI Express

Key features of the soft touch midbus probe

- Supports PCI Express x1, x2, x4, x8
- Agilent soft touch technology
- No slot connector required
- Reduced electrical load
- Eases routing of board traces
- Easy to use - can be tightened manually
- Very reliable probing
- Passive probing runs cool
- Adjusts to uneven board surfaces

The complete solution contains the E2941A soft touch midbus probe (with reference clock cable) and the N4221A PCI Express compression cable set (including five retainers). If you use this you don't need a slot interposer probe board.

Different ways to connect the midbus probe to the DUT

- N4221A Full size soft touch cable (standard specified footprint; recommended and required)
- N4228A Half size soft touch cable (fits in specified standard footprint)
- N4221F Flying lead cable set

General technical specifications

System requirements

Hardware	Pentium® processor 1 GHz or equivalent 512 MB available RAM 8 x CD-ROM driver or higher VGA resolution 1024 x 768
Operating system	Windows® 2000 or Windows XP

General characteristics

Power requirements	100 - 120 V _{ac} 200 - 250 V _{ac} 550 VA max 47 to 63 Hz
Memory	Analyzer: 1 GB trace memory Exerciser: 2 MB data memory
Display	4-character LED display on the I/O module and probe board for status information

Environment

Temperature (AT-ETM757)	Operating: 0 °C to + 55 °C Storage: -40 °C to +70 °C
Humidity (AT-ETM758)	Operating: 15% - 95% Operating soak: 90% (24 h)
Safety standards	Installation category: EN ISO/IEC 17025, IEC 61010-1/EN61010-1, II Pollution degree: 2 Environmental rating: Standard

Physical characteristics

2-slot chassis	Width: 30 cm (11.81 in); Depth: 49.0 cm (19.29 in); Height: 11 cm (4.33 in) Weight (empty): 5.1 kg (112 lbs)
4-slot chassis	Width: 45.4 cm (17.87 in) Mounts in EIA-standard 48.3 cm (19 in) rack; Depth: 49.0 cm (19.29 in) Height: 2U - 8.89 cm (3.5 in) Weight (empty): 5.1 kg (112 lbs)
Probe cable	Length: 1.5 m (59.06 in)
Single probe Y-cable	Length of black segment: 1.5 m (59.06 in) probe board to analyzer Length of white segment: 0.5 m (19.69) analyzer to exerciser

Connectors

MDI	RJ-45; 100 Mb/s Ethernet (to PC controller)
MDI-X	RJ-45; 100 Mb/s Ethernet (to next chassis)
External clock in/out	SMA connector on probe board
AT hard drive power	Connector on probe board (uses 12 V only)
External trigger in	Female BNC; Trigger input from external device
External trigger out	Female BNC; Trigger output from external device

General technical specifications (continued)

Midbus probe

Electrical specifications

Absolute maximum ratings	Amplitude data signal: $2 V_{ppdiff}$	Amplitude ref. CLK: $5 V_{ppdiff}$	
Operating conditions			
Data signals	Amplitude (at eye width of 0.85 UI)	Min: $450 mV_{ppdiff}$	Max: $1600 mV_{ppdiff}$
	Frequency: Internal CLK mode	Min: $2.5 GHz - 50 ppm$	Max: $2.5 GHz + 50 ppm$
	External CLK mode	Min: $2.5 GHz - 300 ppm$	Max: $2.5 GHz + 300 ppm$
Ref. CLK			
	Amplitude	Min: $800 mV_{ppdiff}$	Max: $2000 mV_{ppdiff}$
	DC offset	Min: $0 mV$	Max: $500 mV$
	Frequency: Internal CLK mode	Min: $100 MHz - 50 ppm$	Max: $100 MHz + 50 ppm$
	External CLK mode	Min: $100 MHz - 300 ppm$	Max: $100 MHz + 300 ppm$
Environment			
	Operating temperature: $+5^{\circ}C$ to $+55^{\circ}C$	Storage temperature: $-40^{\circ}C$ to $+70^{\circ}C$	
Physical characteristics			
	Width: 19.70 cm (7.76 in); Depth: 14.50 cm (5.70 in); Height: 2.80 cm (1.10 in); Weight: 0.75 kg / 1.65 lbs		

All specifications are valid for room temperature. Footprint design integration information for the midbus probe can be found in the PCI Express Logic Analyzer Probing Design Guide (Publication # 5989-1172EN) at: www.agilent.com/find/E2960_series

Sot/interposer probe board¹

Active probe board electrical specifications

Transmitter path	Eye opening amplitude ²	$550 mV_{ppdiff}$	
	Transition bit emphasis	2.8 dB	
	Emphasis time	1.1 ns	
	Eye opening time	290 ps ³	
Receiver path	Eye opening amplitude	Min: $220 mV_{ppdiff}$ (from PCIe™ spec)	Max: $1200 mV_{ppdiff}$ (from PCIe spec)
	Eye opening time	260 ps (measured on one lane)	
	Frequency	$2.5 Gb/s \pm 50 ppm^4$	$2.5 Gb/s \pm 300 ppm^5$

Passive probe board electrical specifications

Absolute maximum ratings	Amplitude data signal	2 ppdiff	
	Amplitude ref CLK	2.5 ppdiff	
Recommended operating conditions			
Data signals	Amplitude	Min: $175 mV_{ppdiff}$	Max: $1600 mV_{ppdiff}$
	Eye width	Min: $250 ps^6$	Max: 400 ps
	Frequency	$2.5 Gb/s \pm 50 ppm^4$	$2.5 Gb/s \pm 300 ppm^5$
	System startup lock time	Typ. 400 μs (in normal operation mode) Typ. 3 μs (in fast sync operation mode ⁷)	
Ref. CLK			
	Amplitude	Min: 800 ppdiff	Max: 2000 ppdiff
	DC offset	Min: 0 mV	Max: 500 mV
	Frequency	$100 MHz \pm 50 ppm^4$	$100 MHz \pm 300 ppm^5$

Active/passive probe board physical characteristics	Size: Standard half-length cards, as defined by the PCI Express Electrical Mechanical Specification 1.0A
	Length: 17.3 cm (6.81 in) including I/O connector
	Height: 12.6 cm (4.96 in) including metal bracket; 11.1 cm (4.37 in) excluding metal bracket

Device under test (DUT) position	Horizontal setback 2.7 cm (1.06 in); Elevated vertically 12.5 cm (4.92 in)
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¹ Specifications are valid at room temperature

² Measured using PRBS2⁵⁻¹ pattern

³ When signals come from I/O module

⁴ When I/O module is operated in internal CLK mode

⁵ When I/O module is operated in external CLK mode

⁶ Not for fast sync mode

⁷ Fast sync capture mode: This mode is optimized to analyze around power-up, link-training or L0s states, where faster analyzer reaction times are needed and you are less concerned about signal integrity. The analyzer will take less time to resume capturing after break of electrical idle, but you will probably record false errors.

How to configure a system

Choosing the test tool configurations

First, decide which link width you need: x1, x4 or x8.

Second, choose the application:

- Protocol exerciser (E2960A-E01, E2960A-E04, E2960A-E08)
- Protocol analyzer (E2960A-A01, E2960A-A04, E2960A-A08)
- Protocol analyzer and protocol exerciser on one I/O module (E2960A-C01, E2960A-C04, E2960A-C08)
- Protocol analyzer and protocol exerciser with two I/O modules to use in parallel in the same application (E2960A-B01, E2960A-B04, E2960A-B08)
- Validation station fully populated with protocol exerciser modules used for validation purposes like stress testing (E2960A-V02 two exercisers in the 2-slot chassis, E2960A-V04 four exercisers in the 4-slot chassis)

It is also important to decide whether you need a 2-slot chassis or a 4-slot chassis. Chose the 4-slot chassis if you plan to depends if you want to extend the platform later.

Finally, decide whether you need a midbus probe.

Each complete corresponding configuration includes the following as minimum:

- One 2- or 4-slot chassis (selectable)
- One serial I/O module
- One probe board
- Analyzer Software Package (ASP) or Exerciser Software Package (ESP)

Optional accessories:

E2941A soft touch midbus probe for PCI Express for the protocol analyzer (N4221A PCIe compression cable set is required to complete the E2941A)

E2942A single probe Y-cable (included in E2960A-B01, E2960A-B04, E2960A-B08)

The complete configurations in the table (Figure 12) provide full functionality and they include all the standard hardware and software (chassis, I/O module, slot/interposer probe board, and software package). A protocol analyzer/exerciser with one I/O module can be used interchangeably for analyzing or exercising your device. It is not possible to run the protocol analyzer and the protocol exerciser simultaneously on one module.

A protocol analyzer/exerciser with two I/O modules can be used simultaneously as an analyzer and exerciser and includes a single probe Y-cable.

The upgrade and expansion possibilities show the additional hardware and software available to adapt your solution to changing requirements at a later date.

Typical pre-defined configuration e.g. E2960A-B08:

1 x E2960A-FR2	2-slot chassis
2 x N5305A	Serial I/O module with cable
1 x E2968A	Probe board for PCI Express x8
1 x E2962A	Analyzer Software Package for x8
1 x E2964A	Exerciser Software Package for x8
1x E2942A	Single probe Y-cable
1x E2947A	Passive probe board for PCI Express x8

Ordering information

Complete configurations		PCI Express x1	PCI Express x4	PCI Express x8
Protocol analyzer	E2960-	A01	A04	A08
Protocol exerciser	E2960-	E01	E04	E08
Protocol analyzer/exerciser bundle (one I/O module)	E2960-	C01	C04	C08
Protocol analyzer/exerciser bundle (two I/O modules)	E2960-	B01	B04	B08
2-slot validation station	E2960-			V02
4-slot validation station	E2960-			V04

Upgrade and expansion possibilities		PCI Express x1	PCI Express x4	PCI Express x8
Protocol analyzer software package ASP	E2960A	E2961A	E2965A	E2962A
Protocol exerciser software package ESP	E2960A	E2963A	E2966A	E2964A
Active probe board	E2960A	E2938A	E2939A	E2968A
Passive probe board	E2960A	E2945A	E2946A	E2947A
Soft touch midbus probe+ PCIe compression cable set	E2960A	E2941A+N4221A	E2941A+N4221A	E2941A+N4221A
Single Probe Y-Cable	E2960A	E2942A	E2942A	E2942A

Figure 12. Product selection guide for the E2960A for PCI Express

Agilent offers a variety of service options to support you in getting the most from your E2960A analyzer/exerciser

Start-up assistance

Recommended for new users of the E2960A. This service focuses on speeding your time to measurement in your environment. You will learn to navigate the capabilities of the E2960A and focus on applying the measurements you need to make for your application.

Productivity assistance

Aimed at experienced users who may have a unique problem they are trying to solve and are looking for ways to enhance the use of the product. Examples of productivity assistance might include automating the test suite,

avoiding common measurement errors and improving accuracy or understanding and analyzing a measurement with your device.

Training and education

Agilent offers several classes related to the exerciser/analyzer for PCI Express:

- Exerciser/Analyzer for PCI Express Fundamentals
- Programming the Exerciser/Analyzer for PCI Express
- Advanced Validation Techniques Using Exerciser/Analyzer for PCI Express

Warranty options

All models include a standard 1-year warranty. Contact your local sales office for prices of extended options:

Option number	Description
	3-years of return-to-Agilent
	5-years of return-to-Agilent

You have the maximum flexibility in your purchase options.

Purchase one of the two scope/logic analyzer bundles described below. Reference promotion code 5.455 when ordering.

Scope & Standalone or PC-hosted Logic Analyzer Bundle

Purchase any 500 MHz or 1 GHz DSO6000 or MSO6000 with ≥ 2M of memory, receive a 20% discount on any 1680 Series standalone or 1690 Series PC-hosted logic analyzer. You also receive a FREE E5850A time correlation fixture.

Scope & Modular Logic Analysis System Bundle

Purchase any 500 MHz or 1 GHz DSO6000 or MSO6000 with ≥ 2M of memory and receive a 20% discount on one of the following logic analysis systems: You also receive a FREE E5850A time correlation fixture.

- 16900A or 16902A mainframe and one to six of the following modules: 16910A, 16911A, 16950A module with ≥4M of memory or a 16760A module

OR

- 16903A mainframe and one to three of the following modules: 16910A, 16911A, 16950A module with ≥ 4M of memory or a 16760A module

Maximize your investment and flexibility with a modular system. Customize a system for your current needs and expand as your needs evolve. Additional measurement capability includes higher state and timing speeds (up to 1.5 Gb/s state, 4 GHz timing), more channels, deeper memory, pattern generator and differential signal support.

Related Literature

Publication Title	Publication Type	Publication Number
<i>Serial Protocol Tester XC</i>	Brochure	5989-0159EN
<i>PCI Express Tools, from the Physical Layer to a Fully Operating System</i>	Brochure	5988-7780EN
<i>Protocol Test Card for PCI Express</i>	Photocard	5988-9502EN
<i>E2969A Protocol Test Card for PCI Express</i>	Data sheet	5989-0878EN

Product Web site

For the most up-to-date and complete application and product information, please visit our product Web site at:

www.agilent.com/find/E2960_series

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