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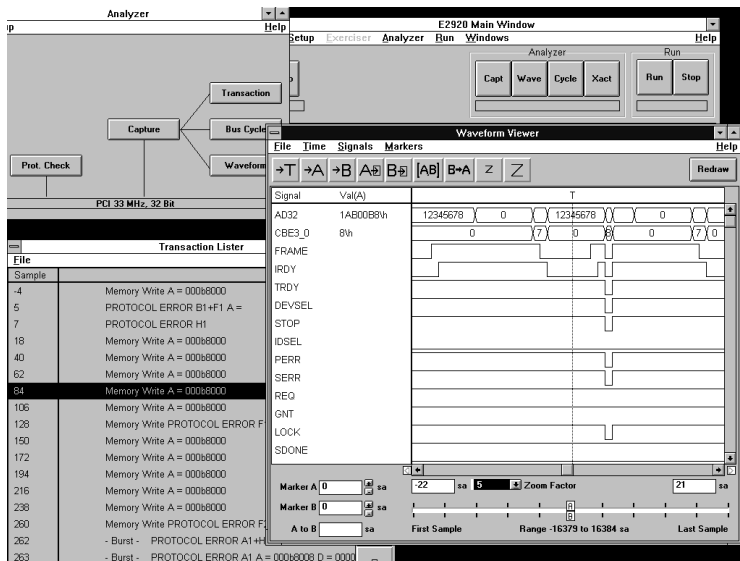
Agilent Technologies
Innovating the HP Way

HP E2970A PCI Analyzer Graphical User Interface for Windows 95/NT



Technical Specifications

HP E2970A PCI Analyzer Graphical User Interface for HP E2925A PCI Exerciser and Analyzer Card

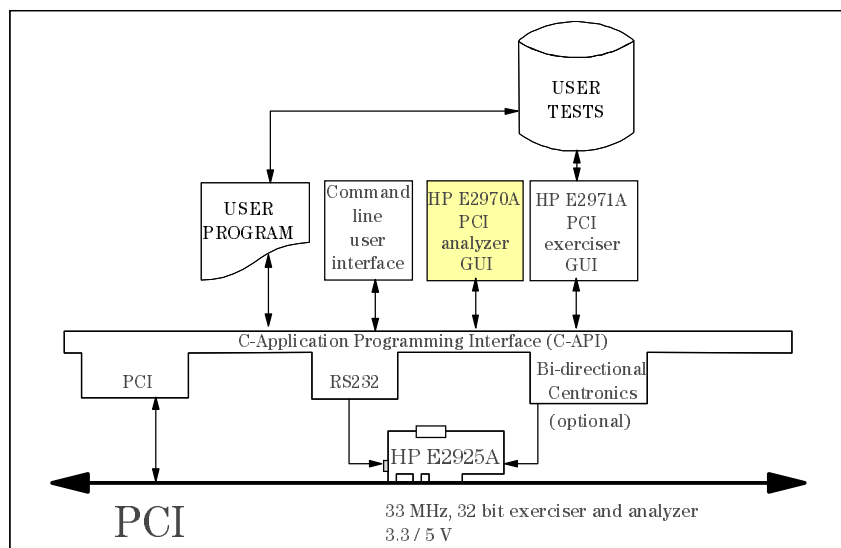


HP E2970A PCI analyzer graphical user interface

Key Features

- Easy PCI-oriented setup of triggering and storage qualification.
- Fast setup and monitoring of protocol checker.
- State waveform lister displays trace of all PCI signals, trigger I/O, and triggering signals.
- Bus cycle lister disassembles bus traffic per state, with comprehensive error reporting.
- Bus transaction lister summarizes bus transfers.

Part of the HP E2920 Computer verification tools, PCI series, the HP E2970A PCI analyzer graphical user interface provides a comprehensive Windows 95/NT interface for the on-board PCI state logic analyzer of the HP E2925A PCI exerciser and analyzer. It allows you to quickly and easily analyze PCI bus traffic, either using an external PC connected via the bi-directional Centronics interface (fast host interface, HP E2925A option 002), or via RS232, or using the system-under-test itself accessing the card via PCI.

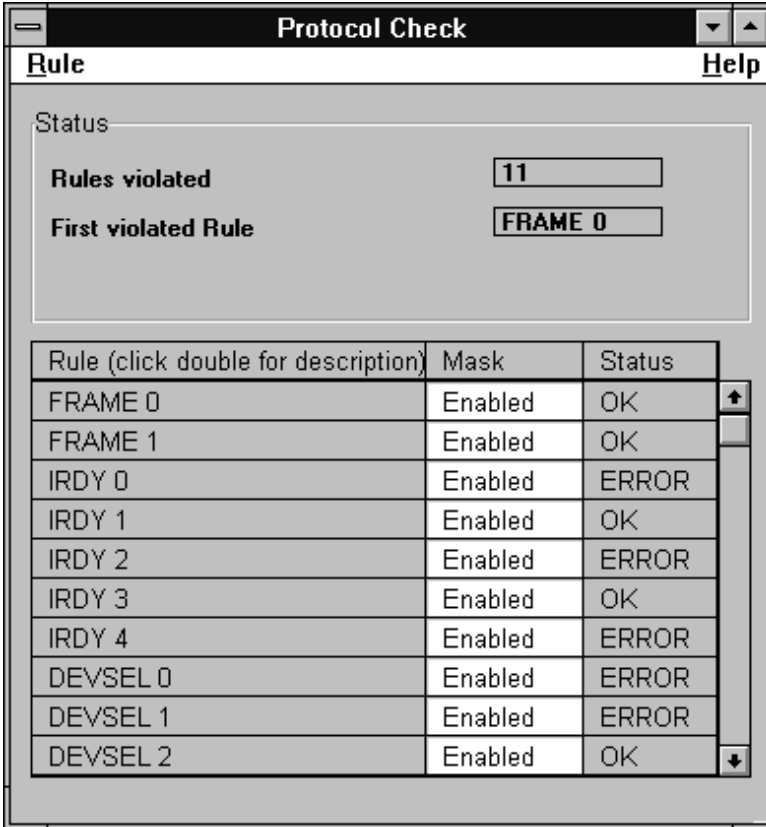


HP E2920 Computer verification tools, PCI series

Protocol Checker

Using the protocol checker window, you can individually enable or disable any of the twenty-five protocol rules which are checked by the protocol checker on the PCI exerciser and analyzer. You can also monitor the individual status of the rules (violated or OK), and you can see a status summary, accumulated since the last time the checker was reset, giving the following details:

- total number of violated rules,
- first rule violated.



The screenshot shows a window titled "Protocol Check" with a "Rule" tab and a "Help" button. The window displays a summary of violated rules and a table of rule statuses.

Status

Rules violated 11

First violated Rule FRAME 0

| Rule (click double for description) | Mask | Status |
|-------------------------------------|---------|--------|
| FRAME 0 | Enabled | OK |
| FRAME 1 | Enabled | OK |
| IRDY 0 | Enabled | ERROR |
| IRDY 1 | Enabled | OK |
| IRDY 2 | Enabled | ERROR |
| IRDY 3 | Enabled | OK |
| IRDY 4 | Enabled | ERROR |
| DEVSEL 0 | Enabled | ERROR |
| DEVSEL 1 | Enabled | ERROR |
| DEVSEL 2 | Enabled | OK |

Capture Window

The capture window allows you to set up both the triggering and storage qualification for the PCI analyzer.

Trigger

You can quickly and easily set the analyzer to trigger:

- Immediately.
- On a user-defined pattern, including a particular bus command or any one of a group of bus commands, with or without address qualification.

The trigger point is always in the middle of the trace memory to allow pre- and post-trigger analysis.

Trigger | Storage |

Immediate

Pattern

Clear

| Signal | Value |
|---------|-----------|
| AD32 | 00b8xxx'h |
| CBE3_0 | x'h |
| b_state | x1x\b |
| m_lock | x\b |
| m_act | x'h |
| t_lock | x\b |
| t_act | x\b |
| DEVSEL | x\b |
| IRDY | x\b |
| TRDY | x\b |
| FRAME | x\b |
| SERR | x\b |
| PERR | x\b |
| IDSEL | x'h |

Occured Once

Did not repeat within Cycles

OK

Cancel

Storage

Without having to set up complex trigger sequences, you can use push-buttons to select storage qualifiers to tune the use of the state analyzer memory, depending on the level of detail you need, for example:

- store all states,
- store only particular bus transactions by command type, or combinations thereof,
- suppress idle cycles,
- suppress wait cycles,
- suppress data transfers.

Trigger | Storage |

All

Selected Transactions / States

| Signal | Value |
|----------|--------------|
| m_act | x\b |
| t_act | x\b |
| xact_cmd | 3'h 0x00\b |

Selected Bus States

Suppress Idle Cycles

Suppress Wait Cycles

OK

Cancel

Waveform Lister

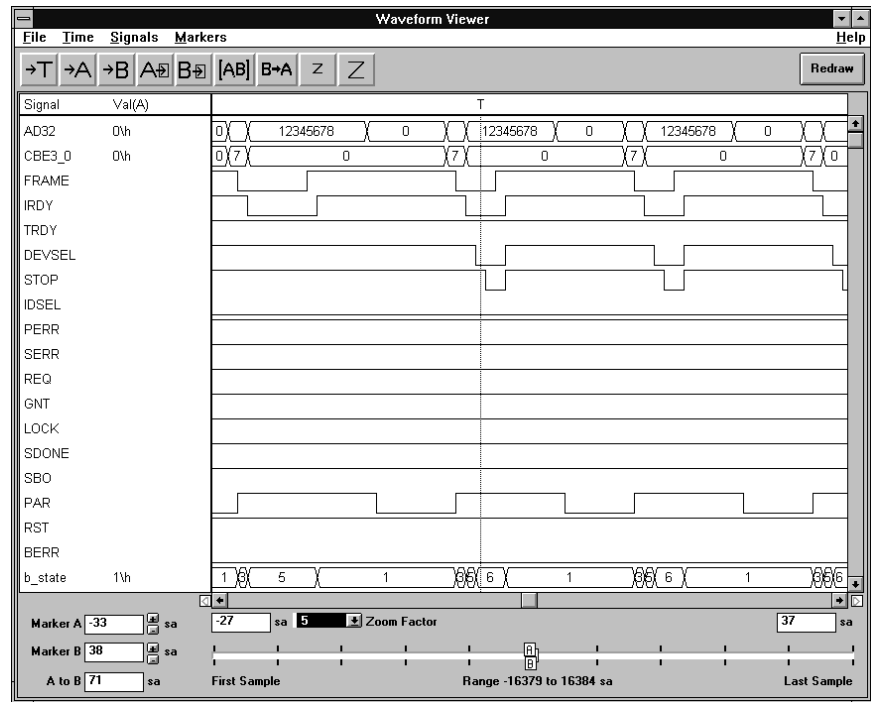
The waveform lister provides a scaleable waveform trace of the captured bus traffic. You can configure which signals are displayed and their order.

Bus Cycle Lister

Disassembles the captured traffic to provide a complete clock-based listing of PCI cycles. Detected protocol violations are clearly indicated with cross-references to the PCI specification.

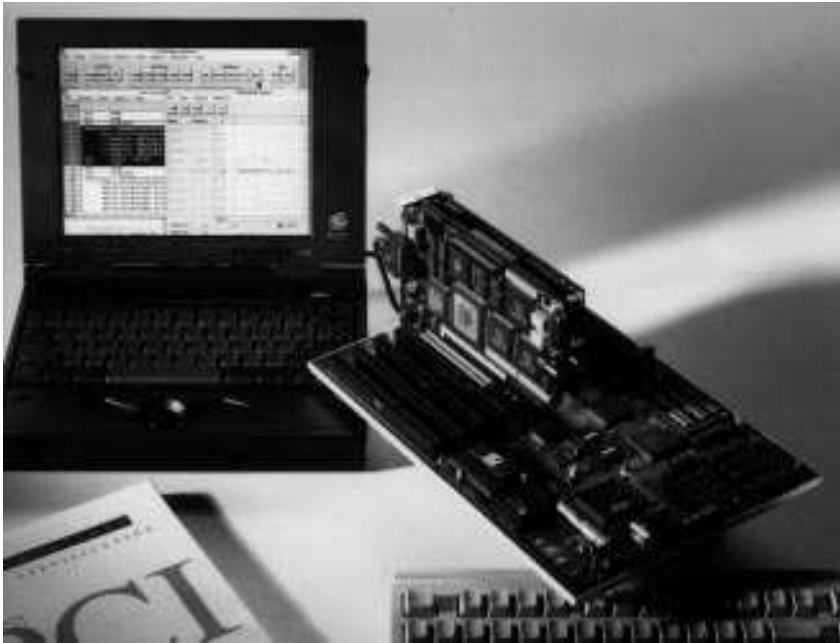
Transaction Lister

The transaction lister further disassembles the data to provide a per transaction overview: transaction type, address, and data content, for example.



| Sample | Description |
|--------|---|
| -4 | Memory Write A = 000b8000 |
| -3 | WAIT (no DEVSEL#) |
| -2 | WAIT (no DEVSEL#) |
| -1 | WAIT (no DEVSEL#) |
| 0 | WAIT (no DEVSEL#) |
| 1 | WAIT (no DEVSEL#) |
| 2 | WAIT (no DEVSEL#) |
| 3 | WAIT (no DEVSEL#) |
| 4 | IDLE -MASTER ABORT |
| 5 | LOCK# SERR# PERR# ERROR B1: IRDY# must not be asserted on the same clock edge that |
| 6 | WAIT (no DEVSEL#, no IRDY#) |
| 7 | IDLE -MASTER ABORT ERROR H1: The earliest a master can terminate a transaction with mas |
| 8 | IDLE |
| 9 | IDLE |
| 10 | IDLE |
| 11 | IDLE |
| 12 | IDLE |
| 13 | IDLE |
| 14 | IDLE |
| 15 | IDLE |
| 16 | IDLE |
| 17 | IDLE |
| 18 | Memory Write A = 000b8000 |
| 19 | WAIT (no DEVSEL#) |
| 20 | WAIT (no DEVSEL#) |
| 21 | WAIT (no DEVSEL#) |
| 22 | WAIT (no DEVSEL#) |

| Sample | Description |
|--------|---|
| -4 | Memory Write A = 000b8000 |
| 5 | PROTOCOL ERROR B1 +F1 A = |
| 7 | PROTOCOL ERROR H1 |
| 18 | Memory Write A = 000b8000 |
| 40 | Memory Write A = 000b8000 |
| 62 | Memory Write A = 000b8000 |
| 84 | Memory Write A = 000b8000 |
| 106 | Memory Write A = 000b8000 |
| 128 | Memory Write PROTOCOL ERROR F1+H7 A = 000b8000 |
| 150 | Memory Write A = 000b8000 |
| 172 | Memory Write A = 000b8000 |
| 194 | Memory Write A = 000b8000 |
| 216 | Memory Write A = 000b8000 |
| 238 | Memory Write A = 000b8000 |
| 260 | Memory Write PROTOCOL ERROR F2+H2+PARITY ERRO |
| 262 | - Burst - PROTOCOL ERROR A1+H2+PARITY ERROR A |
| 263 | - Burst - PROTOCOL ERROR A1 A = 000b8008 D = 0000 |
| 264 | - Burst - PROTOCOL ERROR A1+PARITY ERROR A = 0 |
| 265 | - Burst - PROTOCOL ERROR A1 A = 000b8010 D = xx00 |
| 266 | - Burst - PARITY ERROR A = 000b8014 D = xx00xx00 |



HP E2970A PCI analyzer graphical user interface with HP E2925A 32 bit, 33 MHz PCI exerciser and analyzer card

System Requirements

To use the HP E2970A PCI analyzer graphical user interface, you require a PC with the following specifications:

PC: IBM-PC or 100% compatible with recommended minimum 90 MHz Pentium CPU and CD-ROM drive.

Graphics: 800 x 600 required, recommended 1024 x 768 SVGA.

O/S: Windows 95 or Windows/NT.

Memory: 16 MB minimum, 24 MB recommended.

Hard disk: minimum 50 MB available disk space required, 100MB recommended.

Interfaces: for the HP E2970A graphical user interface, either the fast host interface HP E2925A option 002 of the PCI exerciser and analyzer card, or accessing the card via PCI, is recommended. Alternatively, an RS232 port can be used. A parallel port is required for the software ID module, supplied with the HP E2925A, to enable the software license.

Expansion slots: for the fast host interface HP E2925A option 002 of the PCI exerciser and analyzer card, one ISA slot is required to host the bi-directional Centronics card.

Ordering Information

The HP E2970A includes:

- License to use the PCI analyzer GUI software with a single PCI exerciser and analyzer card.
- Software media (CD-ROM).

Note that if you want to simultaneously analyze more than one HP E2925A card using a single PC, you require the appropriate number of HP E2970A GUIs running on that PC, as well as sufficient fast host interface options (or RS232 ports) to connect to each card (unless you are connecting via PCI).

Related HP Literature

- HP E2925A 32 bit, 33 MHz PCI exerciser and analyzer, technical specifications, p/n 5965-4724E.
- HP E2971A PCI exerciser graphical user interface for Windows 95/NT, technical specifications, p/n 5965-4725E.

For more information:

<http://www-europe.hp.com/dvt>

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