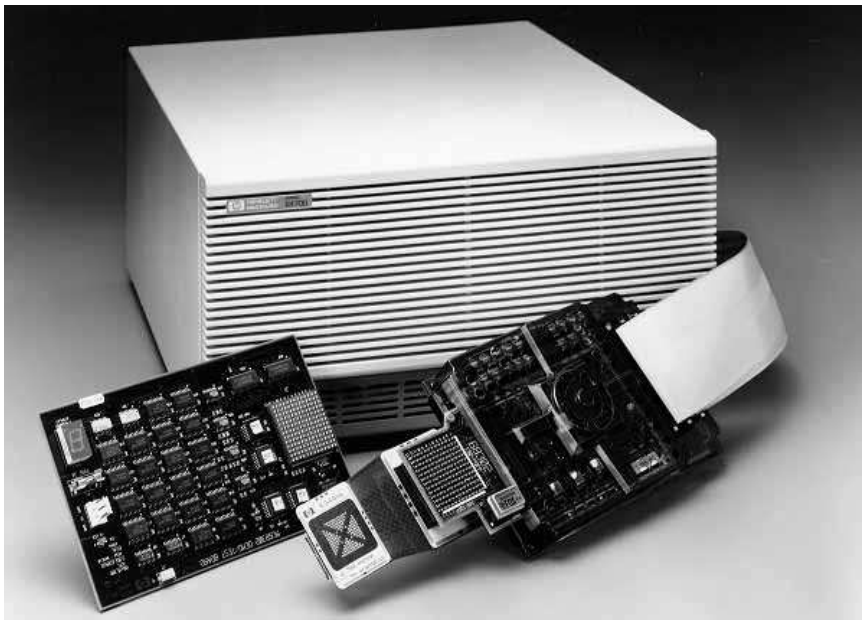
HEWLETT® PACKARD

HP 64798C Emulator for the Motorola 68302 Microprocessor

Design, Debug, and Integrate Real-time Embedded Systems

Product Overview



Hewlett-Packard has the microprocessor development solutions that you need to meet time-to-market and quality goals for Motorola 68302 microprocessor-based designs.

HP 64798C emulator comes with 56Kbytes to 8 Mbytes of emulation memory and a 25MHz-68302 processor in the emulation pod. They support all of the standard emulation features, such as real-time trace and symbolic debug.

The emulator card plugs into a modular cardcage, which connects to your host via RS-232, or LAN. Easy-to-use interfaces are offered on IBM-compatible PCs, Sun SPARCstations, and HP 9000 Series 700 workstations. Additionally, the cardcage's firmware-resident interface can talk to any ASCII terminal.

Designers are assured of a full line of support with modular emulation tools and software support on a wide range of platforms. Hewlett-Packard has integrated the emulator with code development, debug, emulation, software performance analysis, and software test verification into a comprehensive package that will meet your embedded design requirements. You have the choice of selecting the entire development package or only the parts that you need at a specific time.

For PC-hosted embedded development, a real-time C debugger user interface combines the ease of use of a full Microsoft Windows with HP 64700's transparent, real-time emulation. This allows you to debug embedded C programs at the source level, while your target runs at full speed.

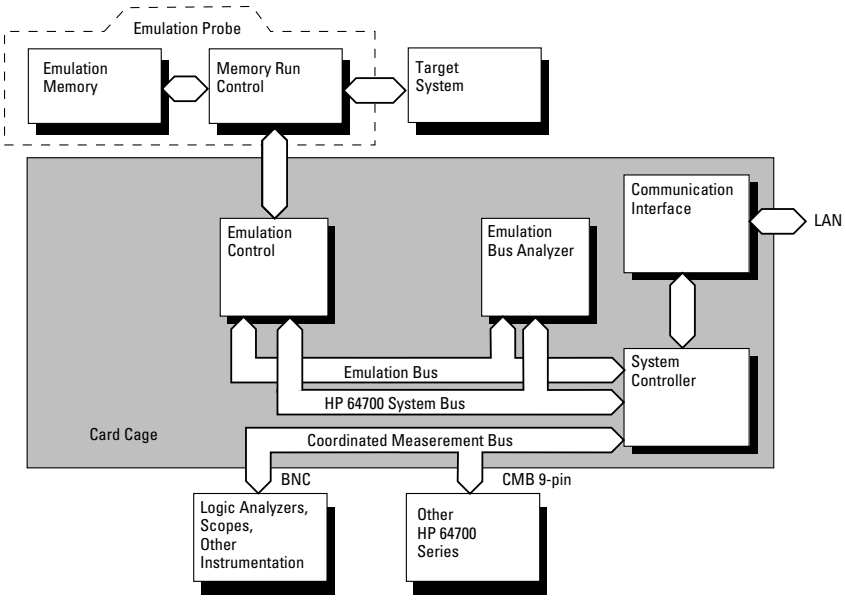
Workstation-hosted embedded development is supported with the X/Motif-based HP Embedded Debug Environment, an integrated suite of tools that supports software development. The environment provides easy-to-use measurement capabilities ranging from real-time, nonintrusive analysis to high-level C debugging.

MOTOROLA 68K DEVELOPER PROGRAM

HP is a Platinum member of the Motorola Developer Program.

Features

- 25 MHz*, zero-wait-state in target memory
- 25 MHz*, zero-wait-state in emulation memory
- Supports 5V processor versions
- Configuration menu for easy emulator setup
- Processor-specific, on-line help in Motorola format
- Display, modification, and high-level interpreted displays of on-chip peripheral registers
- Processor and emulator configuration is cross checked for inconsistencies and incompatible selections; understandable error and warning messages are given
- Reads processor registers and automatically generates startup code
- Background-style monitor
- External TTL, internal oscillator, and internal crystal clocks supported.
- 36-inch probe cable terminating in an active probe
- Unlimited software execution breakpoints
- Multiprocessor emulation: synchronous start of up to 32 emulators
- Cross triggering from another emulator, logic analyzer, or oscilloscope
- 56 Kbytes of built-in dual-port emulation memory
- LAN connection



HP 64700 Series modular architecture offers a selection of emulators, emulation bus analyzers, optional software performance analyzer, and other tools.

Emulation bus analyzer

- 80 channels available with trace buffer depths of 1K, 8K, 64K, or 256K
- Postprocessed software-based dequeued trace with symbols and source lines
- Eight events, each consisting of address, status, and data comparators
- Events may be sequenced eight levels deep
- Timing and state counts
- Prestore capability

Emulation memory

- 56 Kbytes of built-in dual-port emulation memory
- 256 Kbyte, 512 Kbyte, 1 MByte, 1.25 Mbyte, 2 Mbyte, 4 Mbyte, 4.25 Mbyte, 5 Mbyte, and 8 Mbyte memory configurations of optional SIMM memory
- Mapping resolution to 256 bytes

Software support

- Real-time operating system measurement tools
- Operates with the real-time, software performance analyzer
- Real-time C debugger for PC-hosted development
- Support for IEEE-695, HP OMF, Motorola S record and extended Tek HEX file formats (symbols supported with IEEE-695 and HP OMF)

*Contact your HP 64000 Field Engineer for the latest configuration information, supported processor speeds, and software options.

Cardcage

The cardcage is the basis for modular emulators and analyzers. It can be disassembled and reassembled easily for cost-saving reconfiguration to support 8-, 16-, and 32-bit processors.

The cardcage contains a RS-232-C serial port with a standard 25-pin serial connector in addition to LAN connection.

Bundles

HP offers a bundle for those who want a complete emulation system for 68xxx processor. The HP 647xxxXY bundle is a convenient way to order all of the necessary components that complete an HP 64700 Series Emulator.

Each bundle contains your choice of a PC or Workstation based user interface. It includes an HP 64700B card cage, HP 64172B 1 Mbyte memory SIMM, HP 64794A emulation bus analyzer, HP 64748C emulation control card, and the HP 64700xxx Run Control Probe.

Networking

In many embedded designs, it is not possible for each member of a design team to have a target system and an emulator. This makes it essential to have remote access from a networked host. The HP 64700 series emulators offer a LAN connection so that you are able to share a central emulator and target from either a PC or workstation. Not only can team members share a common emulator and database, but you also have rapid file transfers at rates of up to six megabytes per minute for increased productivity. The cardcage connects to all popular Ethernet 802.3 networks through a 10Base2 ThinLAN BNC connector or a 15-pin AUI (attachment unit interface). TCP/IP protocols, LAN gateways, and ARPA/ Berkeley standards are supported.

Emulation bus analysis

Emulation bus analysis provides real-time, nonintrusive analysis along with extensive triggering, tracing and qualification features. Analysis features offer selective tracing, time tagging, prestore, and a selection of trace depths of 1K, 8K, 64K, or 256K. These comprehensive resources combine to solve both simple and complex problems.

Real-time, nonintrusive analysis is achieved through a dual-bus architecture. This allows traces to be set up and reviewed without stopping processor execution. Selective tracing of microprocessor code flow, without stopping execution, is a major strength of the HP 64700 series emulators and analyzers.

Up to eight hardware breakpoint resources, each consisting of address, data, and status event comparators, can be combined in sequential trace specifications, using “find A, followed by B...” constructs up to eight levels deep. A range comparator can be applied to address or data events at any one of these levels. The analyzer will trigger on and store all subsequent execution, or store only specified execution information.

Precise time tagging of events helps you identify discrepancies in code execution. Each event is logged into the analyzer with an execution time. Bus cycle, instruction, and module duration can be measured at full processor speeds.

Prestore assists you in pinpointing possible problem areas in your code. Prestore can determine which of several different functions is accessing a variable and is responsible for corrupting it.

Real-time emulation

The HP 64798C active probe emulators contain the microprocessor, emulation monitor, run-control circuits, and up to 8 Mbytes of emulation memory. Each emulator uses a background monitor which uses no target address space.

Extensive breakpoint capabilities allow you to define where to stop the execution of code. Software breakpoints can be set up in the emulator, allowing execution to be halted at an instruction point. Real-time hardware break events increase the flexibility and power of this feature, extending functionality to include stopping at processor address, data, status points, or a combination of all three.

Flexible memory configuration

Memory modules are used for emulation memory. Two slots are available on the active probe, allowing you to plug in the amount of memory you need—up to 8 Mbytes. If you initially order less than the maximum, you can easily expand by adding modules. Modules for 256 Kbytes (HP 64171/2A), 1 Mbyte (HP 64171/2B), and 4 Mbytes (HP 64173A) are available. Built-into the emulator is 56 Kbytes of dual-ported emulation memory with *no* timing intrusion, allowing you to display and modify critical program variables without halting the target system.

Robust symbolic support

Symbolic debugging is available when using the PC-hosted real-time C debugger, emulator/analyzer, and workstation-hosted software tools. Symbolic debugging clarifies trace list interpretation by allowing you to see program symbols in the trace list. This facilitates quick identification of problems involving the interaction of software and hardware. You also can use symbols in emulation commands and expressions to simplify command entries and user interaction.

Workstation-hosted environment

The HP Embedded Debug Environment is a collection of integrated tools that assist you during software development. These tools include the emulator/analyzer user interface, debugger/simulator, advanced cross language system, and the real-time software performance analyzer.

The **emulator/analyzer** tool gives you the ability to perform trace analysis, set breakpoints, and establish emulator configuration parameters. In addition, the graphical interface tool is integrated with the embedded debug environment, which coordinates high-level software debugging with low-level microprocessor run control.

Optional **software performance analysis** enables you to tune and verify the time-critical aspects of your design. These capabilities are provided at both the C source and assembly language levels. Through automated one-key setup, this system quickly identifies code bottlenecks and gathers statistics and timing information that aid in solving time-critical problems. The software performance analyzer operates with HP 9000 Series 300/400/700 workstations and Sun SPARCstations.

PC-hosted environment

The real-time C debugger is a mouse-driven Microsoft Windows-based, graphical user interface for HP 64700 emulators. The debugger takes full advantage of the emulator's dual-bus architecture and dual-ported memory to perform many C and assembly debug functions while the target runs at full speed. This means that C debugger functions such as setting breakpoints, display and edit of C variables, and measurement of C program behavior can now often be performed without interrupting program execution. This traditionally could be performed only when a user program was stopped.

Terminal mode operation

A firmware-resident ASCII terminal interface is embedded in the emulator, supplying commands for all emulation and analysis features. Commands are ASCII strings; file transfers using industry-standard formats are accepted. Since a terminal can access these commands, host independence is realized.

Specifications and Characteristics

Processor compatibility

The HP 64798C emulator supports the Motorola 68302 microprocessor operating at clock speeds up to 25 MHz.* The emulator supports 5V operation. It can be plugged into a PGA, CQFP, PQFP or TQFP target system using optional accessories.

Environmental

Temperature: operating, 0° to +40°C (+32°F to +104°F); nonoperating, -40°C to +70°C (-40°F to +158°F).

Altitude: operating /nonoperating, 4600 m (15 000 ft)

Relative humidity: 15% to 95%.

Regulatory Compliance

(When installed in HP 64700 cardcage)

Electromagnetic interference:
CISPR 11:1990/EN 55011 (1991): group 1 class A
IEC 801-2:1991/EN50082-1 (1992): 4 kV CD, 8 kV AD
IEC 801-3:1984/EN50082-1 (1992): 3 V/m, 80% modulation, 26 MHz-1000 MHz
IEC 801-4:1988/EN50082-1 (1992): 0.5 kV signal lines, 1 kV power lines

Safety approvals: self-certified to UL 1244, IEC 1010-1, CSA-C22.2 no. 231 Series-M89

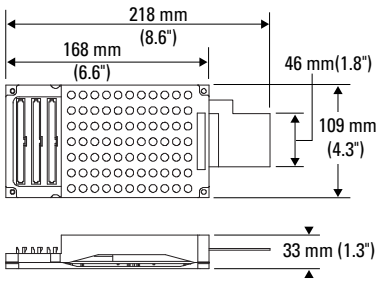
Physical

Emulator dimensions: 173 mm height x 325 mm width x 389 mm depth (6.8 in. x 12.8 in. x 15.3 in.)

Cable length: emulation control card to probe, approximately 914 mm (36 inches).

Probe weight: 0.3 kg (10 oz).

Probe dimensions:



Electrical

DC electrical specifications

Characteristic	Signal	Symbol	Min	Max	Unit
Input High Voltage	All Except EXTAL	V_{IH}	2.0	V_{DD}	V
Input Low Voltage	All Except EXTAL	V_{IL}	V_{SS} - 0.3	0.8	V
Input High Voltage	EXTAL	V_{CIH}	4.0	V_{DD}	V
Input Low Voltage	EXTAL	V_{CIL}	V_{SS} - 0.3	0.6	V
Output High Voltage (I_{OH}= 400 mA)	$\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{IACK7}$, R/$\overline{W}$, $\overline{CS0}$-$\overline{CS3}$, FC0-FC2 (Unbuffered)	V_{OH}	V_{DD} - 1.0	—	V
	$\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{IACK7}$, R/$\overline{W}$, $\overline{CS0}$-$\overline{CS3}$, FC0-FC2 (Buffered)		3.5	—	V
	CLKO		V_{DD} - 1.0	—	
	All Other Outputs		V_{DD} - 1.0		
Output Low Voltage (I_{OL} = 3.2 mA)	A-1-A23, PB0-PB11, FC0-FC2, $\overline{CS0}$-$\overline{CS3}$, IAC, $\overline{AVEC}$, $\overline{BG}$, RCLK1, RCLK2, TCLK1, TCLK2, TCLK3, $\overline{RTS1}$, $\overline{RTS2}$, $\overline{RTS3}$, SDS2, PA12, RXD2, RXD3, $\overline{CTS2}$, $\overline{CD2}$, $\overline{CD3}$, $\overline{DREQ}$, BRG1	V_{OL}	—	0.5	V
	CLKO		—	0.4	
Output Low Voltage (I_{OL} = 5.3 mA)	D0-D15, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, $\overline{BERR}$, $\overline{BGACK}$, $\overline{BCLR}$, $\overline{DTACK}$, $\overline{DACK}$, $\overline{RMC}$, $\overline{RESET}$	V_{OL}	—	0.5	V
Output Low Voltage (I_{OL} = 7.0 mA)	TXD1, TXD2, TXD3	V_{OL}	—	0.5	V
Output Low Voltage (I_{OL} = 8.9 mA)	$\overline{DONE}$, $\overline{HALT}$	V_{OL}	—	0.5	V
Input Low Current (V_{IL} = 0 V)	A1	I_{IL}	—	0.4	mA
	A2, A3, $\overline{IPL0}$-$\overline{IPL2}$, BUSW, DISCPU, $\overline{FRZ}$, $\overline{BGACK}$		—	0.2	mA
	A4-A23, D0-D15		—	70	uA
	FC0-FC2, PB0 ($\overline{IACK7}$)		—	0.5	mA
	$\overline{AS}$		—	1.0	mA
	$\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$		—	0.6	mA
	$\overline{RESET}$, $\overline{HALT}$, $\overline{BERR}$, $\overline{DTACK}$		—	0.7	mA
	All Other Signals		—	20	uA
Input High Current (V_{IH} = V_{DD})	A1, FC0-FC2, $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$, PB0, ($\overline{IACK7}$)	I_{IH}	—	60	uA
	A2, A3, $\overline{RESET}$, $\overline{HALT}$, $\overline{BERR}$ $\overline{DTACK}$, $\overline{BGACK}$		—	30	
	All Other Signals		—	20	
Input Capacitance (With 144-pin TQFP or 132-pin PQGP adaptor cable)	A1-A3	C_{IN}	—	70	pF
	A4-A23		—	60	
	D0-D15, FC0-FC2		—	90	
	$EXTAL_{Note\ 1}$		—	50	
	$\overline{RESET}$, $\overline{HALT}$, $\overline{BERR}$, $\overline{AS}_{Note\ 1}$		—	105	
	$\overline{UDS}$, $\overline{LDS}$, R/$\overline{W}$		—	75	
	$\overline{IPL0}$-$\overline{IPL2}$, $\overline{BGACK}$		—	55	
	BUSW, DISCPU, $\overline{FRZ}$, $\overline{DTACK}$, PB0 ($\overline{IACK7}$)		—	65	
	PB1-PB-11		—	45	
	PA0=PA15, RXD1, RCLK1, TCKL1, $\overline{CD1}$, $\overline{CTS1}$, $\overline{CD3}$, $\overline{CTS3}$, $\overline{BR}$, AVEC		—	40	
Power		V_{DD}	4.5	5.5	V
Common		V_{SS}	0	0	V
Power Supply Current Drawn from Target System		I_{DD}	—	200	mA

Note 1 EXTAL and $\overline{AS}$ are additionally terminated with 100 ohm in series with 100 pF on the emulator.

AC electrical specifications

All specifications are the same as listed in the Motorola MC68302 User's Manual, except for the following:

Num	Characteristic	Min	Max	Unit
	Frequency of Operation	8	25	MHz
1	Clock Period (EXTAL)	40	125	ns
2,3	Clock Pulse Width (EXTAL)	19	62.5	ns
4,5	Clock Rise and Fall Times (EXTAL)	—	4	ns
5a	EXTAL to CLKO DelayNote 2	3.5	12	ns
6	Clock High to Address Valid	-5	28.5	ns
6	Clock High to FC Valid	-5	29	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	—	31.5	ns
8	Clock High to Address, FC Invalid	-5	—	ns
9	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	-2	19	ns
11	Address, FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted	10	—	ns
12	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	—	19	ns
13	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid	10	—	ns
14	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	80	—	ns
14A	$\overline{DS}$ Width Asserted (Write)	40	—	ns
15	$\overline{AS}$, $\overline{DS}$ Width Negated	40	—	ns
16	Clock High to Control Bus High Impedance	—	33	ns
17	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	10	—	ns
18	Clock High to R/$\overline{W}$ High	—	19	ns
20	Clock High to R/$\overline{W}$ Low	—	19	ns
20A	$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	—	7	ns
21	Address, FC Valid to R/$\overline{W}$ Low (Write)	10	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	20	—	ns
23	Clock Low to Data-Out Valid	—	19	ns
25	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid (Write)	10	—	ns
26	Data-Out Valid to $\overline{DS}$ Asserted (Write)	10	—	ns
27	Data-In Valid to Clock Low (Setup Time on Read)	10	—	ns
28	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold)	0	75	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	0	—	ns
31	$\overline{DTACK}$ Asserted to Data-In Valid (Setup Time)	—	33	ns
33	Clock High to $\overline{BG}$ Asserted	—	19	bs
34	Clock High to $\overline{BG}$ Negated	—	19	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High-Z ($\overline{AS}$ Negated)	—	33	ns
41	$\overline{BGACK}$ Asserted to $\overline{AS}$ Asserted	20	—	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{AVEC}$ Negated	0	33	ns
47	Asynchronous Input (Except $\overline{IPL0}$-$\overline{IPL2}$) Setup Time to Clock	12	—	ns
47	Asynchronous Input ($\overline{IPL0}$-$\overline{IPL2}$) Setup Time to Clock	30	—	ns
48	$\overline{BERR}$ Asserted to $\overline{DTACK}$ Asserted	7	—	ns
53	Clock High to Data-Out Invalid (Hold Time on Write)	-5	—	ns
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven$_{Note\ 3}$	1.5	—	clks
58	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven$_{Note\ 3}$	1.5	—	clks
60	Clock High to $\overline{BCLR}$ Asserted	—	18.5	ns
61	Clock High to $\overline{BCLR}$ High Impedance	—	18.5	ns
62	Clock Low (S0 Falling Edge During Read) to $\overline{RMC}$ Asserted	—	18.5	ns
63	Clock High (During Write) to $\overline{RMC}$ Negated	—	18.5	ns
64	$\overline{RMC}$ Negated to $\overline{BG}$ Asserted	—	20	ns
80	$\overline{REQ}$ Asynchronous Setup Time to Clock	15	—	ns
83	Clock High to $\overline{BR}$ Low	—	18.5	ns
84	Clock High to $\overline{BR}$ High Impedance	—	18.5	ns
85	$\overline{BGACK}$ Low to BR High Impedance	20	—	ns
86	Clock High to $\overline{BGACK}$ Low	—	18.5	ns
91	Clock High to $\overline{BGACK}$ High	—	18.5	ns
92	Clock Low to $\overline{BGACK}$ High Impedance	—	8.5	ns
93	Clock High to $\overline{DACK}$ Low	—	18.5	ns
94	Clock Low to $\overline{DACK}$ High	—	18.5	ns
95	Clock High to $\overline{DONE}$ Low (Output)	—	18.5	ns
96	Clock Low to $\overline{DONE}$ High Impedance	—	18.5	ns
97	$\overline{DONE}$ Input Low to Clock High (Asynchronous Setup)	15	—	ns
101	$\overline{DS}$ Low to Data-In Valid	—	20	ns

Num	Characteristic	Min	Max	Unit
105	DS High to DTACK High	—	30	ns
108	DS High to Data High Impedance	—	30	ns
109A	Data-Out Valid to DTACK Low	10	—	ns
110	Address Valid to AS Low	10	—	ns
111	AS Low to Clock High	25	—	ns
112	Clock Low to AS High	—	25	ns
113	AS High to Address Hold Time (Write)	0	—	ns
115	DS Low to Clock High	32	—	ns
116	Clock Low to DS High	—	25	ns
117	R/W Valid to Clock High	25	—	ns
118	Clock High to R/W High	—	25	ns
119	AS Low to IAC High	—	27	ns
120	AS High to IAC Low	—	27	ns
121	AS Low to DTACK Low (0 Wait States)	—	30	ns
122	Clock Low to DTACK Low (1 Wait State)	—	18.5	ns
123	AS High to DTACK High	—	30	ns
124	DTACK High to DTACK High Impedance	—	10	ns
125	Clock High to Data-Out Valid	—	18.5	ns
126	AS High to Data High Impedance	—	30	ns
130	Data-In Valid to Clock Low	25	—	ns
131	Clock Low to Data-In Hold Time	8.5	—	ns
140	Clock High to IAC High	—	25.5	ns
141	Clock Low to IAC Low	—	25.5	ns
142	Clock High to DTACK Low	—	28.5	ns
143	Clock Low to DTACK High	—	25.5	ns
144	Clock High to Data-Out Valid	—	19	ns
145	AS High to Data-Out Hold Time	0	—	ns
150	Clock High to CS, IACK7 Low	-5	26	ns
150	Clock Low to IACK1, IACK6 High	-5	25.5	ns
151	Clock Low to CS, IACK7 High	-5	26	ns
151	Clock Low to IACK1, IACK6 High	-5	25.5	ns
152	CS Width Negated	40	—	ns
153	Clock High to DTACK Low (0 Wait States)	—	28.5	ns
154	Clock High to DTACK Low (1-6 Wait States)	—	18.5	ns
155	Clock Low to DTACK High	—	25.5	ns
156	Clock High to BERR Low	—	25.5	ns
157	Clock Low to BERR High Impedance	—	25.5	ns
158	DTACK High to DTACK High Impedance	—	10	ns
160	AS Low to CS Low	—	20	ns
161	AS High to CS High	—	20	ns
162	Address Valid to AS Low	10	—	ns
163	R/W to AS Low	10	—	ns
165	AS Low to DTACK Low (0 Wait States)	—	30	ns
167	AS High to DTACK High	—	20	ns
168	AS Low to BERR Low	—	20	ns
169	AS High to BERR High Impedance	—	20	ns
171	Clock Low (end to S6) to Data-In Invalid (Hold Time on Read)	3.5	—	ns
172	CS Negated to Data-Out Invalid (Write)	7	—	ns
173	Address, FC Valid to CS Asserted	15	—	ns
174	CS Negated to Address, FC Invalid	12	—	ns
175	CS Low Time (0 Wait States)	80	—	ns
176	CS Negated to R/W Invalid	7	—	ns
177	CS Negated to R/W Low (Write)	—	8	ns
178	CS Negated to Data-In Invalid (Hold Time on Read)	0	—	ns
180	Input Data Setup Time to Clock Low	19	—	ns
181	Clock Low to Input Data Hold Time	17.5	—	ns
182	Clock High to Data-Out Valid (CPU Writes Data, Control, or Direction)	—	22.5	ns
190	Interrupt Pulse Width Low IRQ (Edge Triggered Mode)	34	—	ns
204	Clock High to TOUT Valid	—	22.5	ns
205	FRZ Input Setup Time to Clock High	29	—	ns
206	Clock High to FRZ Input Hold Time	4.5	—	ns

Note 2 CLCKO skew from the rising and falling edges of EXTAL will not differ from each other by more than 2.5 ns, if the EXTAL rise time equals the EXTAL fall time.

Note 3 If bus arbitration occurs while in the background monitor this value is 0.5 clks.

Ordering Information

HEWLETT® PACKARD

Terminal-Based Emulation System

Model	Description
64798C	25 MHz active probe emulator for 68302 PQFP and TQFP processors (includes demo board)
64748C	Emulation control card
64794A	8K deep 80-channel emulation bus analyzer
64700B	Cardcage

Emulation System Options

64171A	256 Kbyte, SRAM memory module (35 ns)
64171B	1 Mbyte, SRAM memory module (35 ns)
64172A	256 Kbyte, SRAM memory module (20 ns)
64172B	1 Mbyte, SRAM memory module (20 ns)
64173A	4 Mbyte, SRAM memory module (25 ns)
64708A	Software performance analyzer card, (supported on HP 9000 Series workstations, and Sun SPARCstations, HP B1487A software, required)
64023A	CMB cable (4m long; includes three 9-pin connectors)
64794C	64K deep 80-channel emulation bus analyzer
64794D	256K deep 80-channel emulation bus analyzer
E5336A	144-pin TQFP probe adapter
E5338A	144-pin TQFP flex cable
E5367A	PGA adapter kit
E3437A	132-pin PQFP adapter kit
E3439A	144-pin TQFP transition bd for HP64746A
64798CY	68302 emulator bundle

Software Options for Workstations

For each software model number ordered, purchase one media option and at least one license option for each concurrent user.

B3093B	Graphical emulator/analyzer
B1487A	Software performance analyzer (requires HP 64708A analyzer card)

Software Options for PCs

B3638A	Real-time C debugger interface

Software Support

HP provides software upgrades through the purchase of the software materials subscription (SMS) service. Contact your HP field engineer for more information.

* Contact your HP 64000 Field Engineer for the latest configuration information, supported processor speeds, and software options.

For more information on Hewlett-Packard Test & Measurement products, applications or services please call your local Hewlett-Packard sales offices. A current listing is available via Web through Access HP at http://www.hp.com/go/emulator If you do not have access to the internet please contact one of the HP centers listed below and they will direct you to your nearest HP representative.

United States:
Hewlett-Packard Company Test and Measurement Organization
5301 Stevens Creek Blvd.
Bldg. 51L-SC
Santa Clara, CA 95052-8059
1 800 452 4844

Canada:
Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario
L4W 5G1
(905) 206 4725

Europe:
Hewlett-Packard
European Marketing Centre
P.O. Box 999
1180 AZ Amstelveen
The Netherlands

Japan:
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