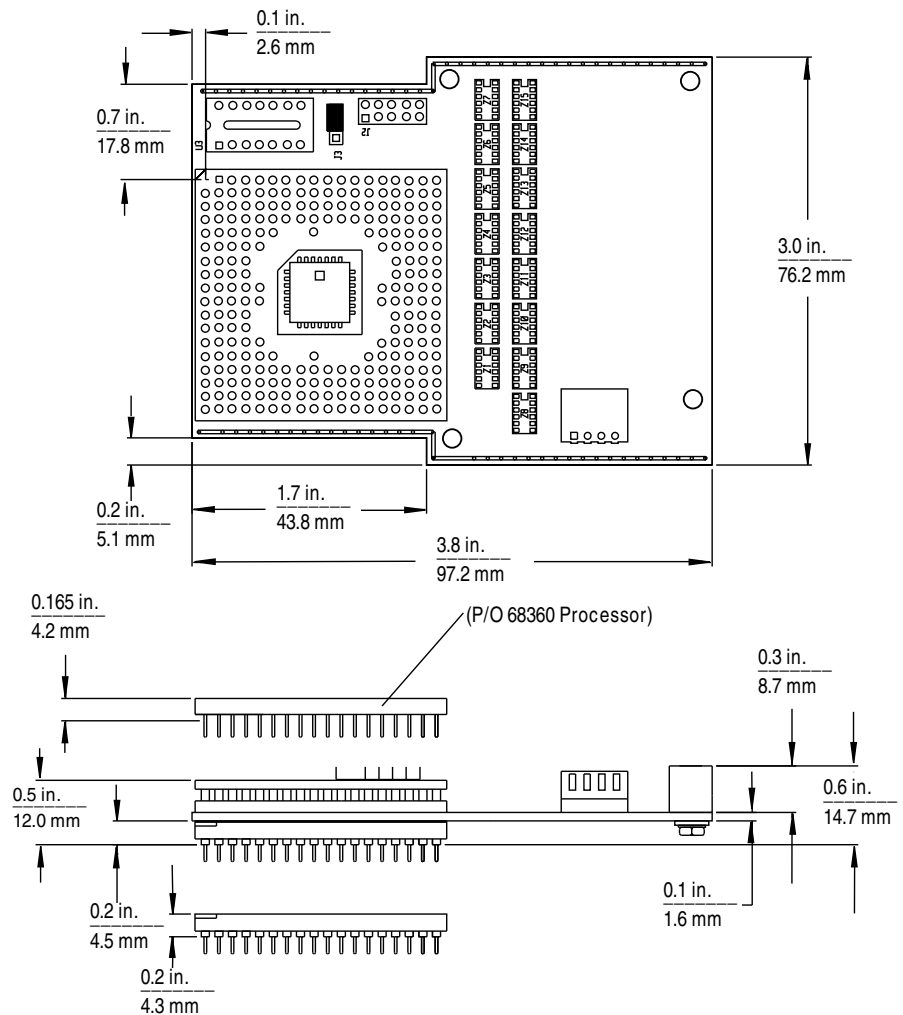


HP E2448A

Motorola 68360 (QUICC) Preprocessor Interface

For use with
HP logic analyzers

The Hewlett-Packard E2448A preprocessor interface provides an easy way to connect an HP logic analyzer to a target system using the Motorola 68360 (QUICC) microprocessor. For example, all necessary clocks are passed through by the preprocessor to the logic analyzer, ensuring that data is captured at the correct time. In addition, software is shipped with the product that automatically configures the logic analyzer, generating labels for address, data, and status signals. Included with the software is a disassembler that displays execution traces in 68360 microprocessor mnemonics. Instructions that are prefetched but not executed are marked in the trace display, or can be suppressed entirely. Additionally, a 10-pin Background Debug Mode (BDM) connector provides connection to a BDM debugger.



Key Specifications:

Timing Analysis:

All M68360 signals, except for the PLL and crystal control signals, are connected to the logic analyzer directly for unbuffered timing analysis. The signals excluded are EXTAL, XFC, and XTAL.

Pods Required:

The preprocessor uses 11 logic analyzer pods. Six are required for inverse assembly. An additional five are provided for state and timing analysis of additional signals on the microprocessor.

Termination Adapters (TAs):

None are required, as the connectors are terminated on the preprocessor.

Logic Analyzers Supported:

One-card HP 16550A in an HP 16500B mainframe for inverse assembly only, or a two-card HP 16550A for full state and timing analysis. In addition, the HP 1661A or HP 1660A are supported for inverse assembly only.

Processors Supported:

68360A 241-pin PGA and 240-pin PQFP (requires one additional adapter, HP E5317A).

Maximum Clock Speed:

33 MHz.

Signal Line Loading:

25 pF in parallel with 100 k Ω to V_{ss} for AS, DS, and CLK01.

25 pF in parallel with 10 k Ω to V_{dd} for FREEZE, BCLR0, RMC, TRIS, MODCK1, and MODCK0.

15 pF in parallel with 100 k Ω to V_{ss} for all others.

Target Signal Timing:

Adjustable from 3.5 ns setup/0 s hold to 0 s setup/3.5 ns hold.

Microprocessor Operations Displayed:

All cycles with AS asserted.

All cycles with DS asserted.

All show cycles (address and data).

Additional Capabilities:

The logic analyzer captures all bus cycles, including prefetches. Unexecuted prefetches are marked with a hyphen (-) or question mark (?).

For more information, call your local HP sales office listed in your telephone directory, or an HP regional office listed below for the location of your nearest sales office.

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Santa Clara, CA 95052-8059
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