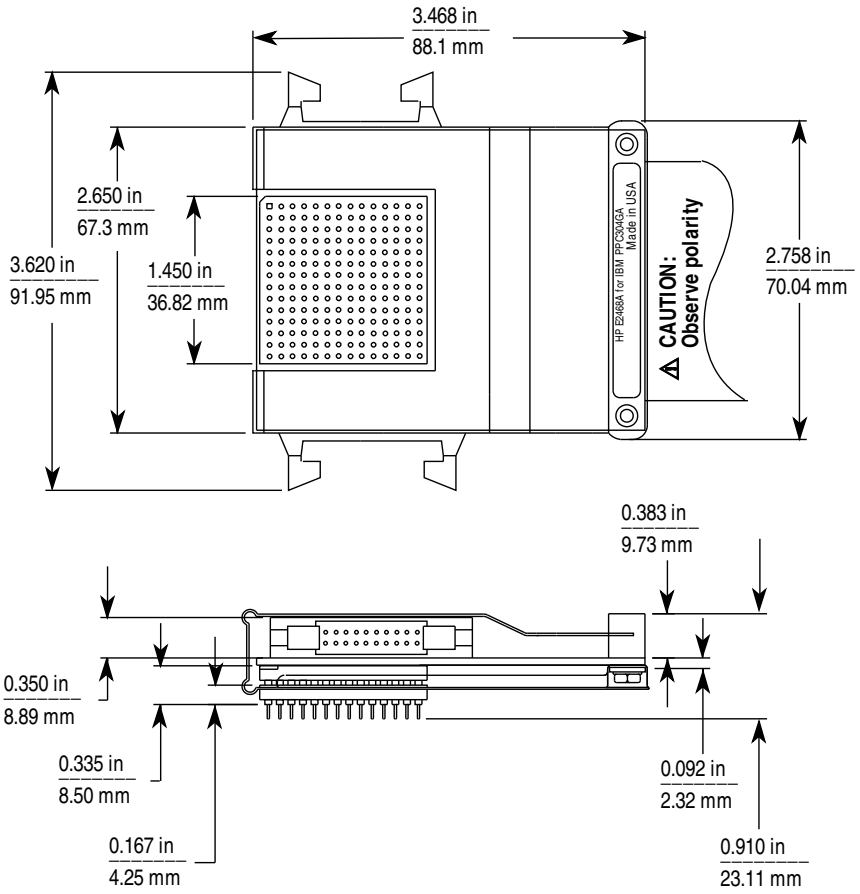
HP E2468A

Preprocessor Interface for the IBM PowerPC 403GA

For use with HP logic analyzers

The Hewlett-Packard E2468A preprocessor interface provides an easy way to connect a Hewlett-Packard logic analyzer to a target system using the IBM PowerPC 403GA microprocessor. All necessary clocks are passed through by the preprocessor to the logic analyzer, ensuring that data is captured at the correct time. Software is shipped with the product that automatically configures the logic analyzer, generating labels for address, data, and status signals. Included with the software is a disassembler which displays execution traces in PowerPC 403GA microprocessor mnemonics. Instructions which are pre-fetched but not executed are marked in the trace display. Three modes of operation are available to the user: state-per-clock, which provides a complete display of all bus activity; state-per-transfer, which filters out wait and idle states; and timing analysis up to 500 MHz. Channel to channel skew is 1 ns.



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Key Specifications

Inverse Assembler Features
All processor instructions are supported. In addition, disassembly is synchronized at branch addresses.

State Per Transfer Mode
In this mode, the logic analyzer records only those states in which the strobe (IOTV, TS6) is asserted. This mode filters wait and idle states.

State Per Clock Mode
When using this mode, address and data are captured on each CPU clock. This feature is useful in hardware validation and debugging of system crashes.

Timing Mode
All address, data and status lines are labeled on the logic analyzer display when making accurate timing measurements.

Logic Analyzers Supported
HP 16550A (1 required)
HP 16554A, HP 16555A , HP 16556A (2 required)
HP 1660A, 1661A

Number of Probes Required
Five, sixteen-channel probes are required for complete state disassembly. An additional three probes will monitor the remainder of the signal pins for timing measurements.

Target Signal Timing
Data must be valid for a 3.5 ns window with respect to the logic analyzer clock, which strobes the data into the logic analyzer on the rising edge.

Termination Required
No user-supplied termination is necessary as the logic analyzer probes are terminated on the preprocessor.

Evaluation Board Compatibility
The IBM Microelectronics' PowerPC 403GA Evaluation Board, which includes 20-pin termination headers for an HP logic analyzer, is supported by the 403GA configuration file of the E2468A.

Processor Supported
IBM PowerPC 403GA in a 160-pin PQFP package up to 50 MHz.
Note: HP E5335A PQFP adapter is required to probe the 160-pin PQFP package.

Signal Line Loading
10 pF and 100 kΩ on all signals.

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