# HP E2972A PCI Performance Analyzer

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## Technical Specifications

**HP E2920 Computer Verification Tools, PCI Series**

Part of the HP E2920 PCI Series of Computer Verification Tools, the HP E2972A PCI Performance Analyzer is an exhaustive solution, which, in conjunction with the HP E2925A, can easily evaluate and analyze PCI system performance in depth, so that PCI systems and components are optimized.

### From Simple Performance Evaluation to In-Depth Analysis

Allowing real-time measurements and in-depth post-processing, the HP E2972A PCI Performance Analyzer performs high quality measurements of PCI-based systems and cards, ranging from first level performance evaluation and comparison to in-depth performance analysis. Results can be easily compared and communicated by using the extensive performance measurement metrics. In comparison with

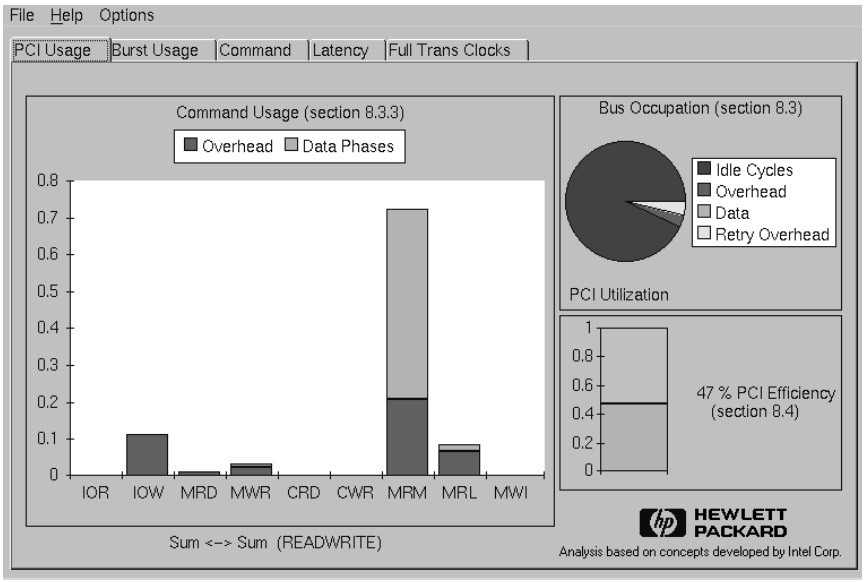


**Figure 1. Performance overview chart**

### Key Features

- In-depth performance analysis through post-processing.
- 1 M sample trace memory.
- Differential storage qualifier to optimize trace memory usage.
- Four real-time counters with virtual infinite counter depth.
- Additional reference counter.
- Advanced, ready-to-run real-time measures for:
  – PCI efficiency,
  – PCI throughput,
  – PCI initialization,
  – retry rate.
- Latency measurement.
- First word latency of split transaction (PCI spec 2.1).
- Activity lister with time stamp.
- Reveals target, master, and arbiter contribution to performance measurement results.
- Measures overall traffic and selective for master/target pair.
- Report generation.
- Cross-references to HP E2970A PCI Analyzer Graphical User Interface.

running software benchmarks, which detail how a user application will perform on a system, the HP E2972A provides an "inside view", instructing design engineers how to optimize PCI systems, cards and chip sets.

**Optimize system performance**
By following the PCI performance measurement metrics, system integrators can easily select the best PCI cards and components, detect and locate PCI performance bottlenecks, and balance BIOS settings so that the overall performance of the system is optimized.

**Optimize PCI System Components**
For PCI chip, card and system designers, the HP E2972A is designed to verify, optimize and document PCI performance. Therefore, the HP E2972A uses a hierarchical approach to analyze real-time and post-processing performance measurements. This means that the HP E2972A moves swiftly from high-level throughput numbers to, for example, PCI command usage and latency measurements, as required. It is therefore simple to identify design issues and analyze their causes. Overall, this approach reduces the effort required in revealing design problems.

## Real-Time Measurement and Post-Processing

The HP E2972A carries out real-time performance measurements and concurrently takes a bus snapshot for exhaustive analysis. So, while monitoring performance over seconds or hours, a valid sample is taken for closer analysis so that performance issues can be identified.

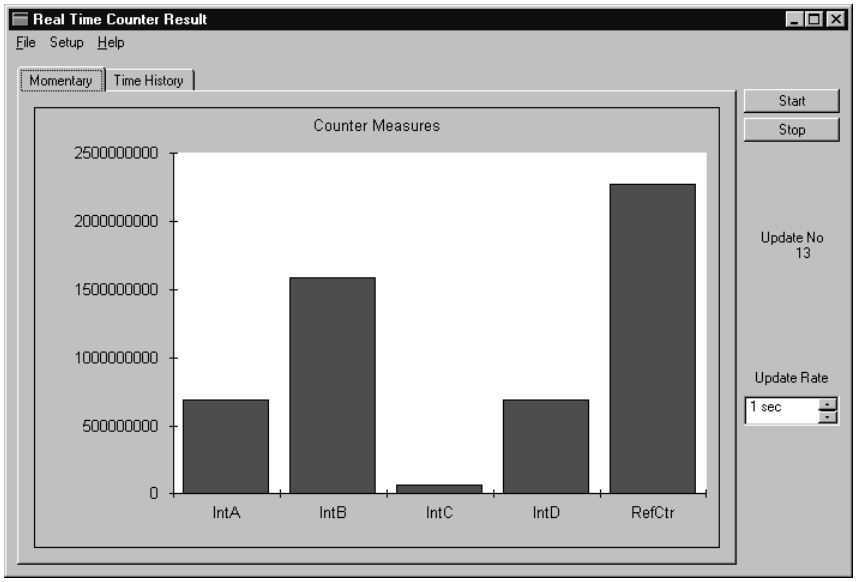


**Figure 2. Real-time counting**

## Real-Time Measurements

To perform the usual single event counting, the HP E2972A supports up to four virtual, infinite counters plus one reference counter.

Taking it a step further, the HP E2972A also offers four advanced, ready-to-run real-time measurements:

- PCI efficiency,
- PCI throughput,
- PCI utilization,
- retry rate.

Each measurement utilizes two real-time counters (nominator and denominator) and can be set up to analyze the complete PCI bus, a single master or a single target. Measurements can be started and stopped by customer-specified bus patterns. Two measurements can be performed simultaneously.

An advanced setup mode (using the trigger sequencer) allows customized, real-time measurements to be defined.

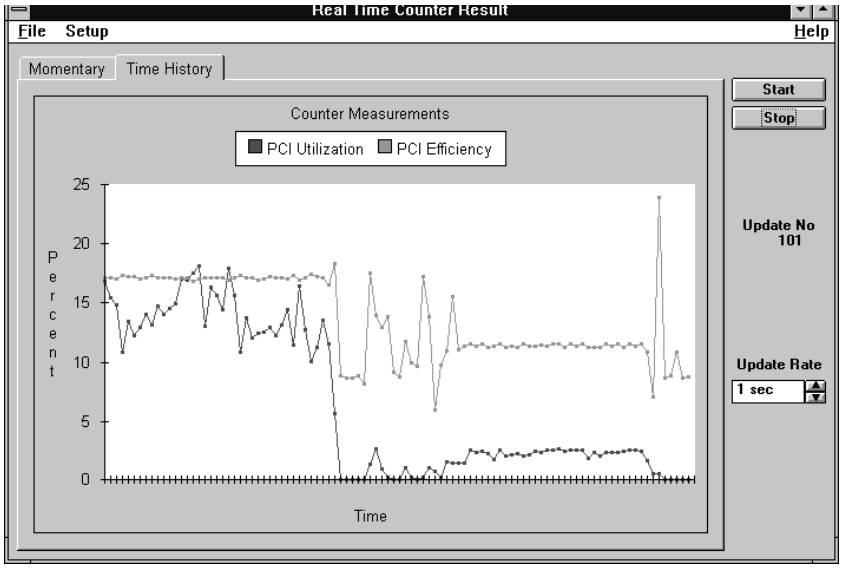


**Figure 3. Real-time measures**

Real-time measurements are presented graphically, either as a cumulative bar chart or as a trend chart showing the last 100 measurement intervals. These intervals range from 1 to 120 seconds. A tabular representation is also part of the report file.

## Post-Processed Data Analysis

The HP E2972A carries out an in-depth performance analysis of sampled PCI transactions by using the HP E2925A 1 M memory/ performance board option to acquire data. To optimize the 1 M of trace memory, the differential storage qualifier is set up to automatically select the data needed for the performance measurement.

**Basic bus statistics**
To obtain an overall picture of the PCI performance, the HP E2972A analyzes the PCI bus for:

- PCI throughput,
- PCI utilization,
- non-retry utilization,
- PCI efficiency,
- PCI non-retry efficiency,
- PCI data efficiency,
- retry overhead.

A bus efficiency chart provides an overview of how efficiently the traffic was handled between different bus agents.

**Bus utilization**
The bus utilization analysis shows how the PCI bus was used by:

- data transfer,
- overhead,
- retry.

A utilization chart shows how the bus was used by the different bus agents.

**Interrupt latency**
Interrupt latencies are evaluated in detail by measuring:

- average interrupt latency; individually for INT A, B, C, D.
- overall interrupt latency; calculates the interrupt latency as a weighted average of INT A, B, C, and D.

An interrupt latency histogram shows the distribution of the individual interrupts over clock cycles.

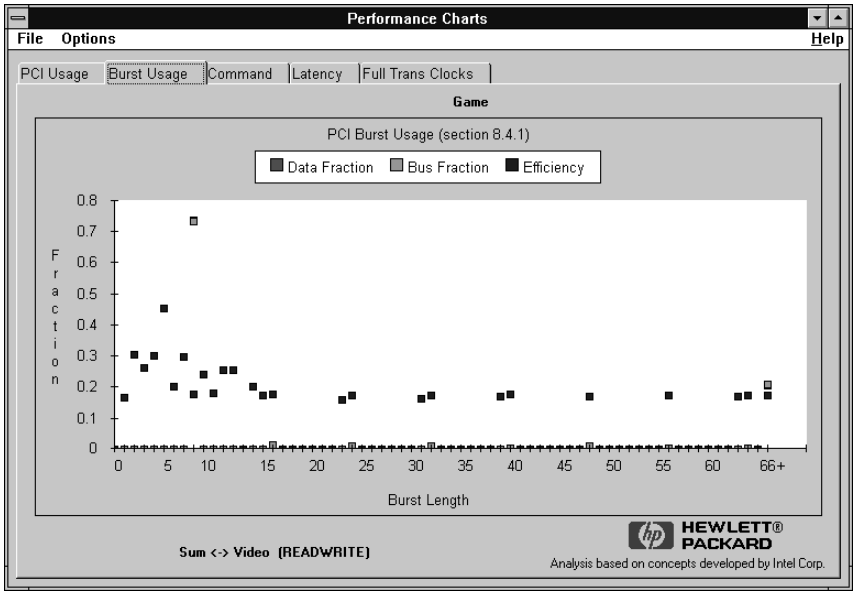


**Figure 4. Burst usage**

## Master/Target Performance

Post-processing allows the analysis of customer-selected master/target combinations so that specific master/target performance behavior can be analyzed in depth. By evaluating the critical agents using the real-time measurements and basic bus statistics, the in-depth master/target analysis provides an "inside view" of how to optimize single agents.

**Master/target bus usage**
The bus usage measurements show:

- Master was waiting for GNT# but bus was idle.
- Master was waiting for GNT# but bus was busy.
- Bus occupation by selected master/target, split into retry overhead, transfer overhead and data phases.
- Data phase statistics, showing the distribution of byte enable 1, 2, 3, or 4.
- Average byte enable efficiency.
- Average decode speed.

**Wait cycle histogram**
A wait cycle histogram shows wait cycles caused by the master and target.

**Burst length distribution**
As well as displaying the average overall burst length, this histogram also shows the distribution of burst length over PCI commands. Again, this provides an "inside view" into performance bottlenecks in PCI systems.

**Command usage chart**
The command usage chart lists the usage of different PCI commands so that performance issues caused by inefficient command usage are revealed.

**Master/target efficiency**
A further important indication for PCI system performance is how efficiently a certain master/target pair uses the occupied bus time. Thus, the HP E2972A examines:

- master/target overall efficiency of transferred data,
- non-retry efficiency,
- efficiency over burst length.

**Termination statistics**
The PCI termination statistics indicate:

- average number of retries needed,
- termination by arbiter in favor of other bus agents,
- termination over burst length.

**Latency distribution**
This histogram shows the following (over clock cycles):

- first word latency,
- average latency,
- arbiter latency,
- bus access latency,
- first word retry.

## Report and Result ASCII File

All results are available as an ASCII report file for further analysis and customer post-processing.

The different segments are:

1 GENERAL INFORMATION
1.1 Test Settings
1.2 Statistical Base

2 BASIC BUS STATISTICS

3 BUS THROUGHPUT STATISTICS

Hewlett-Packard HP E2972A PCI Performance Analyzer SW (W3.22.15)
Analysis based on concepts developed by Intel Corporation
Statistical Report File
Date: 06/18 at 17:28 h

1.2 Statistical Base
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| | |
|---|---|
| Test covered | 1228225 clocks |
| Test covered | 0.03721894 sec |
| No. of captured address cycles | 152215 clocks |
| No. of captured data cycles | 8882 clocks |
| Bytes transferred | 35489 bytes |
| No. of Interrupts occurred | 0 |

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2 BASIC BUS STATISTICS
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| | |
|---|---|
| PCI Throughput | 0.9535 Megabytes/sec |
| | 7.6282 Megabits/sec |
| PCI Utilization | 50.07 % |
| Non-retry PCI Utilization | 3.60 % |
| PCI Efficiency | 1.44 % |
| Non-retry PCI Efficiency | 20.09 % |

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4 EFFICIENCY STATISTICS
==========

| | |
|---|---|
| PCI Byte Enable Efficiency | 99.89 % |
| PCI Time Efficiency | 1.44 % |
| Non-retry PCI Time Efficiency | 20.11 % |
| Retry Overhead = Non-retry Time Efficiency - PCI Time Eff. | 18.66 % |

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5 BUS UTILIZATION STATISTICS
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| | |
|---|---|
| Overhead Utilization | 2.87 % |
| Retry Overhead | 46.47 % |
| Data Utilization | 0.72 % |

8.3.2 Time Overhead
---
Average Decode Speed (1 == fast .... 2.00 cycle(s)

| | Overhead caused by Master | Target | Both | Sum |
|---|---|---|---|---|
| a) Address Phase | 1.46 % | — | — | 1.46 % |
| b) Waits | 0.00 % | 1.51 % | 0.00 % | 1.51 % |
| 1) First Word Latency (a+b) | 1.46 % | 1.51 % | 0.00 % | 2.97 % |
| 2) Retry Transactions | — | 94.18 % | — | 94.18 % |
| 3) Subsequent Latency | 0.00 % | 2.85 % | 0.00 % | 2.85 % |
| Sum ((1) + (2) + (3)) | 1.46 % | 98.54 % | 0.00 % | 100.00 % |

**Figure 5. ASCII report file (extract)**

4 EFFICIENCY STATISTICS
4.1 Master Target Efficiency

5 BUS UTILIZATION STATISTICS
5.1 Master Target Utilization

6 BUS USERS OVERVIEW

7 INTERRUPT STATISTICS
7.1 Interrupt Latency Histogram

8 MASTER - TARGET PAIR: All Masters <-> All Targets (Read Write)
8.1 Statistical Basis
8.2 Bus Usage
8.3 Bus Occupation
8.3.1 Data Phase
8.3.2 Time Overhead
8.3.3 Command Usage
8.3.4 Command Termination
8.3.5 Wait Histogram
8.3.6 Burst Length over Command
8.4 Efficiency Statistics
8.4.1 Efficiency over Burstlength
8.5 Termination Statistics
8.5.1 Termination Burst Histogram
8.6 Latency Histogram

However, please note that the ASCII report and result file (Figure 5) is only an extract of a full report, and complete information on this topic is available in the User Manuals Section on the www at http://www-europe.hp.com/dvt/product/E2925A/Listlit.htm

## Measurement and Resource Requirements

The HP E2972A PCI Performance Analyzer requires the HP E2925A PCI Exerciser and Analyzer with option 100 1 M memory/ performance board and option 002 fast host interface. If master identification is needed, the GNT# and REQ# lines of the PCI bus must be connected to the HP E2925A option 100 trigger input lines. GNT# lines must be connected for latency measurements. The target is identified by the user-specified target decode address.

## System Requirements

To use the HP E2972A PCI Performance Analyzer, a PC with the following specifications is required.

**PC**: IBM-PC or 100 % compatible, with recommended minimum 90 MHz Pentium CPU and CD-ROM drive.

**Graphics**: 800 x 600 required, 1024 x 768 SVGA recommended.

**O/S**: Windows 95, Windows NT rev. 3.51 or Windows NT 4.0.

**Memory**: 24 MB minimum, 32 MB recommended (for the complete HP E2920 Series).

**Hard disk**: minimum 50 MB available disk space required, 100 MB recommended (for the complete HP E2920 Series).

**Interfaces**: A parallel port is required for the software ID module supplied with the HP E2925A.

**Expansion slots**: for the HP E2925A option 002 fast host interface of the PCI Exerciser and Analyzer Card, one ISA slot is required to host the bi-directional Centronics card.

## Ordering Information

The HP E2972A includes:

- license to use the PCI Analyzer GUI software with a single PCI exerciser and analyzer card,
- software media (CD-ROM).

The HP E2972A requires:

- HP E2925A PCI Exerciser and Analyzer,
- HP E2925A option 100 1 M deep trace memory/performance board,
- HP E2925A option 002 fast host interface (recommended).

## Related HP Literature

- HP E2920 Computer Verification Tools, PCI Series, brochure, p/n 5965-4723E.
- HP E2925A 32 bit, 33 MHz PCI Exerciser and Analyzer, technical specifications, p/n 5965-4724E.
- HP E2970A PCI Analyzer Graphical User Interface for Windows 95/NT, p/n 5965-4726E.
- HP E2971A PCI Exerciser Graphical User Interface for Windows 95/NT, technical specifications, p/n 5965-4725E.
- HP E2974A Sub-System Stress Tests, technical specifications, p/n 5965-8009E.
- HP E2975A PCI Protocol Permutator and Randomizer, technical specifications, p/n 5965-8010E.

**Additional literature**

- 'Efficient Use of PCI' Frank Hady, Intel. Available on the www: http://www-europe.hp.com/dvt/applic/applic.htm#BusExercisers

For more information:
http://www-europe.hp.com/dvt

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