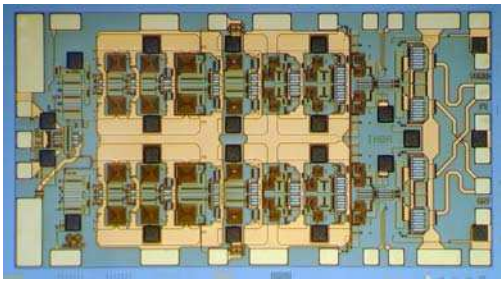
Agilent 1GG6-8083
250–8000 MHz MMIC
Low Distortion IQ Modulator

TC932
Data Sheet



Features

- **Broadband: 250 - 8000 MHz**
- **High Linearity: -74 dBc ACLR (4-carrier WCDMA, 2 GHz)**
- **Low +8 dBm LO Drive**

Chip Size: 2,600 x 1,370 µm (102.4 x 53.9 mils)
Chip Size Tolerance: ± 10 µm (± 0.4 mils)
Chip Thickness: 127 ± 15 µm (5.0 ± 0.6 mils)
Pad Dimensions: 80 x 80 µm (3.2 x 3.2 mils)-smallest

Description

The TC932 is a broadband IQ modulator designed for instrumentation applications. The LO input is vector–modulated in response to differential signals into the I and Q ports. The differential outputs may be combined with a balun for better output power, carrier rejection, and dynamic range.

The TC932 is also available in a 14–lead "Fastpak II" surface mount package.

Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Min.	Max.	Units
V_{ss}	Negative Supply Voltage	–6.1	0	Volts
V_{blo}	Mixer Bias Voltage	–5	+2	Volts
V_{ci},V_{cq}	I and Q Channel Phase Control Voltage	–5	+2	Volts
VI, VI_{bar} VQ,VQ_{bar}	I and Q Input Voltages	–1	+1	Volts
I_{di},I_{dq}	Detector Diode Bias Current		125	uA
V_{in}	DC Voltage on LOinput	–2	+2	Volts
P_{LO}	Total LO Input Power		+18	dBm
T_{ch}	Operating Channel Temp.		150	°C
T_{stg}	Storage Temperature	–65	165	°C
T_{max}	Maximum Assembly Temp. (for 60 seconds maximum)		300	°C

Notes:

1. Operation excess of any one of these ratings may result in permanent damage to this device. T_A=25°C except for T_{op}, T_{st}, and T_{max}.

DC Specifications/Physical Properties[1]

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
V_{ss}	Supply Voltage	–6.1	–6.0	–5.9	Volts
I_{ss}	Supply Current	800	970	1100	mA
V_{out1} V_{out2}	Output Node Bias Voltage	–0.1	0.0	0.1	Volts
I_{out1} I_{out2}	Output Bias Current		140		mA
V_c	Quadrature Coarse Adjust Control Voltage (average of V_{ci} and V_{cq}, set by external DC feedback loop to equalize V_{Di} and V_{Dq})	–2.0		+1	Volts
$V_{ci} – V_{cq}$	Quadrature Fine Adjust (aka "Torque")	–0.4	–0	+0.4	Volts
I_{Di} I_{Dq}	Detector Diode Bias Current	45	50	55	uA
V_{Di} V_{Dq}	Detector Voltage (LO off)		+0.9		Volts
dV_{Di} dV_{Dq}	Detected Voltage (= $Vd_{LO\ on} – Vd_{LO\ off}$)[2]	-1.5	–0.6	-0.17	Volts
V_{blo}	Mixer Bias Voltage	-2.5	–1.4	0	Volts
RL_{Di} RL_{Dq}	Resistive Load on Di and Dq		100k		ohms

Notes:

1. Evaluation PCB includes backside heatsink and fan.
2. LO = 10dBm

RF Specifications

Symbol	Parameters/Conditions	Min.	Typ.	Max.	Units
f	Frequency Range	250		8000	MHz
P_{LO}	LO Input Power	8	8	13	dBm
RL_{LO}	LO Port Return Loss		–15	–10	dB

RF Specifications (includes output balun)

Parameter	Min.	Typ.	Min.	Typ.	Min.	Typ.	Units
Frequency Range	250-1000		1000-3000		3000-6000		MHz
Output IP3		+32		+34		+27	dBm
Output ACPR (Test Model 1 with 64 channels)		65		73		71	dBc
Output Power (at output ACPR above)		-24		-17		-20	dBm

Applications

The TC932 adds accurate vector modulation to broadband signal sources.

Biasing and Operation

Overview

TC932 operation requires a single –6V power supply ("V_{ss}"), and other biases and adjustments as shown in Figure 1. Two 50 uA current sources bias internal detector diodes. A negative feedback loop automatically sets coarse quadrature and stabilizes gain ratio and quadrature against time and temperature. V_{blo} optimizes mixer linearity. There are also four adjustments which are frequency dependent:

1. V_{ci}–V_{cq}: Fine adjustment of quadrature.
2. I (or Q) Gain: To compensate for slight channel conversion efficiency differences.
3. I channel offset: A small dc offset to cancel in-phase carrier leakage paths to the output.
4. Q channel offset: A small dc offset to cancel quadrature carrier leakage paths to the output.

Values for the above four should be determined during calibration.

TC732's 50 dB gain LO amplifiers reduce drive requirement to +8 dBm for low LO leakage, while maintaining large, fast-edged squarewaves at the mixers' LO ports. An output balun's common-mode rejection further improves LO feedthru.

An output balun provides up to 6 dB more output signal power with only about 3 dB more noise output power (since the noise is mostly uncorrelated).

A V_{ss} bypass capacitor of 0.1 uF should be placed on the PCB as close as possible to the TC932 package, and no more than 5 mm away.

Note that the TC932 output is close to a square wave, containing strong harmonic content at odd multiples of the LO frequency. External filtration is required if these harmonics are unacceptable.

Package

The TC932 is also avaiable in a 14-lead "Fastpak II" surface mount package.

Baseband ports

The baseband I and Q inputs connect directly to the sources of the passive bridge mixer FETs. There are also on-chip 50ohm resistors to ground on each port. Port input impedance changes slightly as a function of V_{blo} and frequency. Input impedance is mostly 50 ohms and

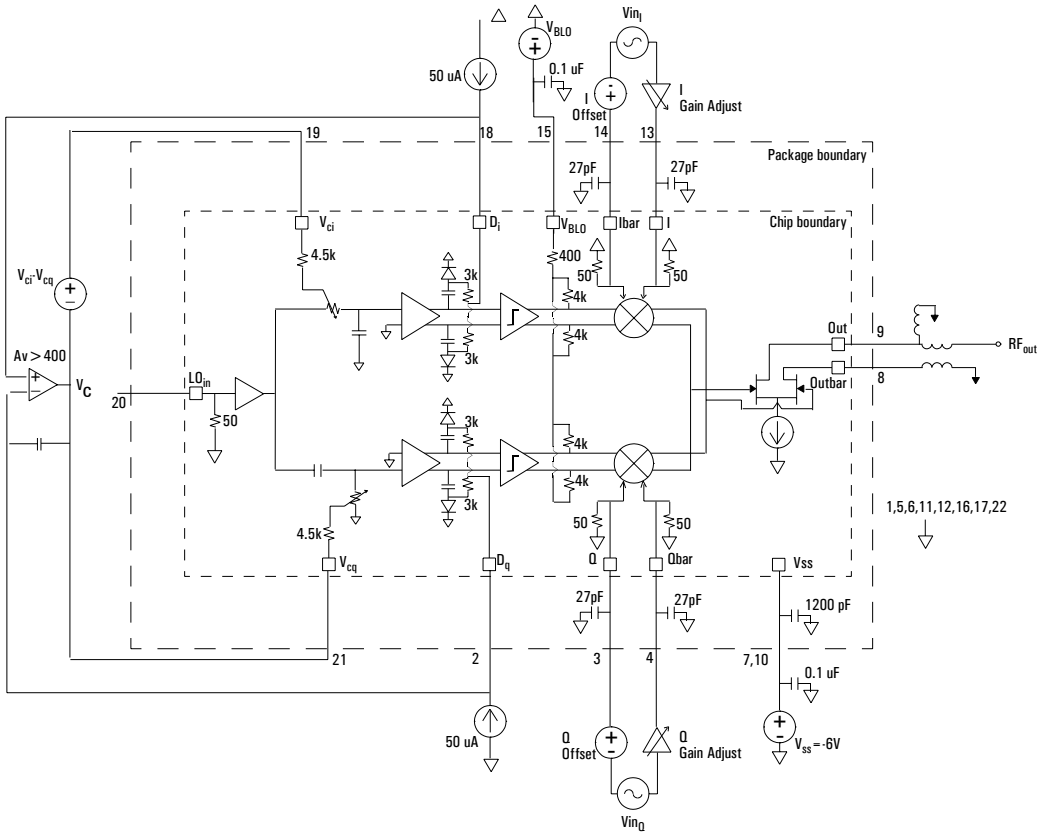


Figure 1.
TC932 Electrical Control Diagram

about 100 fF of capacitance in parallel, but can drop as either V_{blo} is adjusted more positive and/or as RF frequency increases. This happens because the mixer FETs are spending larger fractions of their time turned on as V_{blo} becomes more positive, or the mixer FETs are spending larger fractions of their time in intermediate states between full-on and pinched-off as frequency increases, respectively.

Impulsive waveforms at twice the LO frequency exist common-mode at the baseband ports because of the asymmetrical turn-on/turn-off characteristics of the mixer FETs. These even-harmonic-rich waveforms could upset DC levels and/or cause response ripples without preventative steps. 27pF bypass caps are included within the package to address this problem, albeit limiting modulation bandwidth to approximately 200 MHz.

Diode Biasing

The 50uA detector bias current supplies must be able to source into +1V. 180kohm resistors to +10V have been successfully used in practice.

Optimum V_{BLO} for Linearity

The VBLO quoted herein refers to a programmable DAC's Thevenin equivalent voltage, and includes a series 7.8 kohm source resistor.

Optimum V_{BLO} ("Voltage, Bias, Local Oscillator") for linearity varies as FET pinchoff voltage varies over process.

Optimum V_{BLO} for TOI at different frequencies is shown in Fig. 9. The historical TC733 method of utilizing the tight correlation between V_{BLO}-for-best-P_{out} and V_{BLO}-for-best-linearity isn't useful for TC932 since linearity varies significantly with V_{BLO} while P_{out} remains flat. The difference between TC733 and TC932 is the much more precise square-waves at the mixers even at highest frequencies. Adjusting VBLO for best linearity thus requires monitoring some linearity figure of merit.

It has been found that linearity is influenced by V_{BLO} source impedance. At 0.1uF bypass cap should be included on the V_{BLO} line near the package.

Assembly

Epoxy die-attach using conductive epoxy or solder die-attach using a fluxless AuSu Solder preform can be used for assembly. Gold thermosonic wedge bonding with 0.7 mil diameter gold wire is recommended for all bonds. Tool force should be 22 ± 1 gram, stage temperature should be 150 ± 2°C, and ultrasonic power and dduration should be 64 ± 1 dB and 76 ± 8 mse, respectively. The bonding pad and chip backside metallization is gold.

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. Agilent application note #54, "GaAs MMIC ESD, Die Attach and Bonding Guidelines" provides basic information on these subjects.

Test Fixture

The specifications and graphs herein were generated using two different evaluation PCBs. The first PCB (Fig. 13) includes a distributed 250-6000 MHz output balun, representative of typical use. The balun resonances at about 8000 MHz causing some anomolies in the output-referred data.

The second PCB (Fig. 14) does not have a balun and is used for single-output measurements.

Output Noise Special Case

Warning

Under typical operating conditions output noise is a relatively benign -160 dBm/Hz. A special case exists however where if 1. LO input power is removed, and 2. Vblo is near the FET threshold (typically about -1.4V) and 3. at least a few mVDC of baseband input, then the high levels of noise at the mixer LO inputs (recall that the LO amps have 50 dB of gain) can pass to the output, causing a dramatic rise in output noise. Thus, if LO power is removed, VBLO should also be taken to some extreme such as 0 or -3Vdc to prevent amplified LO noise from switching the mixer FETs.

Post-calibration stability

The feedback loop serves to maintain equal LO drives to the mixers. Benefit are that gain ratio and phase angle are desensitized to the effects of disturbance inputs such as temperature change or aging. See A. Teetzel, "A Stable 250-4000 MHz GaAs IQ Modulator IC", ISSCC97

LO feedthrough (i.e. "offsets") is unfortunately not stabilized by the feedback loop.

Post-calibration stability can be compromised if LO input harmonic content varies with time and/or temperature (see, for example, the TC733 datasheet). LO harmonic energy passes more readily thru the highpass Q phaseshifter than the lowpass I phaseshifter, so a LO harmonic change effects the detector in the Q-channel more than the I-channel and upsets the calibration. Also, LO harmonic content that fluctuates versus frequency can cause similarly fluctuating calibration coefficients, upsetting the otherwise smooth calibration curves.

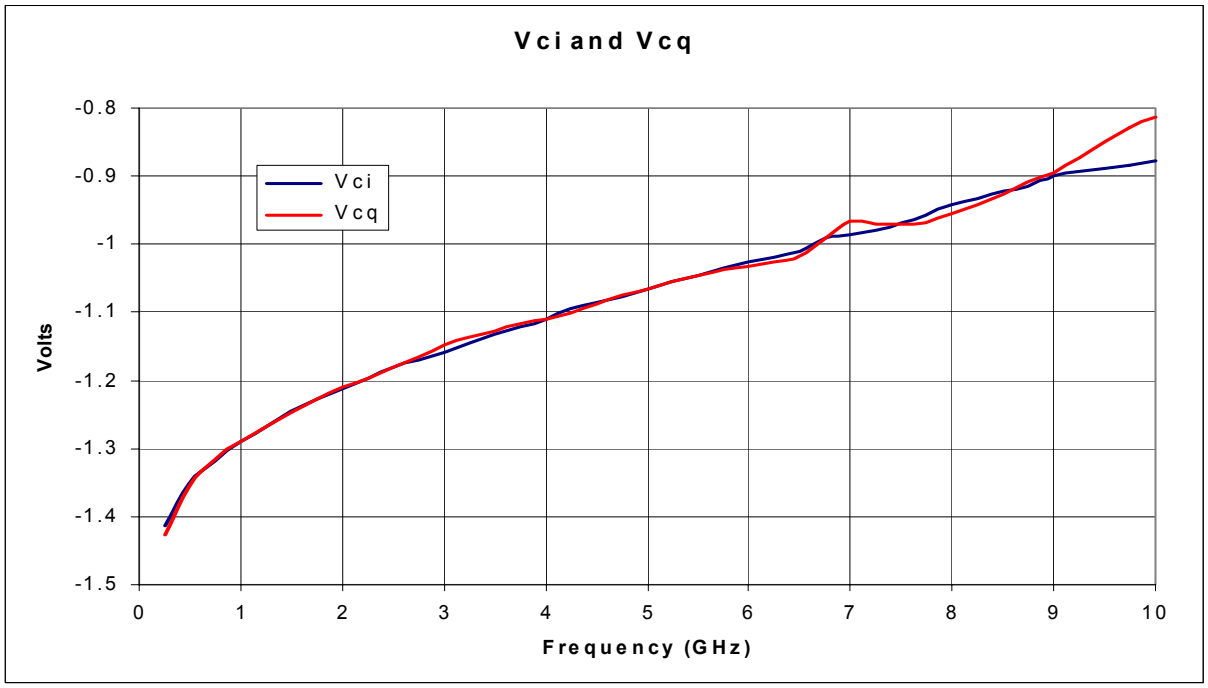


Figure 2.
Loop control voltages Vci and Vcq for simultaneous quadrature and equal detected amplitudes versus frequency.

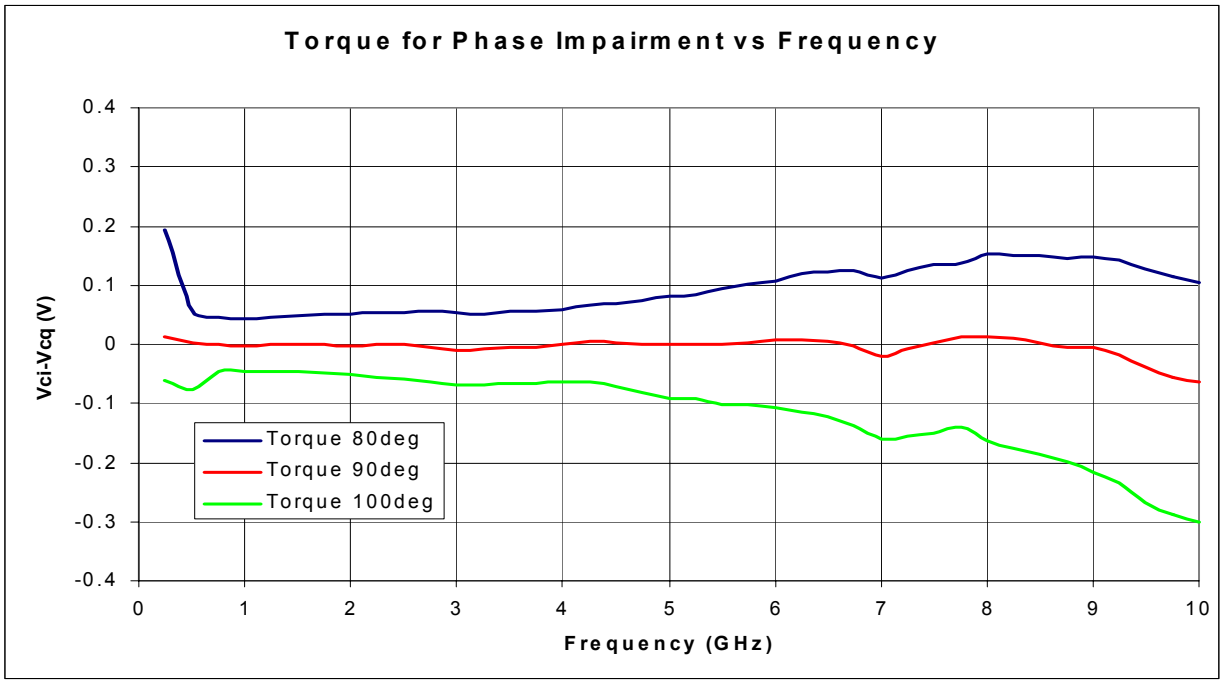


Figure 3.
"Torque" (Vci minus Vcq) for equal detected amplitudes and quadrature +/-10 degree phase impairment versus frequency.

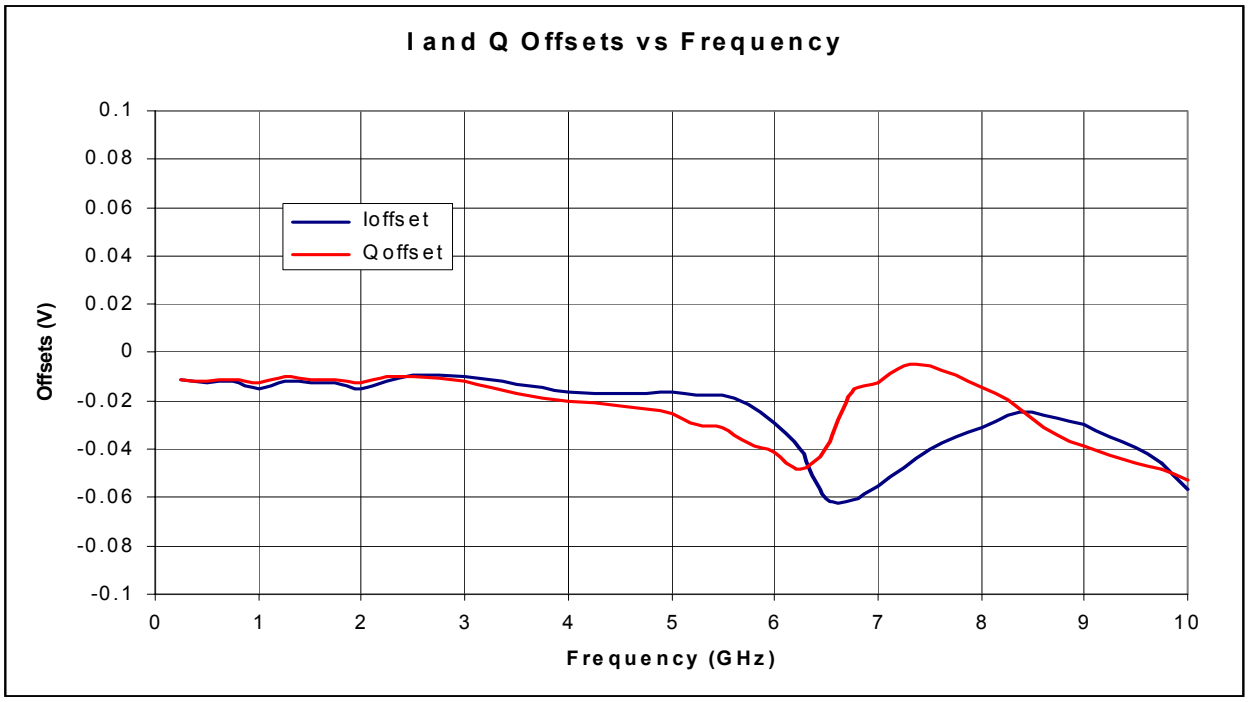


Figure 4.
Differential I and Q DC inputs required to suppress LO feedthrough versus frequency.

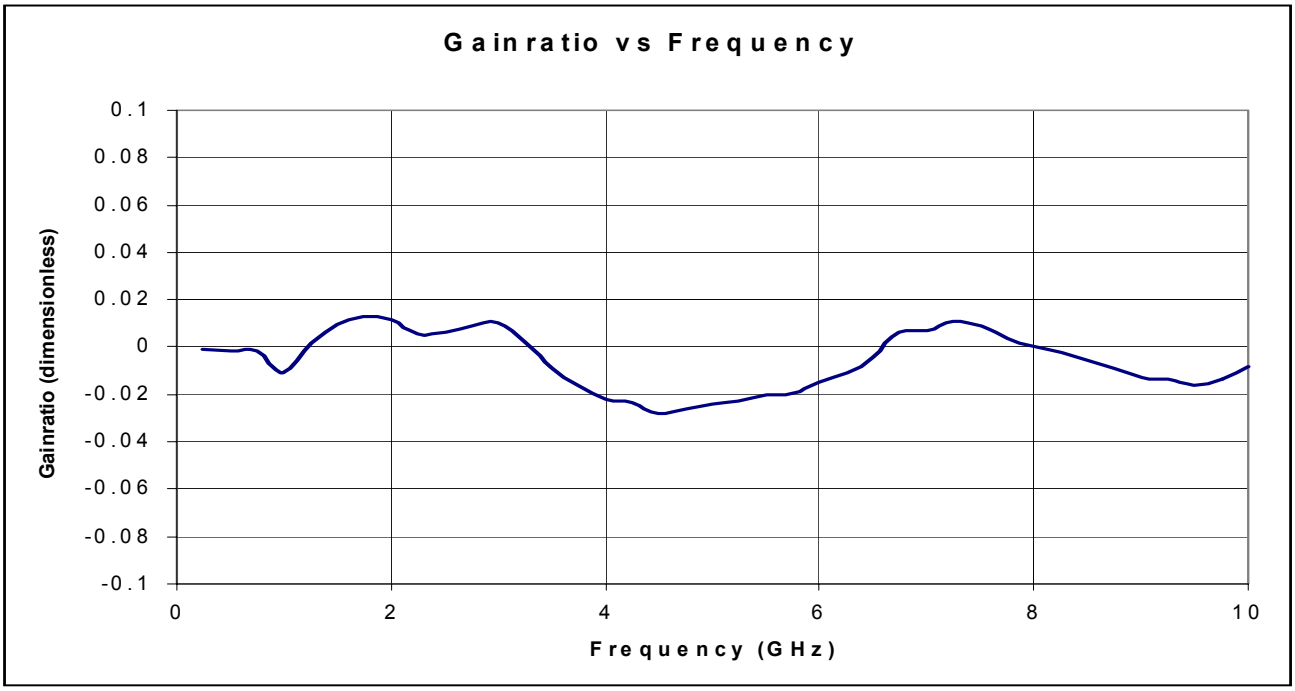


Figure 5.
Gainratio (ratio of I to Q baseband amplitudes for image supression) versus frequency.

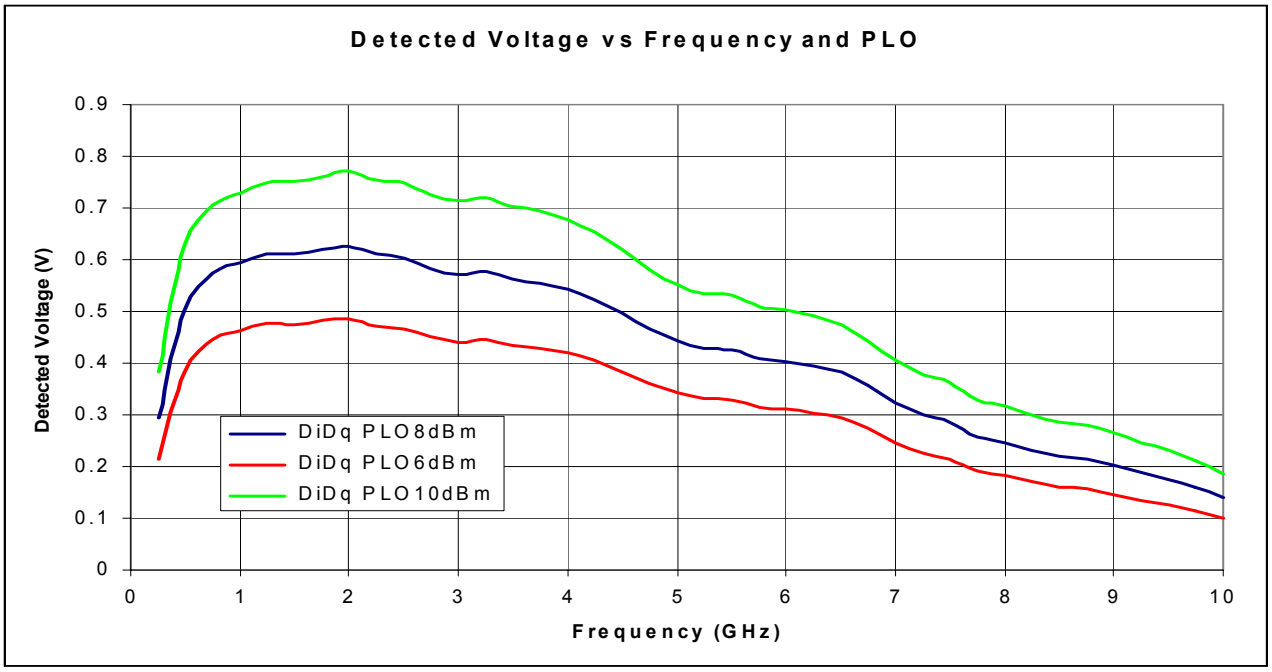


Figure 6.
Magnitude of detected voltages (DiDq - difference between PLO off and on, closed loop) versus frequency and PLO. Note the detectors actually deflect increasingly negative with LO power.

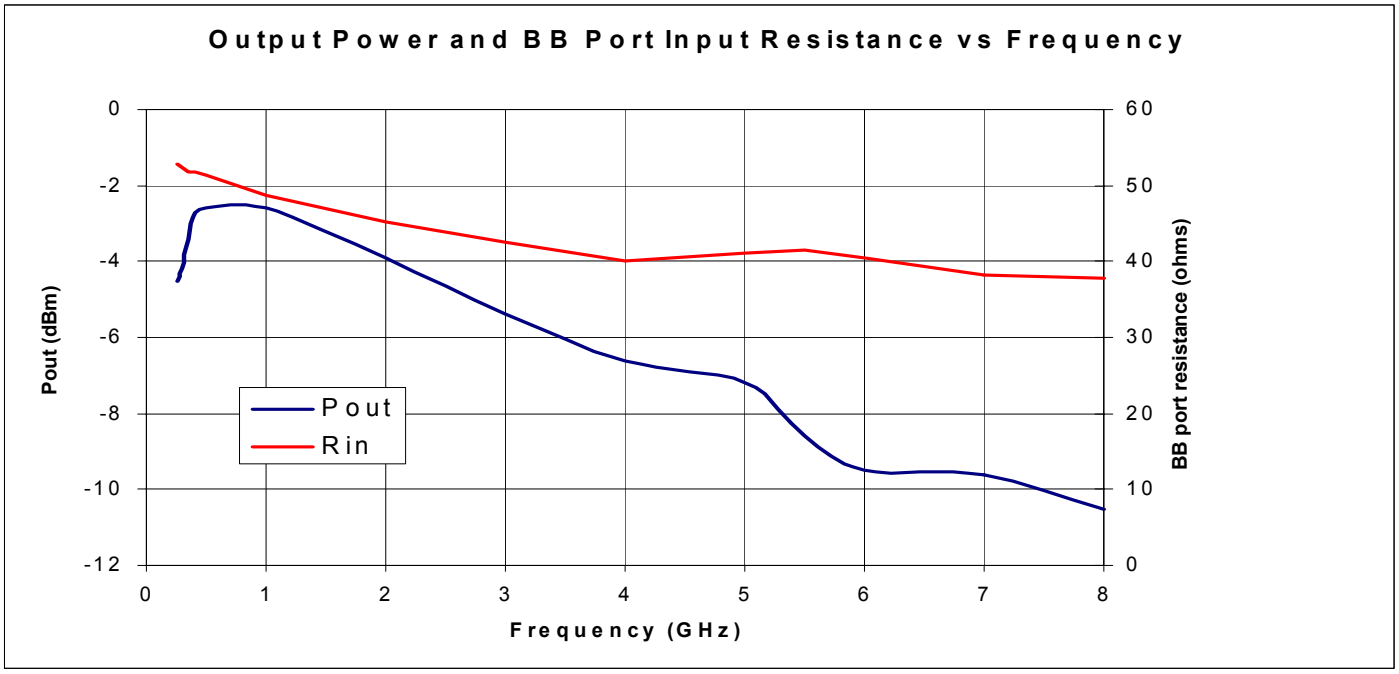


Figure 7.
Output power from one output port with V(I-Ibar) = V(Q-Qbar) = 200mVDC and single-ended base-band port resistance versus frequency.

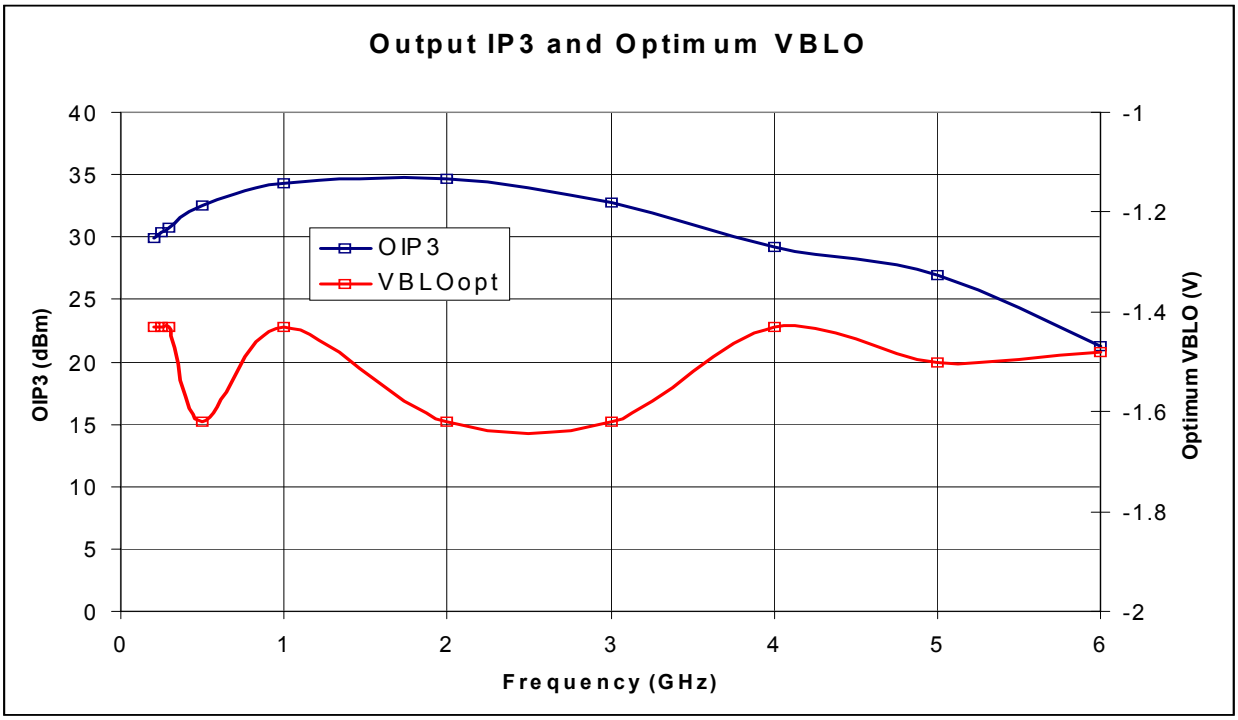


Figure 8.
Output 2-tone IP3 and optimum VBLO versus frequency (250-6000 MHz output balun included.)

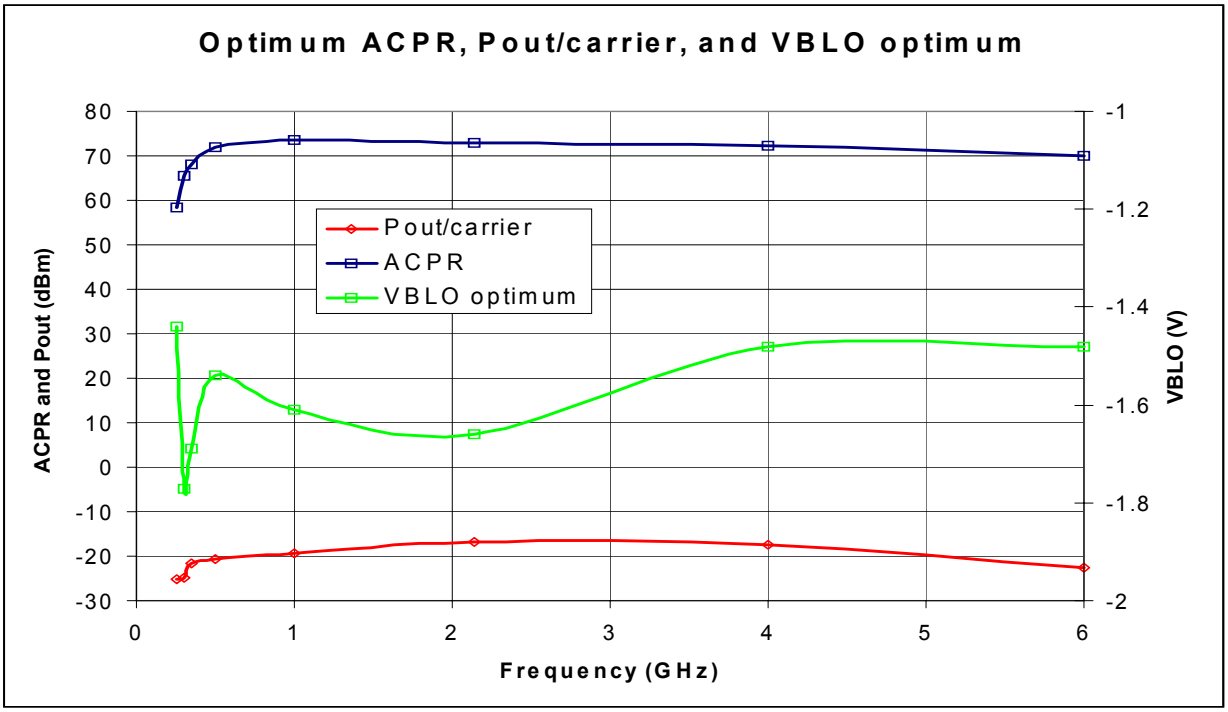


Figure 9.
ACPR (3GPP 4-carrier WCDMA), Pout/carrier, and optimum VBLO versus frequency (250-6000 MHz output balun included.)

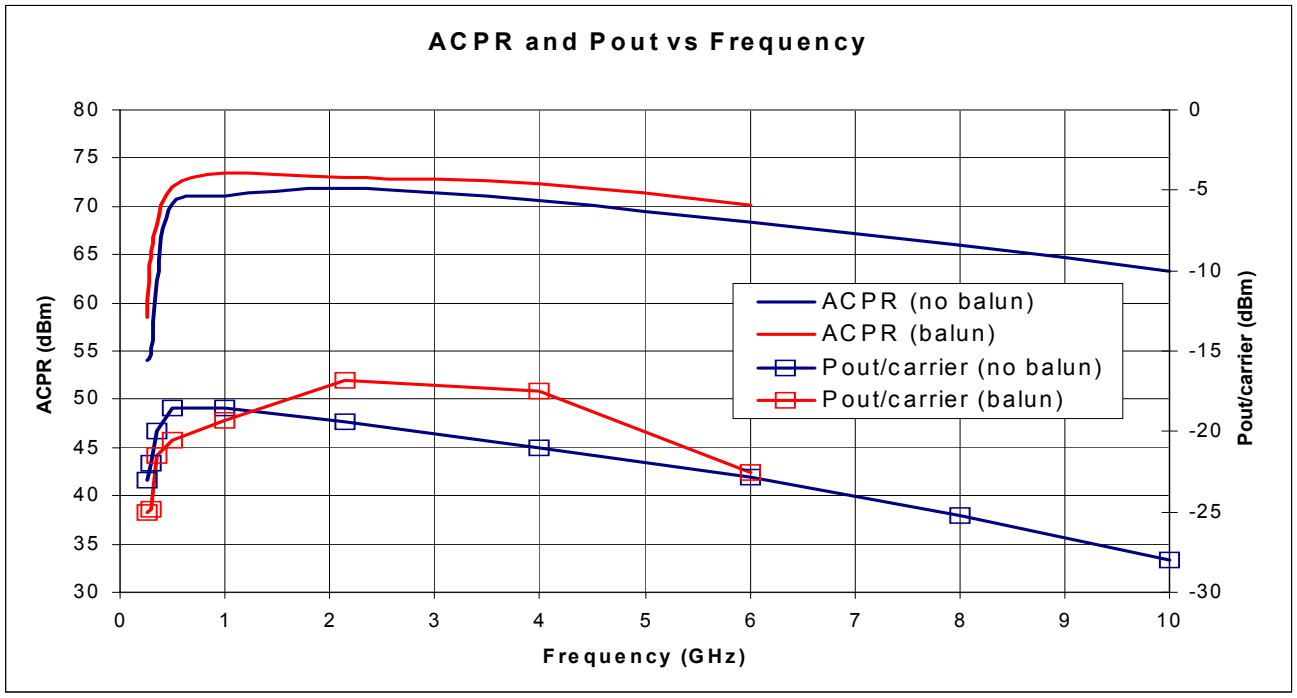


Figure 10.
Comparing ACPR (3GPP 4-carrier WCDMA) and Pout/carrier versus frequency with and without 250-6000 MHz output balun.

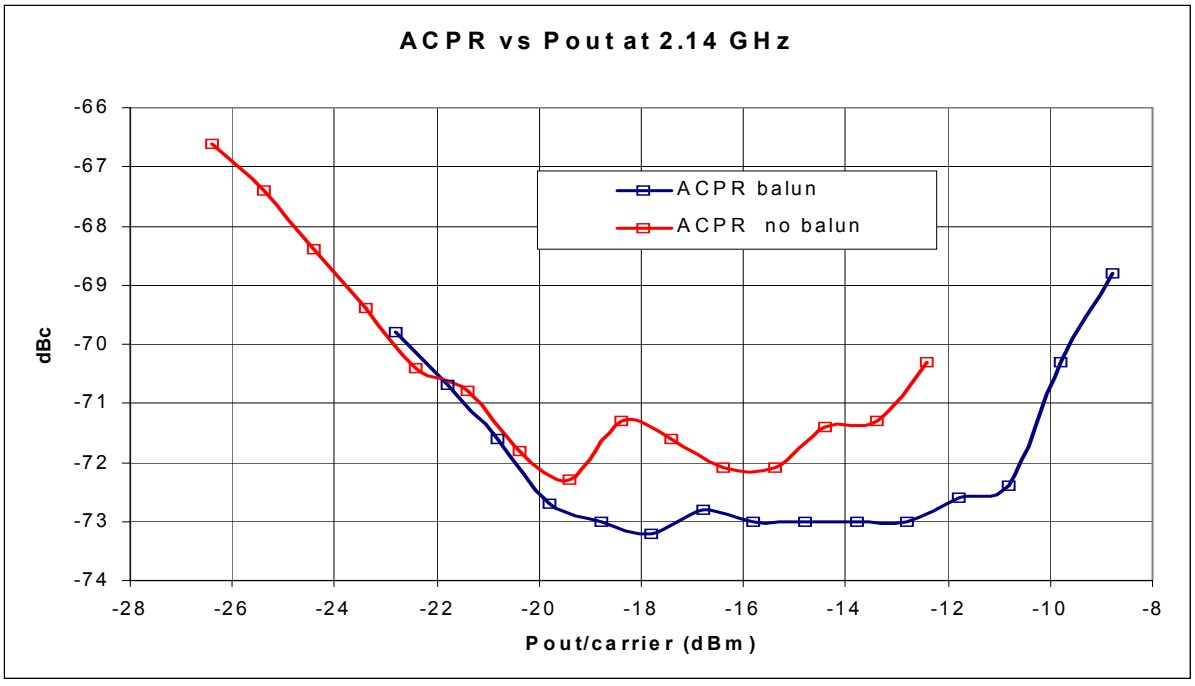


Figure 11.
Comparing 2.14 GHz ACPR (3GPP 4-carrier WCDMA) versus Pout/carrier with and without 250-6000 MHz output balun.

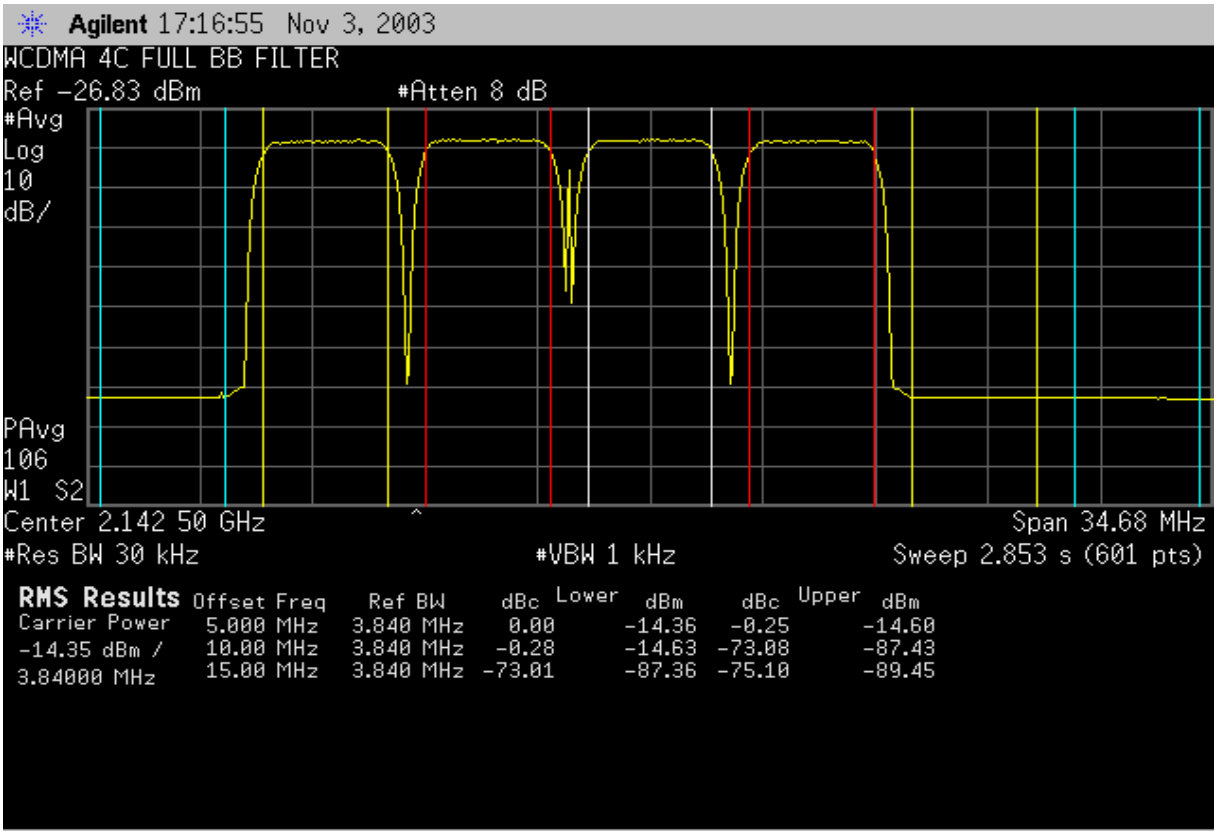


Figure 12.
2.14 GHz ACPR (3GPP 4-carrier WCDMA) spectral plot (includes 250-6000 MHz output balun.)

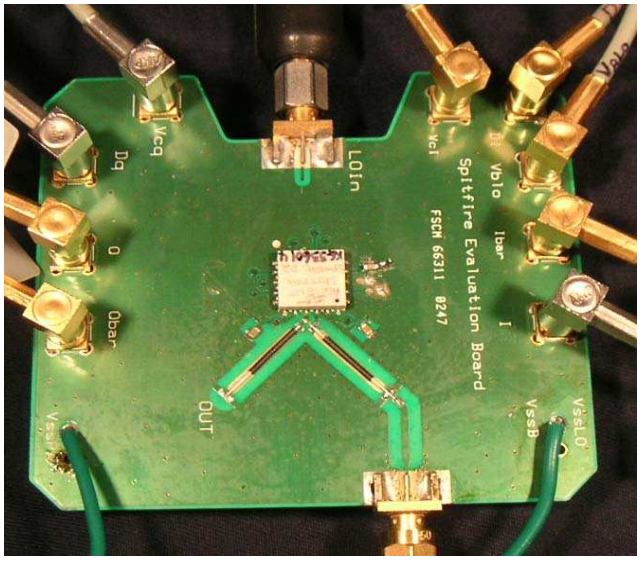


Figure 13.
TC932P test fixturing includes a PCB-based 250-6000 MHz output balun and a substantial backside heatsink.

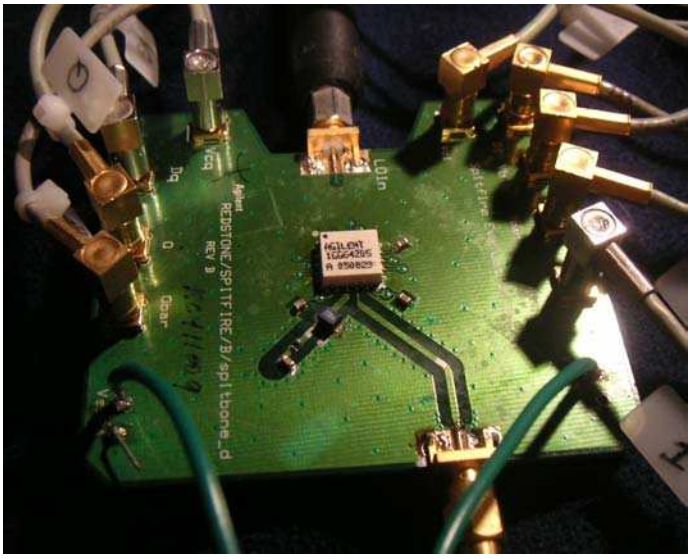


Figure 14
Test fixturing without balun for single-output measurements.

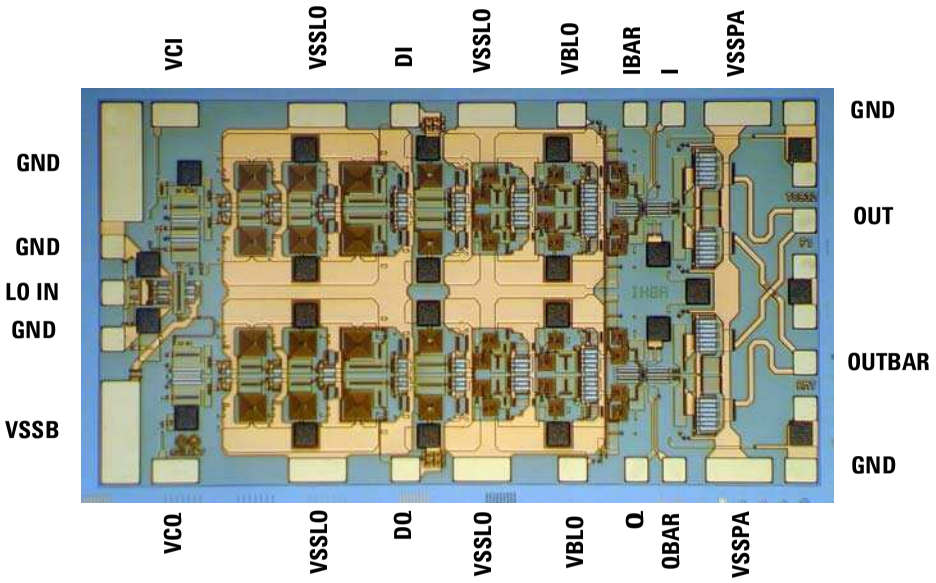


Figure 15.
TC932 Chip Pad Identifications.

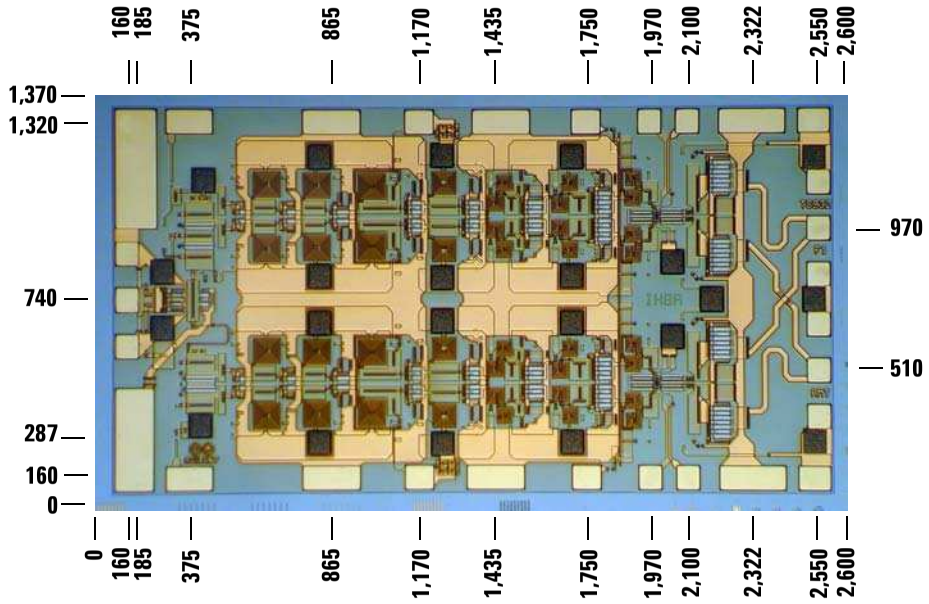


Figure 16.
TC932P Chip Pad Locations.