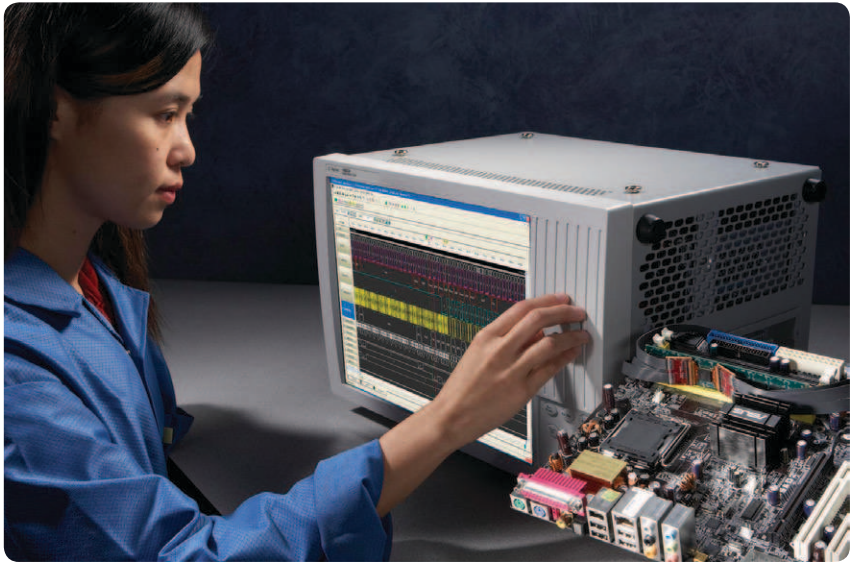




B4622A DDR2/3 Protocol Compliance and Analysis Tool

Data Sheet



DDR2/3 measurement and debug work has become more complex and time consuming over the years as the speed becomes faster and the architecture becomes more advance. Logic analyzer is one of the main measurement tools to acquire multiple DDR buses at speed for analysis through saved traces in waveform and listing window. This sometimes can be time consuming and complex with deep traces. The B4622A DDR2/3 protocol compliance and analysis tool enables automation on the measurement of your deep DDR bus trace to help you quickly identify protocol problem area and also gives you an overview of your system performance.

Features

- Automates DDR2/3 protocol compliance measurement at speed
- Quickly identifies protocol violation and timing errors
- Allows user-defined timing parameters
- Provides test results in HTML format for reporting purpose
- Provides a quick overview of the DDR bus performance with statistic and histogram view for bus optimization purposes
- Enables fast trigger setup with DDR trigger tool



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DDR2/3 Protocol Compliance Analysis

The B4622A DDR2/3 protocol compliance and analysis tool enables timing and functional validation measurement through the protocol compliance check capability. The tool provides the test results with details of the test failure in HTML format for reporting purposes. The following is the list of timing and protocol violations analysis enabled with the tool.

Timing violations

- Active/Read/Write to Precharge < tRASmin
- Active/Read/Write to Precharge < tRASmax
- Active to Read/Write < tDARW
- Precharge to Active/Precharge < tRP
- Read to Precharge/Auto-Precharge < tDRP
- Read to Write < tDRW
- Write to Precharge/Auto-Precharge < tDWP
- Write to Read < tDWR
- Write to Write < tCCD
- Refresh to non-NOP/DES must be > tRFC

State violations

- Read or Write to an inactive row
- Refresh to an active bank
- Activate to an active bank.

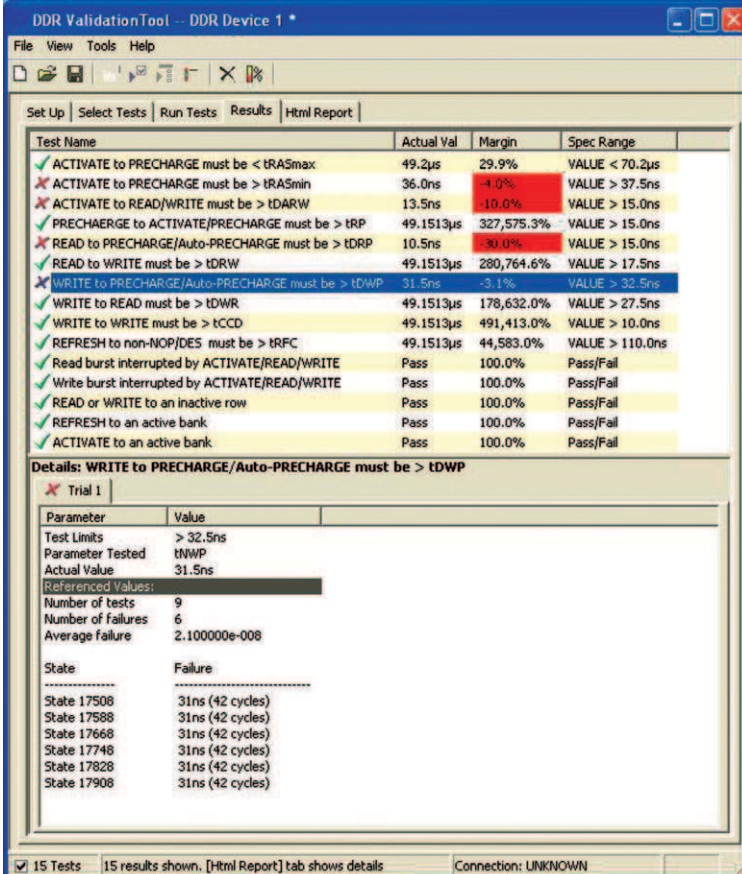


Figure 1. DDR2/3 protocol compliance tool for automated timing and state violations check

DDR2/3 Performance Analysis

Another key feature of the B4622A is the ability to view the performance of your DDR bus through bus statistic report and histogram. The bus statistic report gives you an overview of the DDR bus utilization for a specific trace to help you analyze the behavior and activity of your DDR bus. The histogram view reports the number of access in specific memory location to help you improve optimization by controlling the number of access across the address bus.

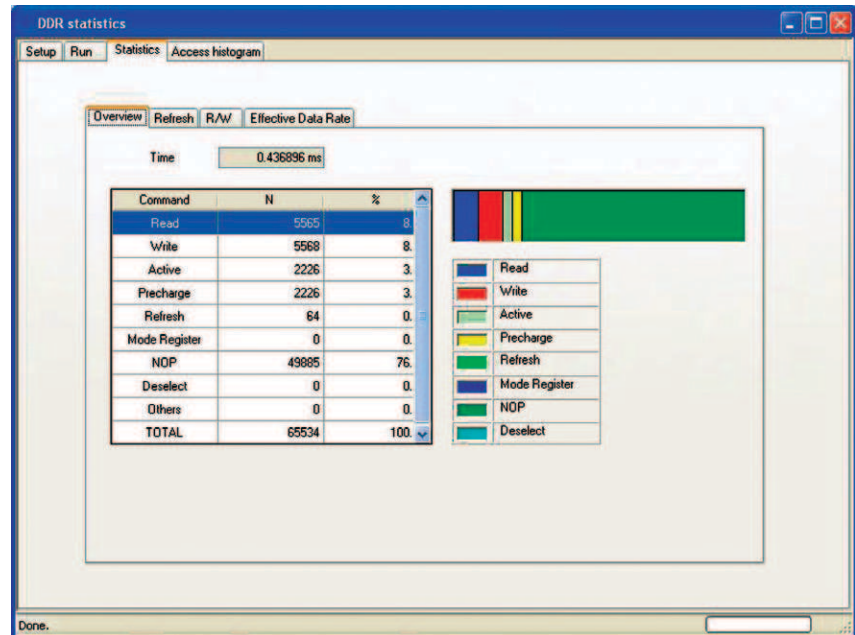


Figure 2. DDR bus statistic view for obtaining command cycles information in color-coded chart

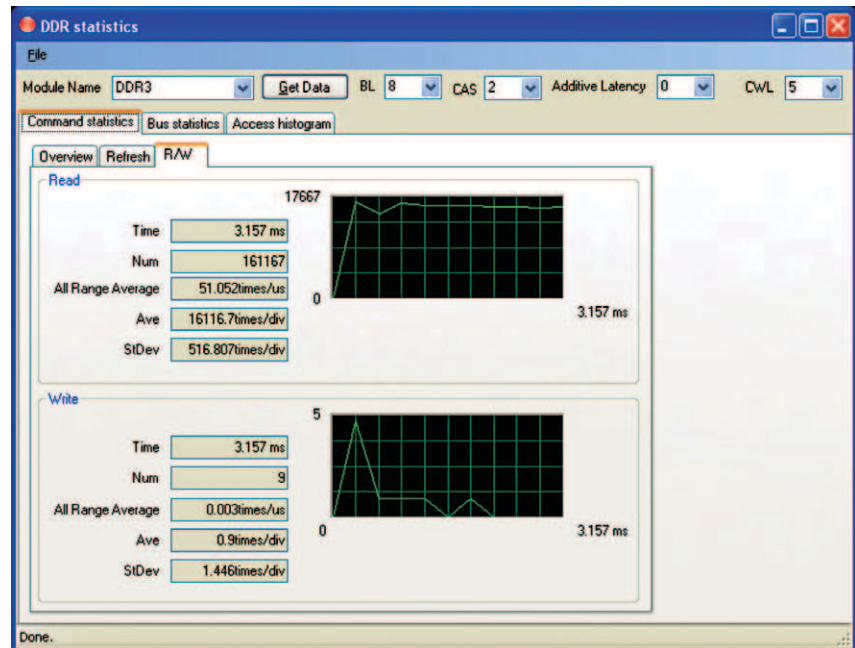


Figure 3. DDR bus statistic views for providing bus utilization information on read and write commands.

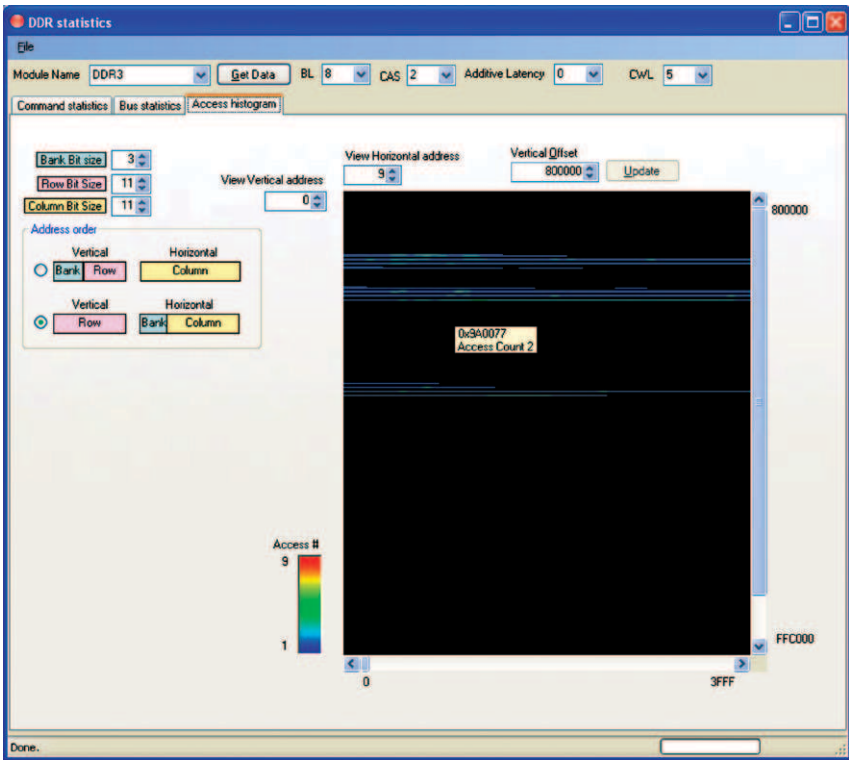
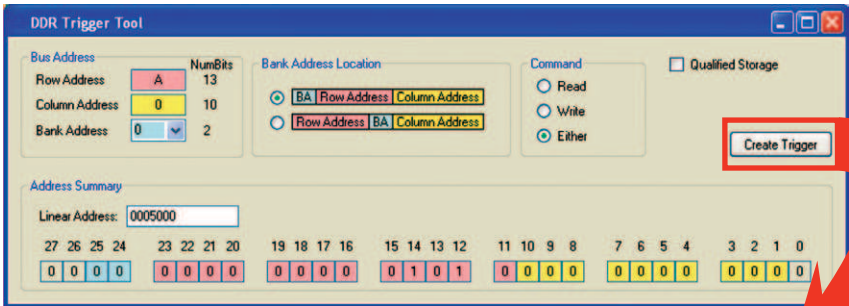


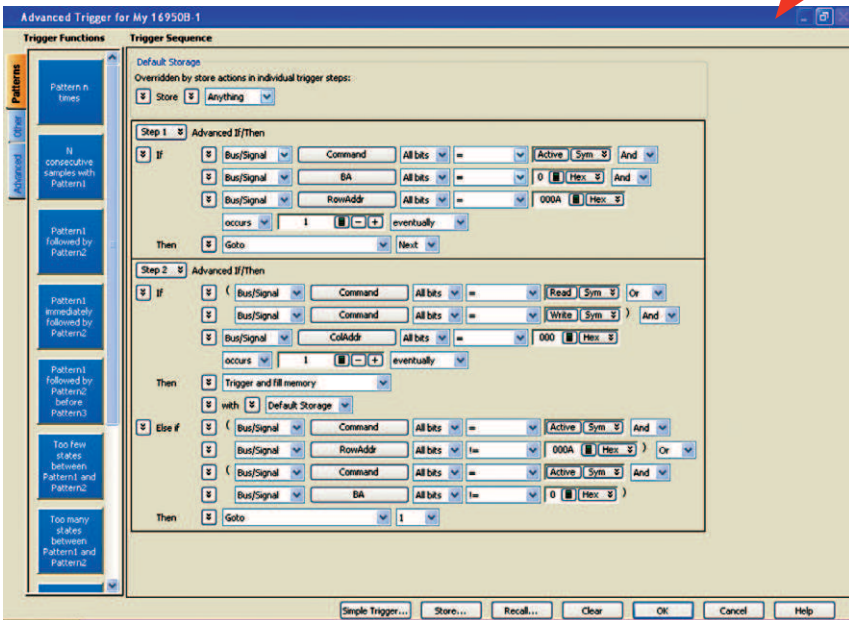
Figure 4. Access histogram view to enable overview of number of access at specific DDR address

DDR2/3 Trigger Tool

Setting up a trigger on a specific DDR2/3 physical address to obtain the corresponding data bus can be very tedious. The B4622A allows you to automatically create a trigger on a specific physical address without having to go through a step by step trigger add-in. The trigger setup tool incorporates a user-friendly interface to help you quickly setup the trigger.



(5a)



(5b)

Figure 5(a and b). User friendly interface to setup trigger on a physical address

Logic Analyzer Ordering Information

Product	Description
DDR2 BGA probes	
W2631A	DDR2 x16 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2632A	DDR2 x16 BGA data probe for logic analyzer and oscilloscope – kit of 4 probes
W2633A	DDR2 x8 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2634A	DDR2 x8 BGA data probe for logic analyzer and oscilloscope – 4 probe set
16900 Series logic analyzers	
16900A	6-slot mainframe, requires external display
16901A	2-slot mainframe with 15-inch display with touch screen
16902B	6-slot mainframe with 15-inch display with touch screen
Logic analyzer modules	
16950B	68-channel 4 GHz timing, 667 MHz state logic analysis module
16962A	68- channel 2GHz timing, 2GT/s state logic analysis module
AXIe-based logic analyzers	
U4154A	136-channel, 4 Gb/s state, AXIe-based logic analyzer module
Logic analyzer ZIF probes (used to connect W2630As Series DD2 BGA probes to 90 pin logic analyzer cables)	
E5384A	46-ch single-ended ZIF probe for x8/x16 DRAM BGA probe connect to 90-pin logic analyzer cable
E5826A	46-ch single-ended ZIF probe for x16 DRAM data only BGA probe connect to logic analyzer cable
E5827A	46-ch single-ended ZIF probe for 2 x8 DRAMs data only BGA probe connect to 90-pin logic analyzer
DDR3 BGA probes	
W3631A	DDR3 x16 BGA command and data probe for logic analyzer and oscilloscope
W3633A	DDR3 x4/x8 BGA command and data probe for logic analyzer and oscilloscope
Logic analyzer ZIF probes (used to connect W3630A Series DDR3 BGA probes to 90 pin logic analyzer cables)	
E5845A	46-ch single-ended ZIF probe for x16 DRAM BGA probe connect to 90-pin logic analyzer cable
E5847A	46-ch single-ended ZIF probe for x8 DRAM BGA probe connect to 90-pin logic analyzer cable
Software	
B4621A	DDR2/3 bus decoder
DDR3 DIMM Probe	
N4835A	DDR3 advanced slot interposer probe
N4834A	Soft touch, double probe enhanced, SE, 90-pin cable

Related Literature

Publication title	Pub number
<i>16900 Series Logic Analysis System Brochure</i>	5989-0420EN
<i>U4154A Logic Analyzer Module Data Sheet</i>	5990-7513EN
<i>W2630A Series DDR2 DRAM BGA Probe Data Sheet</i>	5989-5964EN
<i>Agilent W3630A Series DDR3 BGA Probe Data Sheet</i>	5990-3179EN

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