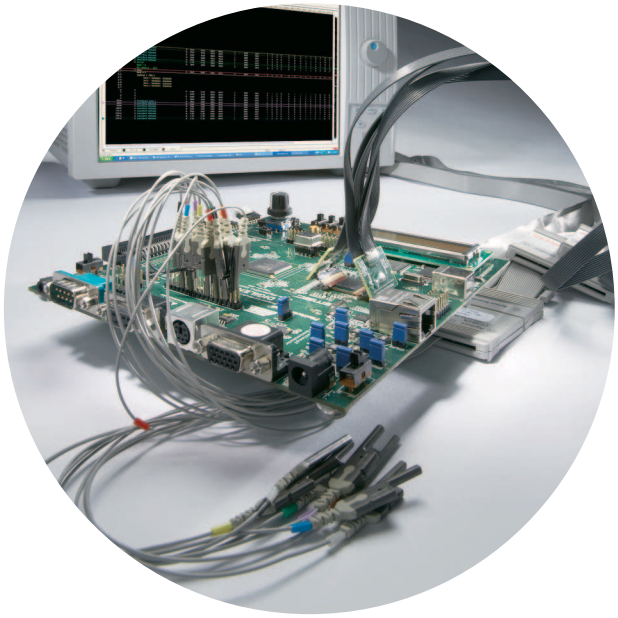
W2630 Series DDR2 BGA Probes for Logic Analyzers and Oscilloscopes

Data Sheet



The W2630 Series DDR2 BGA probes enable probing of embedded memory DIMMs directly at the ball grid array with Agilent logic analyzers and oscilloscopes

Agilent Technologies

Features

The Agilent W2630 Series DDR2 BGA probes for logic analyzers and oscilloscopes enable viewing of data traffic on industry standard DDR2 DRAMs with the Agilent 16900 Series logic analysis system and Infiniium 80000 Series oscilloscopes.

Features	Benefits
Connects directly to the DDR2 BGA balls	Eliminates reflections from mid-bus probing methods. Also eliminates board space and trace routing required for connector probing methods.
Supports: • x8 (84 ball) all signals • x16 (92 ball) all signals and x16 (84 ball) without mechanical support balls • x4 (60 ball) dual die packages with traces to CS0, CKE0, and OTD0 only • Quad die packages with W2632A and traces to CS0, CKE0 and ODT0 only	Get complete signal access to the DDR2 signals critical to your debug and validation effort
Buried resistors provide signal isolation and minimize capacitive loading. Probe loading: 2 pF Minimum signal amplitude: • 250 mV p-p for single-ended signals • $V_{max} - V_{min}$ 100 mV for differential signals	Acquire high-speed signals without impacting the performance of your design. The DDR2 BGA probe provides a non-intrusive electrical and mechanical connection between the memory device and an Agilent 16900 Series logic analyzer.
• Operating transfer rate of 800 Mb/s • 2 GHz bandwidth	Operate at full speed whether you're making measurements with a logic analyzer or oscilloscope.
Works with existing designs	Eliminates need for re-design or up front planning.
Supports either leaded or lead-free solder	Easily works with all solder finishes. Designed to tolerate lead-free soldering temperature profiles.
Contract manufactures available for those without the in-house expertise or facilities for soldering BGAs	Eliminates the need to develop BGA soldering expertise.
Flexible "wings" with ZIF connectors	Ensures reliable connection to the ZIF probes. Enables placement of the probe cables around adjacent components. Minimizes the torque to the balls of the BGA.
Attach to E5384A, E5826A, or E5827A single-ended ZIF probes for connection to the logic analyzer	Optimizes the use of logic analyzer channels by allowing assignment of channels to 8 or 16 bits on each DRAM.
Probe points available for soldering ZIF tip accessories to the scope probe adapter board that connects to the BGA probe	Enables oscilloscope probing of the DRAM signals with an Agilent Infiniium 80000 Series oscilloscope, giving you a DDR2 test solution covering the clock characterization, electrical and timing parameters of the JEDEC specification.

DDR2 BGA Probe Connection to an Agilent Logic Analyzer

The W2630 Series DDR2 BGA probes are used with the 46 channel single-ended ZIF probe which connects to 90-pin logic analyzer cable. The BGA probe has ZIF connections on each wing to connect to DDR2 address, control and data signals to the logic analyzer through the 46 channel single-ended ZIF probe. Different probes are available for different DRAM signal probing:

ZIF probes	Provides access to
E5384A	All x8 or x16 DRAM buses
E5826A	x16 DRAM data buses
E5827A	Two x8 DRAM data buses

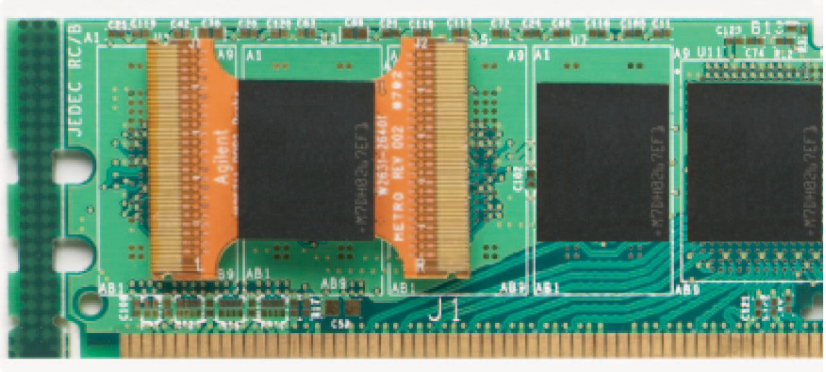


Figure 1. W2631B DDR2 x16 BGA command and data probe for logic analyzer and oscilloscope soldered onto a DDR2 DIMM

Figure 2. E5384A 46-ch single-ended ZIF probe for x8/x16 DRAM BGA probe connects to 90-pin logic analyzer cables

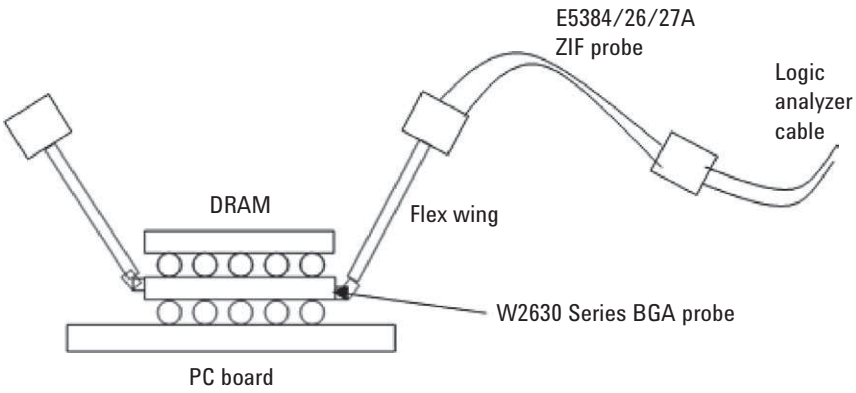


Figure 3. Probe connection to the logic analyzer

Protocol Analysis

The W2630 Series BGA probe along with the B4621A memory bus decoder provides complete protocol decode of memory transactions using an Agilent logic analyzer as the analysis execution engine. This combination provides memory bus triggering, debug and compliance verification measurements. Data is decoded and displayed at any level of detail from the protocol to binary. The B4621A protocol-decode software translates acquired signals into easily understood bus transactions, at the full bus speed. The Agilent logic analyzer provides extensive triggering and store qualification features.
The DDR protocol-decode software executes in the logic analyzer and takes user input on system attributes such as Burst length, CAS and Additive Latency, as well as Chip Selects to decode the key DDR bus signals and present a display that lists the transaction type, address, data and command conditions. The software also supports user-defined symbols that can be easily added to the state listing display.

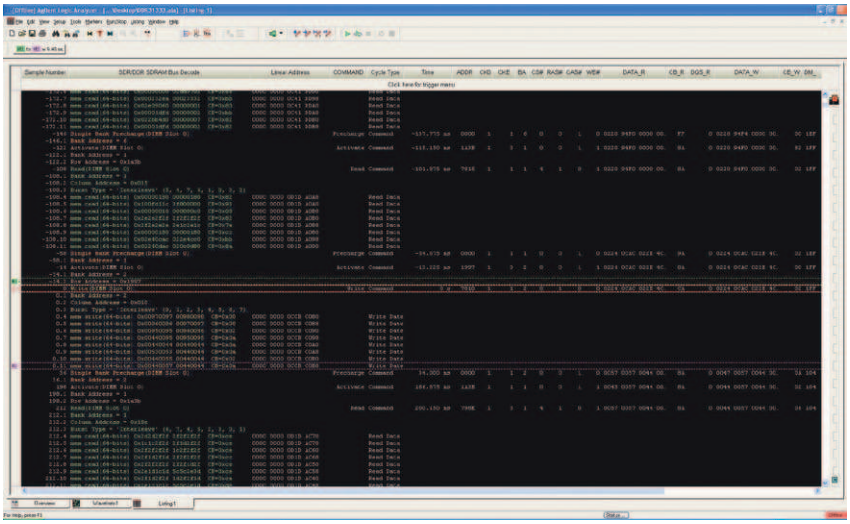


Figure 4. Reliable protocol decode with B4621A DDR2 bus decoder

DDR2 BGA Probe Connection to an Oscilloscope

The DDR2 BGA probe is used with W2639A scope probe adapter and the E2678A socketed probe head with damping headers to connect to the oscilloscope. The socketed probe head makes a 4 GHz bandwidth (typical) connection with the pin headers on the W2639A scope probe adapter.

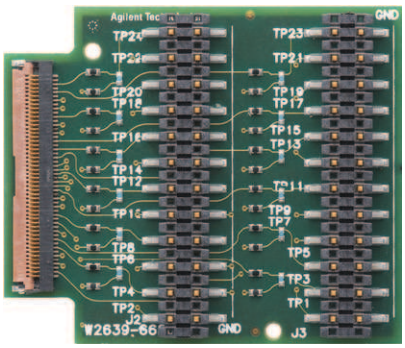


Figure 5. W2639A

Probe Pin-out to Oscilloscope

W2639A LPDDR BGA probe adapter board pin-out for DDR2 interposer configuration (W2631B)

Left flex wing						Right flex wing					
Signal name	**Signal name**	**Test point**	**Signal name**	**Signal name**	**Test point**	**Test point**	**Signal name**	**Signal name**	**Test point**	**Signal name**	**Signal name**
GND	UDM	TP1	GND	DQ14	TP2	TP24	DQ15	GND	TP23	DQ8	GND
GND	DQ9	TP3	GND	DQ11	TP4	TP22	DQ10	GND	TP21	DQ13	GND
GND	DQ12	TP5	GND	DQ6	TP6	TP20	LDQS#	GND	TP19	DQ7	GND
GND	LDM	TP7	GND	DQ1	TP8	TP18	LDQS	GND	TP17	DQ0	GND
GND	DQ3	TP9	GND	DQ4	TP10	TP16	DQ2	GND	TP15	DQ5	GND
GND	VREF	TP11	GND	CKE	TP12	TP14	CK	GND	TP13	ODT	GND
GND	WE#	TP13	GND	BA1	TP14	TP12	CK#	GND	TP11	RAS#	GND
GND	BA0	TP15	GND	BA2	TP16	TP10	CAS#	GND	TP9	CS#	GND
GND	A1	TP17	GND	A5	TP18	TP8	A0	GND	TP7	A4	GND
GND	A10	TP19	GND	A3	TP20	TP6	A2	GND	TP5	A6	GND
GND	A7	TP21	GND	NC	TP22	TP4	A8	GND	TP3	RFU#2	GND
GND	A12	TP23	GND	A9	TP24	TP2	A11	GND	TP1	NC	GND

W2639A LPDDR BGA probe adapter board pin-out for DDR2 interposer configuration (W2633B)

Left flex wing						Right flex wing					
Signal name	**Signal name**	**Test point**	**Signal name**	**Signal name**	**Test point**	**Test point**	**Signal name**	**Signal name**	**Test point**	**Signal name**	**Signal name**
GND	NC	TP1	GND	Nc	TP2	TP24	NC	GND	TP23	NC	GND
GND	NC	TP3	GND	NC	TP4	TP22	NC	GND	TP21	NC	GND
GND	NC	TP5	GND	DQ6	TP6	TP20	LDQS#	GND	TP19	DQ7	GND
GND	NC	TP7	GND	DQ1	TP8	TP18	LDQS	GND	TP17	DQ0	GND
GND	DQ3	TP9	GND	DQ4	TP10	TP16	DQ2	GND	TP15	DQ5	GND
GND	VREF	TP11	GND	CKE	TP12	TP14	CK	GND	TP13	ODT_0	GND
GND	WE#	TP13	GND	BA1	TP14	TP12	CK#	GND	TP11	RAS#	GND
GND	BA0	TP15	GND	BA2	TP16	TP10	CAS#	GND	TP9	CS#	GND
GND	A1	TP17	GND	A5	TP18	TP8	A0	GND	TP7	A4	GND
GND	A10	TP19	GND	A3	TP20	TP6	A2	GND	TP5	A6	GND
GND	A7	TP21	GND	A9	TP22	TP4	A8	GND	TP3	RFU#2	GND
GND	A12	TP23	GND	NC	TP24	TP2	A11	GND	TP1	NC	GND

Logic Analyzer Configuration Guide and Ordering Information

DRAM type	Data width	Access to	Probes	Cables	Logic analyzer modules	Order summary
x8	x32	Command, Address, Control and Data	W2633B	E5384A	16950B[1] x 2	16950B: 3 E5384A: 1 E5827A: 2 W2633B: 1 (kit of 4 probes) W2634A: 1 (kit of 4 probes)
		Data	W2634A			
		Data	W2634A	E5827A		
		Data	W2634A	E5827A	16950B	
x8	x64	Command, Address, Control and Data	W2633B	E5384A	16950B[1] x 2	16950B: 4 E5384A: 1 E5827A: 4 W2633B: 1 (kit of 4 probes) W2634A: 2 (kit of 4 probes)
		Data	W2634A		16950B	
		Data	W2634A	E5827A		
		Data	W2634A			
		Data	W2634A	E5827A		
		Data	W2634A		16950B	
		Data	W2634A	E5827A		
		Data	W2634A	E5827A		
x16	x32	Command, Address, Control and Data	W2631B	E5384A	16950B	16950B: 2 E5384A: 1 E5826A: 1 W2631B: 1 (kit of 4 probes) W2632A: 1 (kit of 4 probes)
		Data	W2632A	E5826A	16950B	
x16	x64	Command, Address, Control and Data	W2631B	E5384A	16950B	16950B: 3 E5384A: 1 E5826A: 3 W2631B: 1 (kit of 4 probes) W2632A: 1 (kit of 4 probes)
		Data	W2632A	E5826A	16950B	
		Data	W2632A	E5826A		
		Data	W2632A	E5826A	16950B	

1. One pod pair is required for time tags

Logic Analyzer Configuration Guide and Ordering Information for 16962A Logic Analyzer Module

DRAM type	Data width	Access to	Probes	Cables	Logic analyzer modules	Order summary
x8	x8	Command, Address, Control and Data	W2633B	E5384A	16962A[1] x 2	16962A: 2 E5384A: 1 W2633B: 1 (kit of 4 probes)
x8	x16	Command, Address, Control and Data	W2633B	E5384A	16962A[1] x 2	16962A: 2 E5384A: 1 W2633B: 1 (kit of 4 probes) W2634A: 2 (kit of 4 probes)
		x8 Data	W2634A	E5827A		
x16	x16	Command, Address, Control and Data	W2631B	E5384A	16962A[1] x 2	16962A: 2 E5384A: 1 W2631B: 1 (kit of 4 probes)
x16	x32	Command, Address, Control and Data	W2631B	E5384A	16962A[1] x 2	16962A: 2 E5384A: 1 E5826A: 1 W2631B: 1 (kit of 4 probes)
		x16 Data	W2632A	E5826A		W2632A: 1 (kit of 4 probes)

1. *16962A requires address, command and control to be on a separate logic analyzer module as the data for DDR Eyefinder software to find the read and write sampling position. The number of cards maybe reduced to 1 if a stimulus to do read only or write only is available for use with Eyescan to find sampling position.*

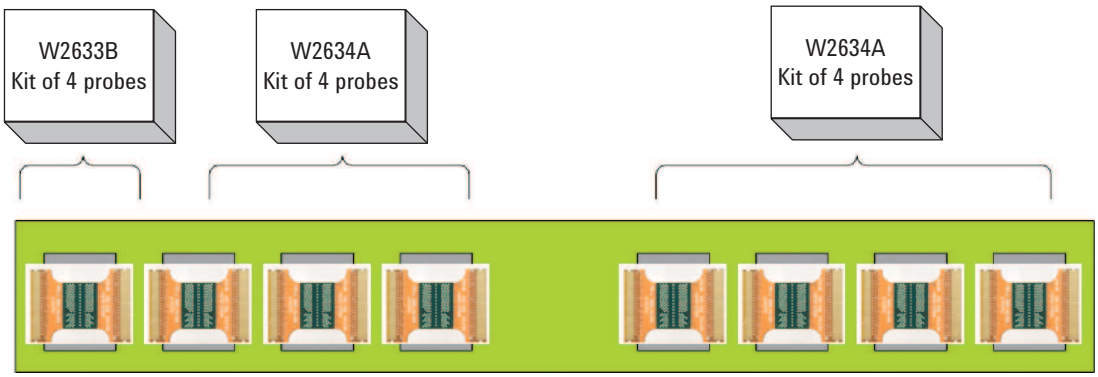


Figure 6. Example of use model for W2630 Series DDR2 BGA probes when configuring a probing solution for a x8 DDR2 DIMM with 64 data width

Logic Analyzer Ordering Information

Product	Description
DDR2 BGA probe	
W2631B	DDR2 x16 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2632A	DDR2 x16 BGA data probe for logic analyzer and oscilloscope – kit of 4 probes
W2633B	DDR2 x8 BGA command and data probe for logic analyzer and oscilloscope – kit of 4 probes
W2634A	DDR2 x8 BGA data probe for logic analyzer and oscilloscope – 4 probe set
16900 Series logic analyzer	
16900A	6-slot mainframe, requires external display
16901A	2-slot mainframe with 15-inch display with touch screen
16902B	6-slot mainframe with 15-inch display with touch screen
Logic analyzer modules	
16950B	68-channel 4 GHz timing, 667 MHz state logic analysis module
16962A	68-channel 2 GHz timing, 2 GT/s state logic analysis module
Logic analyzer ZIF probes (used to connect W2630s Series DDR2 BGA probes to 90 pin logic analyzer cables)	
E5384A	46-ch single-ended ZIF probe for x8/x16 DRAM BGA probe connect to 90-pin logic analyzer cable
E5826A	46-ch single-ended ZIF probe for x16 DRAM data only BGA probe connect to logic analyzer cable
E5827A	46-ch single-ended ZIF probe for 2 x8 DRAMs data only BGA probe connect to 90-pin logic analyzer
Software Decoder	B4621A Bus Decoder for DDR2 and DDR3

Oscilloscope Ordering Information

Product	Description
92504A	2.5 GHz 4 channels 20 GSa/s Infiniium oscilloscope
90404A	4 GHz 4 channels 20 GSa/s Infiniium oscilloscope
90604A	6 GHz 4 channels 20 GSa/s Infiniium oscilloscope
90804A	8 GHz 4 channels 40 GSa/s Infiniium oscilloscope
91204A	12 GHz 4 channels 40 GSa/s Infiniium oscilloscope
91304A	13 GHz 4 channels 40 GSa/s Infiniium oscilloscope
Oscilloscope software packages	
N5413B	LPDDR2 and DDR2 Compliance Test Application
N5414B	InfiniiScan Event Identification Software
Oscilloscope probe amplifier	
1169A	12 GHz InfiniiMax differential probe amplifier
1168A	10 GHz InfiniiMax differential probe amplifier
1134A	7 GHz InfiniiMax differential probe amplifier
1132A	5 GHz InfiniiMax differential probe amplifier
1131A	3.5 GHz InfiniiMax differential probe amplifier
1130A	1.5 GHz InfiniiMax differential probe amplifier
Oscilloscope probe heads	
E2678A	InfiniiMax single-ended/differential socketed probe head and accessories
Oscilloscope probe board adapters	
W2639A	Scope probe adapter – kit of 2

Related Agilent Literature

Publication title	Pub number
Agilent Technologies 16900 Series Logic Analysis System Color Brochure	5989-0420EN
Agilent W2630 Series DDR2 DRAM BGA Probe User's Guide Manual	W2631-97000
Infiniium DSO90000A Series Oscilloscopes and InfiniiMax Series Probes Data Sheet	5989-7819EN
Agilent Technologies N5413B DDR2 and LPDDR2 Compliance Test Application for Infiniium 9000 and 90000 Series Oscilloscope Data Sheet	5989-3195EN
W3630 Series DDR3 BGA Probe for Logic Analyzer and Scope Data Sheet	5990-3179EN
B4622A DDR2/3 Protocol Compliance and Analysis Tool Data Sheet	5990-3300EN
A Time-Saving Method for Analyzing Signal Integrity in DDR Memory Buses Application Note	5989-6664EN

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