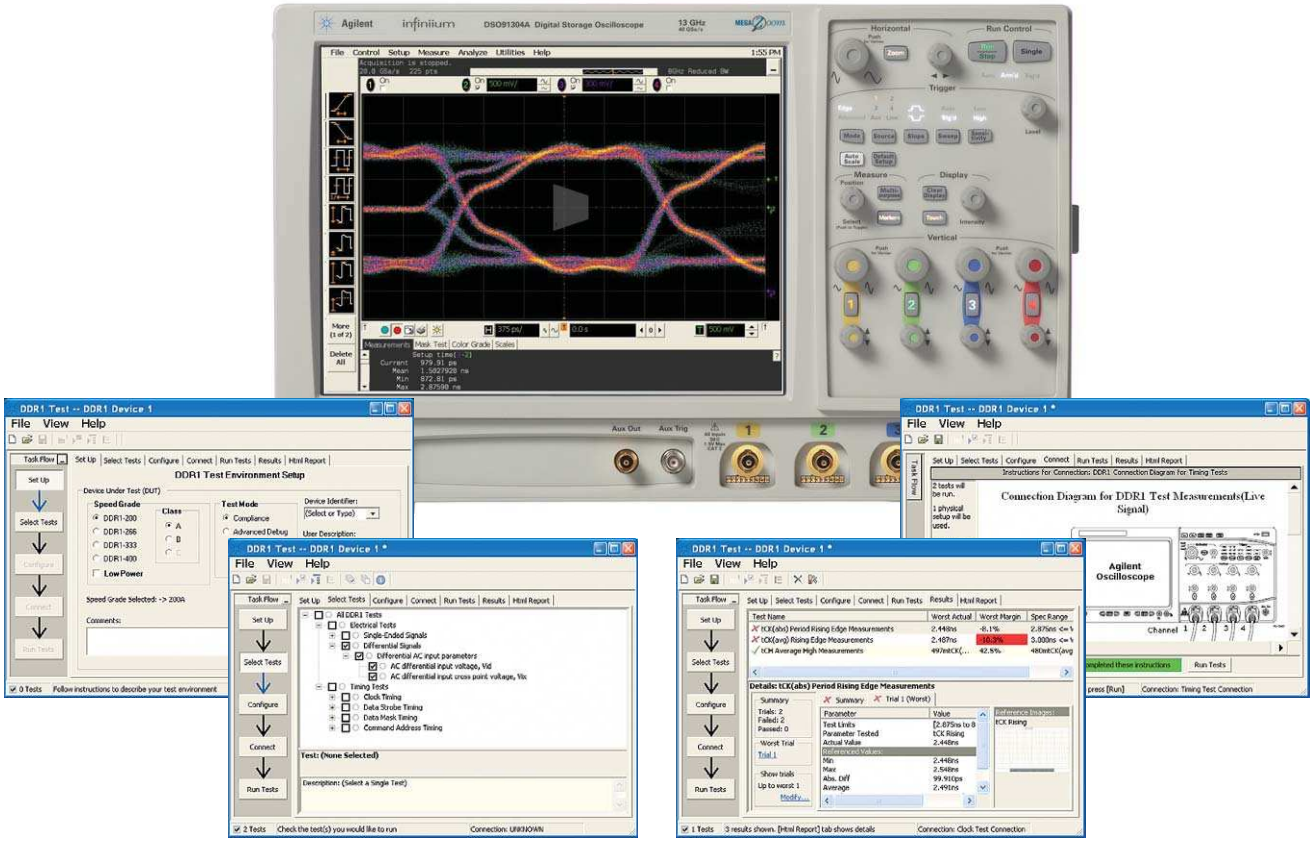
Agilent U7233A DDR1 Compliance Test Application with LPDDR and mobile-DDR Support for Infiniium Series Oscilloscopes

Data Sheet



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Test, debug and characterize your DDR1 designs quickly and easily

The Agilent Technologies U7233A DDR1 compliance test application provides a fast and easy way to test, debug and characterize your DDR1 designs. The tests performed by the U7233A software are based on the JEDEC[1] JESD79E Double Data Rate (DDR) SDRAM Specification and JESD209A Low Power Double Data Rate (LPDDR) SDRAM Specification. In addition, the application features Advanced Debug mode, which provides testing for embedded memory interfaces that do not operate according to the speeds specified by JEDEC. The test application offers a user-friendly setup wizard and a comprehensive report that includes margin analysis.

DDR1 is the first generation of a new breed of memory technology where data is transferred on both the rising and falling clock edges. DDR1 offers a significant performance advantage compared to previous memory technologies that were based on single data rates. As DDR1 manufacturing has matured, product costs have been driven down significantly, which has fueled growth, especially in the consumer product segment. DDR1 comes in two different packages, a fine ball-grid array (FBGA) package and a thin small-outline package (TSOP).

Signal integrity is crucial for memory system interoperability. Compliance to the JEDEC specification is the key to reliable and interoperable modular memory systems. Besides that, it ensures the memory system functions correctly and stays error free.

The U7233A DDR1 compliance test application is compatible with Agilent 9000 and 90000 Series Infiniium oscilloscopes.

1 The JEDEC (Joint Electronic Device Engineering Council) Solid State Technology Association is a semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronic industry.

Features

The U7233A DDR1 compliance test application offers several features to simplify the validation of your DDR1 designs:

- New setup wizard for quick setup, configuration and test
- Compliance testing of clock, electrical and timing measurements in accordance with the JEDEC JESD79E and JESD209A specifications
- Comprehensive analysis that automates the complex measurements, even when you are not there
- Unique read and write separation techniques with InfiniiScan "Zone Qualify" feature
- Ability to separate and analyze the loading due to adjacent rank of the same memory channel
- Automatically perform derating table calculations for setup and hold time measurements based on slew rate

Comprehensive test coverage

With the DDR1 compliance test application, you can use the same oscilloscope you use for everyday debugging to perform automated testing and margin analysis based on the JEDEC electrical and timing specifications. The application automatically configures the oscilloscope for each test and provides informative results. It includes margin analysis indicating how close your device comes to passing or failing the test for each specification.

Some of the difficulties in performing DDR1 tests are connecting to the target device, configuring the oscilloscope, performing the tests and analyzing the measured results. The DDR1 compliance test application does most of this work for you.

Easy test definition

The test application enhances the usability of Agilent Infiniium oscilloscopes for testing DDR1 devices. The Agilent automated test framework guides you quickly through the steps required to define the setup, perform the tests and view the test results. On the environmental setup page, you can select the type of DDR1 devices, and the framework automatically filters the tests based on your selection. You can then select a category of tests or specify individual tests. The user interface is designed to minimize unnecessary reconnections, which saves time and minimizes potential operator error. You can save the tests and configurations as project files and recall them later for quick testing and review of previous results. Clear menus let you perform tests with a minimum of mouse clicks.

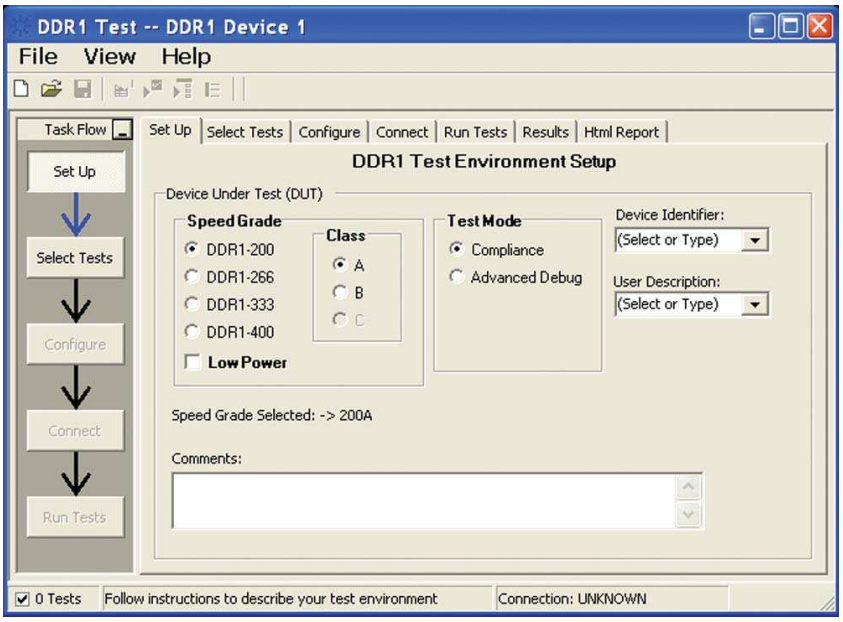


Figure 1. DDR1 application test setup screen. Select Compliance or Advanced Debug test mode and the speed grade of your device.

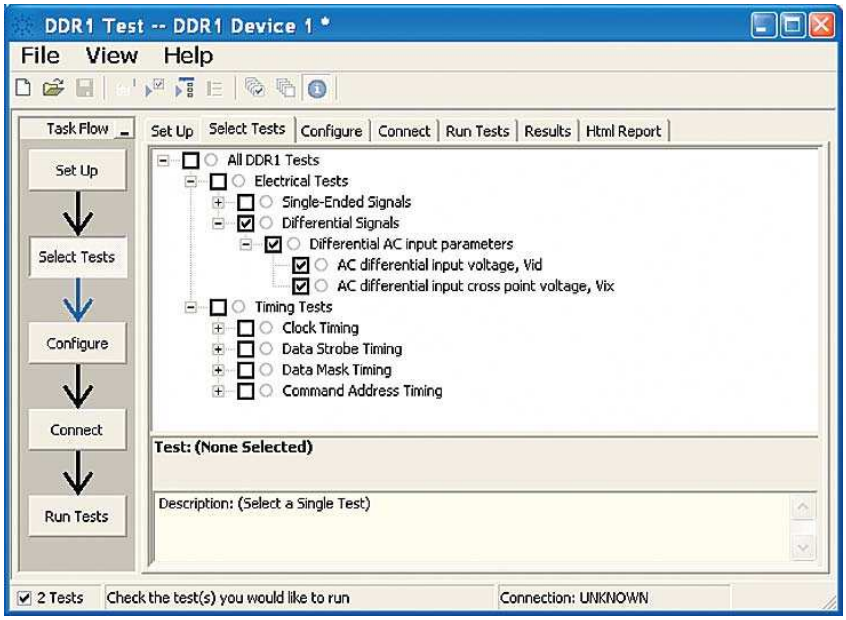


Figure 2. The Agilent automated test engine filters the test selection based on your test setup. You can easily select individual tests or groups of tests with a mouse-click.

Configurability and guided connection

The U7233A DDR1 compliance test application provides flexibility in your test setup. The application lets you define controls for critical test parameters such as voltage threshold values, number of waveforms used for analysis and customizable violation settings. Once you have configured the tests, the connection page will display the connection diagram for the test you have selected.

With the multiple test trial capability, you can extensively characterize the performance of your DDR1 devices. You can run the selected tests until the stop condition is met. The application will then save the worst-case conditions and help you track down the anomalies in your signals.

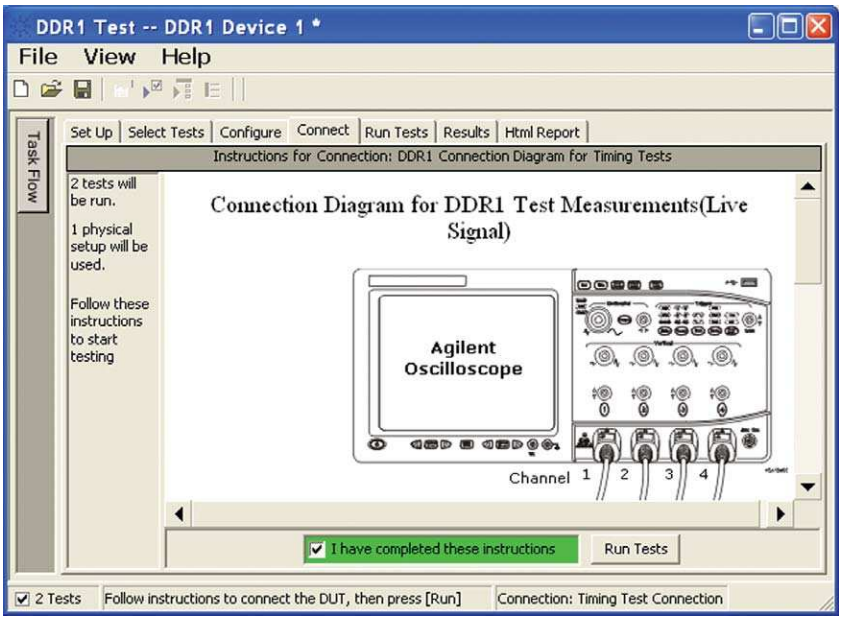


Figure 3. The software prompts you with the connection diagrams for the tests you have selected.

Comprehensive results analysis

In addition to providing you with measurement results, the U7233A DDR1 compliance test application reports how close you are to the specified limit. You can specify the level at which warnings are to be issued. You are provided with a full array of statistics for each measurement, and you can save worst-case conditions to extensively test the performance of your device.

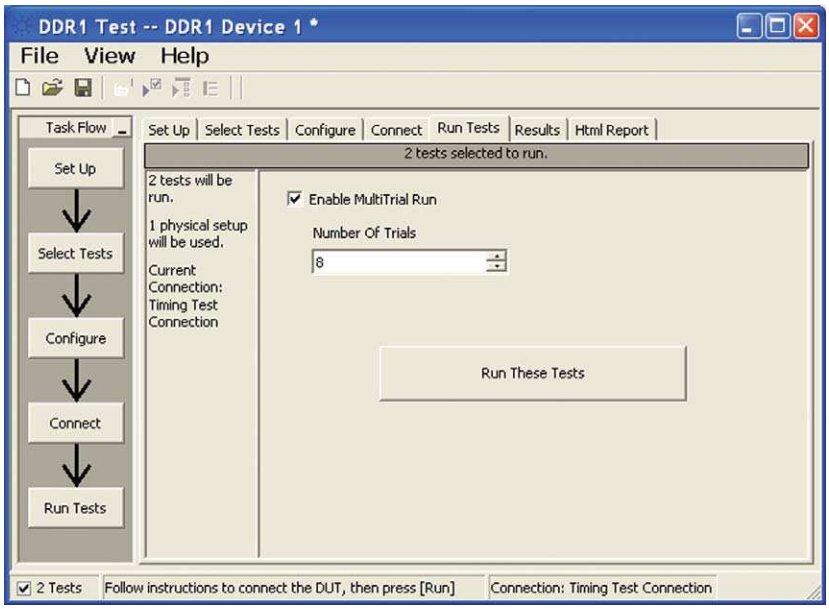


Figure 4. The Repetitive Run feature allows you to run the selected tests until the stop condition is met. It allows you to extensively test the performance of your device.

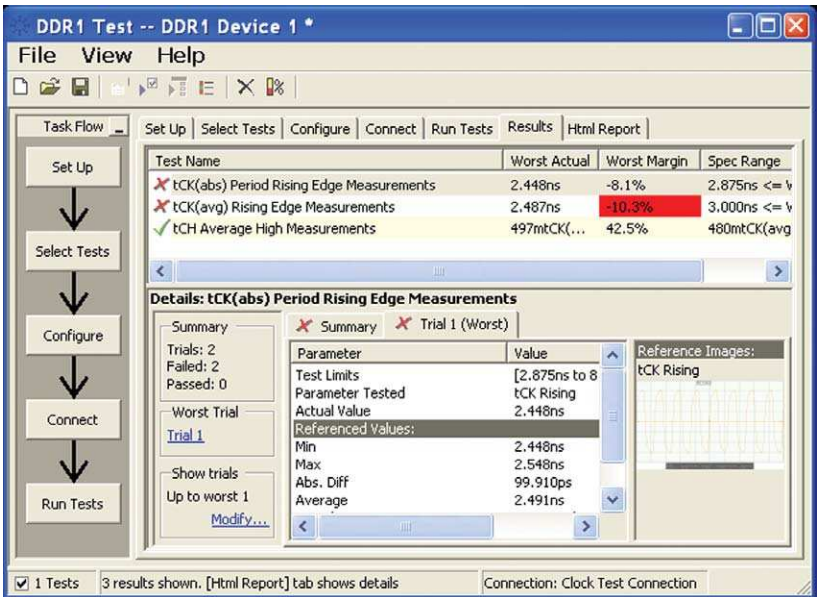
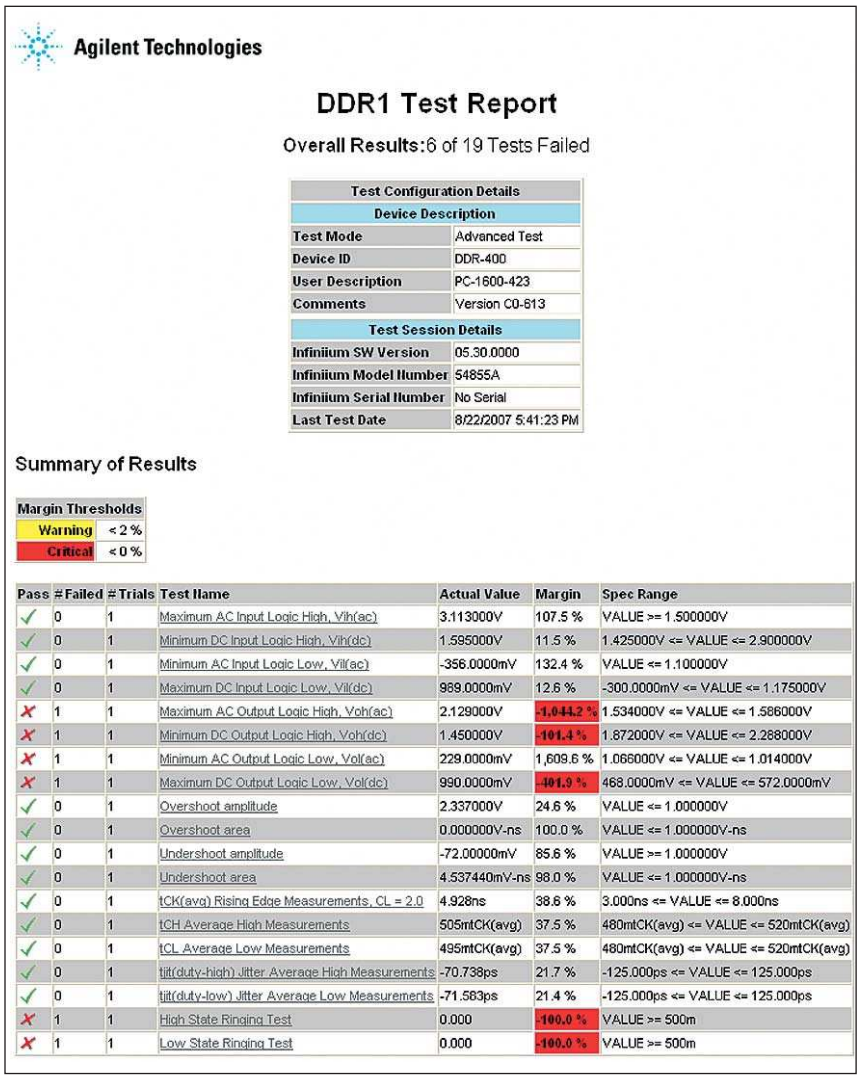


Figure 5. The DDR1 test application documents your test parameters, pass or fail status, test specification range, measured values and the pass/fail margin.

Thorough performance reporting

The U7233A DDR1 compliance test application generates thorough HTML reports that capture the performance, status and margins of your device. It also captures screen shots of critical measurements for your reference and documentation. This report is suitable for printing and sharing with your vendors, customers or colleagues.



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DDR1 Test Report

Overall Results: 6 of 19 Tests Failed

Test Configuration Details	
Device Description	
Test Mode	Advanced Test
Device ID	DDR-400
User Description	PC-1600-423
Comments	Version C0-813
Test Session Details	
Infiniium SW Version	05.30.0000
Infiniium Model Number	54855A
Infiniium Serial Number	No Serial
Last Test Date	8/22/2007 5:41:23 PM

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	Maximum AC Input Logic High, Vih(ac)	3.113000V	107.5 %	VALUE >= 1.500000V
✓	0	1	Minimum DC Input Logic High, Vih(dc)	1.585000V	11.5 %	1.425000V <= VALUE <= 2.900000V
✓	0	1	Minimum AC Input Logic Low, Vil(ac)	-356.0000mV	132.4 %	VALUE <= 1.100000V
✓	0	1	Maximum DC Input Logic Low, Vil(dc)	989.0000mV	12.6 %	-300.0000mV <= VALUE <= 1.175000V
✗	1	1	Maximum AC Output Logic High, Voh(ac)	2.129000V	-1,044.2 %	1.534000V <= VALUE <= 1.586000V
✗	1	1	Minimum DC Output Logic High, Voh(dc)	1.450000V	-101.4 %	1.872000V <= VALUE <= 2.288000V
✗	1	1	Minimum AC Output Logic Low, Vol(ac)	229.0000mV	1,609.6 %	1.066000V <= VALUE <= 1.014000V
✗	1	1	Maximum DC Output Logic Low, Vol(dc)	990.0000mV	-101.9 %	468.0000mV <= VALUE <= 572.0000mV
✓	0	1	Overshoot amplitude	2.337000V	24.6 %	VALUE <= 1.000000V
✓	0	1	Overshoot area	0.000000V-ns	100.0 %	VALUE <= 1.000000V-ns
✓	0	1	Undershoot amplitude	-72.00000mV	85.6 %	VALUE >= 1.000000V
✓	0	1	Undershoot area	4.537440mV-ns	98.0 %	VALUE <= 1.000000V-ns
✓	0	1	tCK(avg) Rising Edge Measurements, CL = 2.0	4.928ns	38.6 %	3.000ns <= VALUE <= 8.000ns
✓	0	1	tCH Average High Measurements	505mtCK(avg)	37.5 %	480mtCK(avg) <= VALUE <= 520mtCK(avg)
✓	0	1	tCL Average Low Measurements	495mtCK(avg)	37.5 %	480mtCK(avg) <= VALUE <= 520mtCK(avg)
✓	0	1	tjit(duty-high) Jitter Average High Measurements	-70.738ps	21.7 %	-125.000ps <= VALUE <= 125.000ps
✓	0	1	tjit(duty-low) Jitter Average Low Measurements	-71.583ps	21.4 %	-125.000ps <= VALUE <= 125.000ps
✗	1	1	High State Ringing Test	0.000	-100.0 %	VALUE >= 500m
✗	1	1	Low State Ringing Test	0.000	-100.0 %	VALUE >= 500m

Figure 6. The DDR1 test application generates a summary report where you can see your device's test results quickly and clearly. Details are available for each test including the test limits, test description and test results, including saved waveforms. In addition, the pass/fail margin is indicated to give you further insight.

Extensibility

You may add additional custom tests or steps to your application using the N5467A User Defined Application (UDA) development tool (www.agilent.com/find/uda). Use UDA to develop functional "Add-Ins" that you can plug into your application.

Add-ins may be designed as:

- Complete custom tests (with configuration variables and connection prompts)
- Any custom steps such as pre or post processing scripts, external instrument control and your own device control

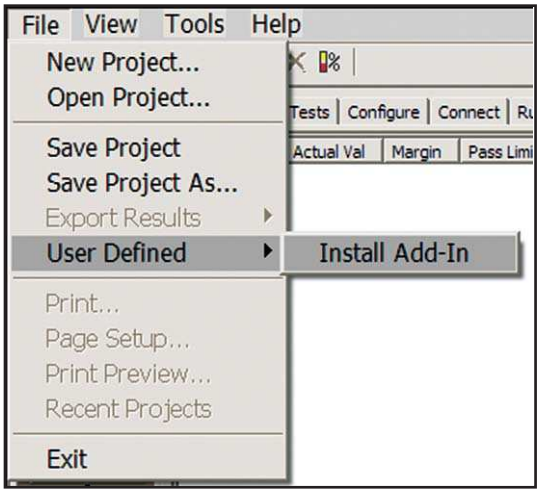

Figure 7. Importing a UDA Add-In into your test application.

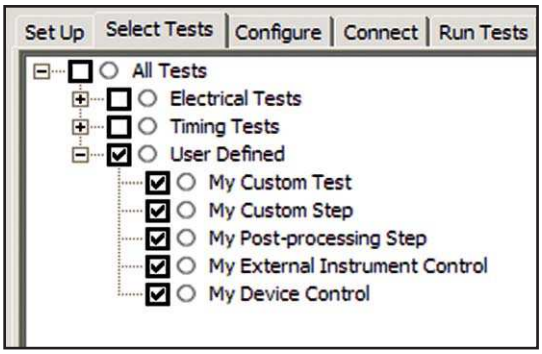

Figure 8. UDA Add-In tests and utilities in your test application.

Automation

You can completely automate execution of your application's tests and Add-Ins from a separate PC using the included N5452A Remote Interface feature (download free toolkit from www.agilent.com/find/scope-apps-sw). You can even create and execute automation scripts right inside the application using a convenient built-in client.

The commands required for each task may be created using a command wizard or from "remote hints" accessible throughout the user interface.

Using automation, you can accelerate complex testing scenarios and even automate manual tasks such as:

- Opening projects, executing tests and saving results
- Executing tests repeatedly while changing configurations
- Sending commands to external instruments
- Executing tests out of order

Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive:

- Interact with your device controller to place it into desired states or test modes before test execution.
- Configure additional instruments used in your test suite such as a pattern generator and probe switch matrix.
- Export data generated by your tests and post-process it using your favorite environment, such as MATLAB, Python, LabVIEW, C, C++, Visual Basic etc.
- Sequence or repeat the tests and "Add-In" custom steps execution in any order for complete test coverage of the test plan.

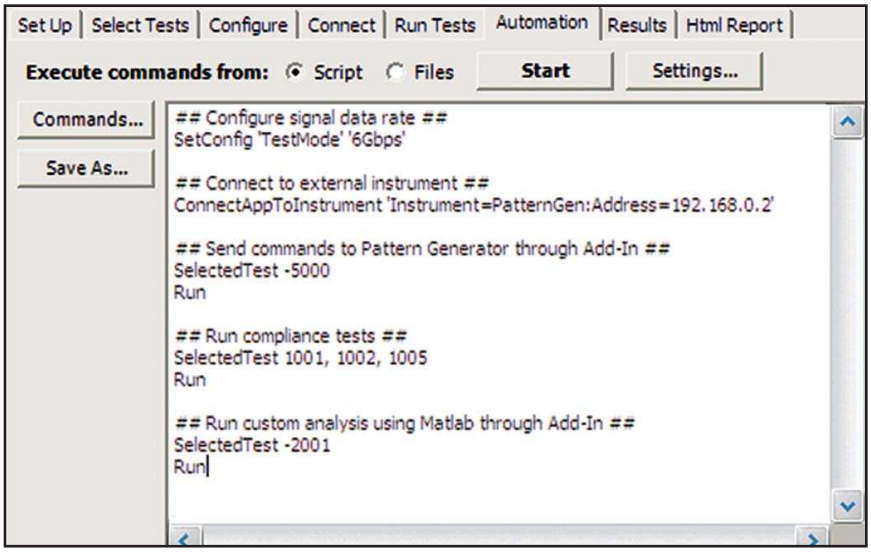

Figure 9. Remote Programming script in the Automation tab.

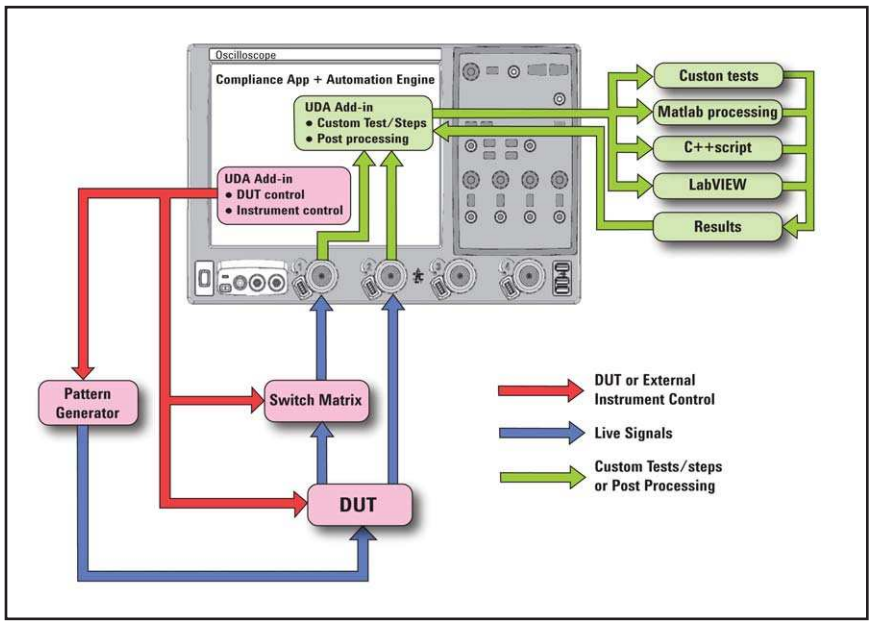

Figure 10. Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive.

System device requirements

In order to speed your test time, you must use the appropriate RAM test reliability software with the memory system to generate random activity on the memory bus. Memtest, is commonly used RAM reliability test software that can run on DOS, Windows® and Linux systems.

Test performed

The Agilent U7233A DDR1 compliance test application covers clock, electrical and timing parameters of the JEDEC JESD79E DDR SDRAM Specifications and JESD209A Low Power Double Data Rate (LPDDR) SDRAM Specifications. The application helps you test all DDR1 devices for compliance, using an Agilent 9000 or 90000 Series Infiniium oscilloscope.

In addition, the test application's Advanced Debug feature provides popular test methodologies that are not covered in any specification. These tests help users who want to perform extensive validation beyond the test specification. It also sets up the scope to isolate the read and write signals so you can immediately jump in to debug the signals.

Table 1. JEDEC tests covered by the U7233A test application

	Speed supported			
Specification	**DDR-200**	**DDR-266**	**DDR-333**	**DDR-400**
AC and DC input measurement levels				
Table 6 (JESD79E – AC Electrical Characteristics and DC Operating Conditions (page 51)	x	x	x	x
Table 7 (JESD79E) – AC Operating Conditions (page 52)	x	x	x	x
Table 8 (JESD79E) – Low Power DDR SDRAM Electrical Characteristics (page 52)	x	x	x	x
Table 13 (JESD79E) – Input Slew Rate for DQ, DQS and DM (page 60)	x	x	x	x
Table 15 (JESD209A) – Output Slew Rate Characteristics (page 63)	x	x	x	x
Table 16 (JESD209) – AC Overshoot/Undershoot Specification (page 63)	x	x	x	x
Table 20 (JESD79E) – AC Overshoot/Undershoot Specification for Address and Control Pins (page 61)	x	x	x	x
Table 21 (JESD79E) – Overshoot/ Undershoot Specification for Data, Strobe, and Mask Pins (page 61)	x	x	x	x
Electrical characteristics and AC timing				
Table 11 (JESD79E) – Electrical Characteristics and AC Timing Part A: DDR333, DDR266, DDR200 Devices (page 56)	x	x	x	
Table 11 (JESD79E) – Electrical Characteristics and AC Timing Part B: DDR400A, DDR400B, DDR400C (page 57)				x
Table 12 (JESD79E) – AC Timing Variations for DDR333, DDR266 and DDR200 Devices (page 58)	x	x	x	
Table 14 (JESD209A) – AC Timing Variations for LPDDR Devices (page 59)	x	x		

Table 2. Advanced Debug feature covered by the U7233A test application

Measurement items	Speed supported
All JEDEC tests from compliance mode	User configurable
High/low state ringing test	User configurable

Oscilloscope compatibility

The U7233A DDR1 compliance test application is compatible with Agilent 9000 or 90000 Series oscilloscopes with operation software revision 2.0 or higher and 8000/80000 Series oscilloscopes with operation software revision 5.70 or higher (Windows XP Pro). For oscilloscopes with earlier software revisions, free upgrade software is available at **http://www.agilent.com/find/scope-apps-sw**

DDR1 data rate	Recommended oscilloscope	Bandwidth	Sampling rate
Up to 400 MT/s	DSO/MSO9104A	1 GHz	10 GSa/s
	DSO/MSO9254A	2.5 GHz	10 GSa/s
	DSO/MSO9404A	4 GHz	10 GSa/s
	DSO/DSA90254A	2.5 GHz	20 GSa/s
	DSO/DSA90404A	4 GHz	20 GSa/s
	DSO/DSA90604A	6 GHz	20 GSa/s
	DSO/DSA90804A	8 GHz	40 GSa/s
	DSO/DSA91204A	12 GHz	40 GSa/s
	DSO/DSA91304A	13 GHz	40 GSa/s

Note:
1. Recommended 1 GHz bandwidth or greater for full characterization
2. Option 005 noise reduction is recommended for 4-GHz or higher bandwidth Infiniium 90000/80000 Series oscilloscopes.
3. The JEDEC JESD79E or JESD209A Specification does not specify the rise time and fall time for DDR1 signals. The required oscilloscope bandwidth is also not mentioned. It is advisable for you to determine the oscilloscope bandwidth required for your DDR1 signals based on the fastest rise time and fall time of the signals in your DDR1 device. Please refer to Table 3.

For 9000 and 90000 Series oscilloscopes, you can choose the oscilloscope bandwidth using the calculation below.

Maximum signal frequency content = 0.5/fastest rise or fall time (10 - 90%)
Scope bandwidth required = 1.4x maximum signal frequency for 3% accuracy measurement
Scope bandwidth required = 1.2x maximum signal frequency for 5% accuracy measurement
Scope bandwidth required = 1.0x maximum signal frequency for 10% accuracy measurement

Table 3. Infiniium 9000 and 90000 Series oscilloscope rise/fall time specifications

Rise time/fall time	90254A	90404B	90604A	90804A	91204A	91304A
10 – 90%	140 ps	105 ps	70 ps	54 ps	35 ps	32 ps

Ordering information

To purchase the U7233A DDR1 compliance test application for your new or existing Infiniium 8000, 80000, 9000 and 90000 Series oscilloscope, order the following:

Oscilloscope requirements for Infiniium 8000 Series oscilloscope

Model number	Description
DSO8000 or MSO8000	Infiniiium Series scope with software 5.70 or higher
U7233A	DDR1 compliance test application (Option N5435A-021 for application server license)
N5415A	InfiniiScan event identification software (Option 009 on new oscilloscopes)
116x/113xA[1, 2]	InfiniiMax I/II probe amplifier (minimum quantity 3 required)

Oscilloscope requirements for Infiniium 9000 and 90000 Series oscilloscope

Model number	Description
9000/90000 or 80000	Infiniiium Series scope with software 2.0 or higher Infiniiium Series scope with software 5.70 or higher
U7233A or N5459A	DDR1 compliance test application (Option 031 on new 90000 Series oscilloscope or Option N5435A-021 for application server license) DDR 1, 2 and 3 Software Bundle Option (contain options U7233A, N5413A and U7231A)
E2688A	High-speed serial data analysis and clock recovery software (option 003 on new 9000 or 90000 Series oscilloscopes or option N5435A-003 for application server license)
N5415A	InfiniiScan event identification software (Option 009 on new 9000 Series oscilloscopes)
N5414B	InfiniiScan event identification software (Option 009 on new 90000 Series oscilloscopes)
116xA/113xA[1,2]	InfiniiMax I/II probe amplifier (minimum quantity 3 required)

1 Ensure that the probe amplifier meets the bandwidth requirement for your signal measurements. Refer to the "Probe accessories" section below to configure the probe head to go with your probe amplifier.

2 For multiple RANK testing, a quantity of 4 probes are required for additional probing of Chip Select (CS) pin.

Probe accessories

InfiniiMax probe amplifiers

Model number	Description
1169A	12-GHz differential probe amplifier
1168A	10-GHz differential probe amplifier
1134A	7-GHz differential probe amplifier
1132A	5-GHz differential probe amplifier
1131A	3.5-GHz differential probe amplifier
1130A	1.5-GHz differential probe amplifier

Probe accessories

InfiniiMax probe heads

Model number	Description
N5381A	InfiniiMax II 12-GHz differential solder-in probe head and accessories
N5382A	InfiniiMax II 12-GHz differential browser
E2677A	InfiniiMax 12-GHz differential solder-in probe head and accessories
E2675A	InfiniiMax 6-GHz differential browser probe head and accessories
N5425A	InfiniiMax 12-GHz ZIF probe head
N5426A	ZIF tips (x10)
N5451A	Long Wire ZIF tips (x10)
E2678A	InfiniiMax 12-GHz differential socketed probe head and accessories
E261xA/B	Wedge Adapters to work with E2678A for probing DDR1 TSOP (3 – 8 signals)
E264xA	Wedge Adapters to work with E2678A for probing DDR1 TSOP (16 signals)
W2637A	x16 LPDDR BGA probes for oscilloscopes and logic analyzers
W2638A	x32 LPDDR BGA probes for oscilloscopes and logic analyzers
W2639A	LPDDR scope probe adapter

Related literature

Publication title	Publication type	Publication number
Agilent Infiniium DSO/DSA 90000A Series Oscilloscopes and InfiniiMax Probes	Data Sheet	5989-7819EN
Infiniium 8000 Series Oscilloscopes	Data Sheet	5989-4271EN
Infiniium DSO80000B Series Oscilloscopes and InfiniiMax Series Probes	Data Sheet	5989-4606EN
Agilent InfiniiScan Event Identification Software for Infiniium Series Oscilloscopes N5414A and 5415A)	Data Sheet	5989-4605EN
Infiniium Series Oscilloscope Probes, Accessories, and Options	Selection Guide Data Sheet	5968-7141EN
Agilent Technologies E2688A, N5384A High-Speed Serial Data Analysis and Clock Recovery Software for Infiniium Series Oscilloscopes	Data Sheet	5989-0108EN
Agilent Technologies EZJIT and EZJIT Plus Jitter Analysis Software for Infiniium Series Oscilloscopes	Data Sheet	5989-0109EN
A Time-Saving Method for Analyzing Signal Integrity in DDR Memory Buses	Application Note	5989-6664EN
W2637A, W2638A, and W2639A LPDDR BGA Probes for Logic Analyzers and Oscilloscopes	data Sheet	5990-3892A

Product Web site

For the most up-to-date and complete application and product information, please visit our product Web site at:
www.agilent.com/find/u7233a

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