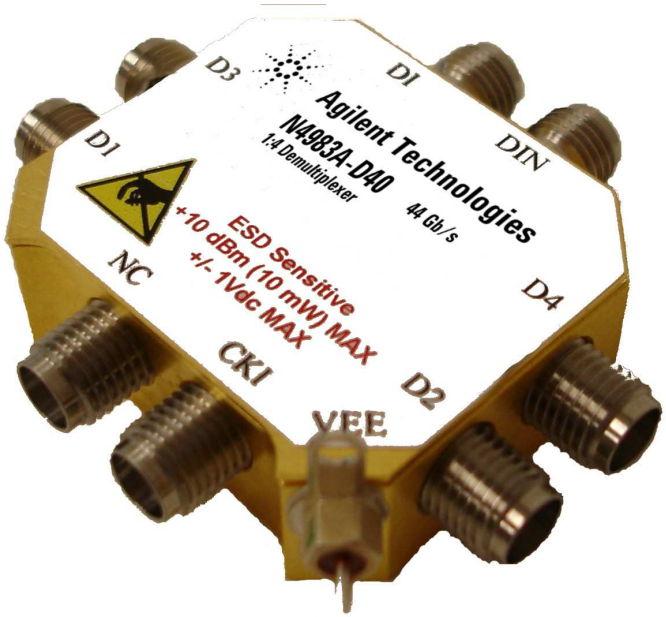
Agilent

N4983A Multiplexer and Demultiplexer Data Sheet

Telecom and datacom applications

- 44 Gb/s 4:1 multiplexer
- 44 Gb/s 1:4 demultiplexer
- Broad bandwidth
- High input sensitivity
- Low power dissipation
- Precision connectors

N4983A-M40 44 Gb/s 4:1 multiplexer (MS4S1V1M)

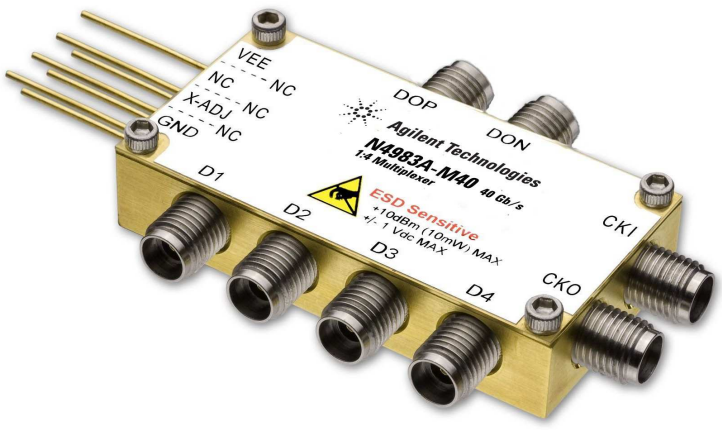


N4983A-D40 44 Gb/s 1:4 demultiplexer (MD1S4V1M)

N4983A-M40 mulitplexer 4:1, 44 Gb/s

Features

- Half rate clock
- High input sensitivity
- Wide operating range, 2 to 44 Gb/s
- Low output jitter
- Low power consumption
- Fast output rise/fall times



Description

The N4983A-M40 (MS4S1V1M) is a broadband 4 to 1 MUX with continuous coverage from 2 to 44 Gb/s. The four quarter-rate data inputs are single-ended and AC-coupled, while the full-rate data output is fully differential and DC-coupled. The MUX accepts a half-rate input clock and returns a quarter-rate output clock for driving other circuits. A clock crossing adjustment pin allows correction for duty cycle distortion. Power supply bias of negative 3.6 V is required.

Applications

The N4983A-M40 multiplexer 4:1, 44 Gb/s (MS4S1V1M) can be used with existing equipment to generate higher rate bit streams for use in telecom applications up to 44 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors, and excellent output waveform characteristics. The compact size of the module allows the N4983A-M40 multiplexer 4:1, 44 Gb/s (MS4S1V1M) to be placed at the measurement plane, reducing or eliminating artifacts related to long cables.

Parameter	Minimum	Typical	Maximum	Units
Operating conditions				
Vee	–3.7	–3.6	–3.5	V
Key specifications @ 25 °C				
Vee= –3.6V, Iee = 560 mA, Zo = 50 Ω				
Data input				
Bit rate	0.5	–	11	Gb/s
Amplitude	100	–	1000	mVpp
Clock input				
Frequency	1	–	22	GHz
Amplitude	200	–	1400	mVpp
Power	-10	–	+7	dBm
Data output				
Bit rate	2	–	44	Gb/s
Amplitude (single-ended)	450	500	600	mVpp
Jitter RMS	–	0.5	1	psec
Jitter Pk-Pk	–	2.5	4	psec
Rise time (20/80)	–	8	10	psec
Fall time (20/80)	–	8	10	psec
SNR	10	–	–	dB
Clock output				
Frequency	0.5	–	10	GHz
Amplitude	300	–	450	–

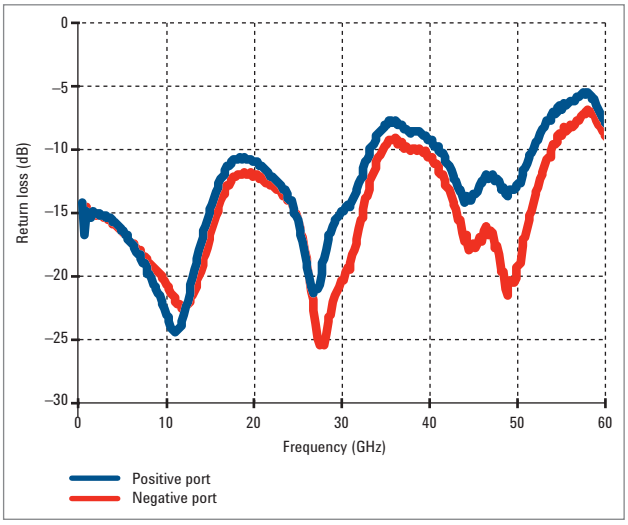


Figure 1. Data output return loss

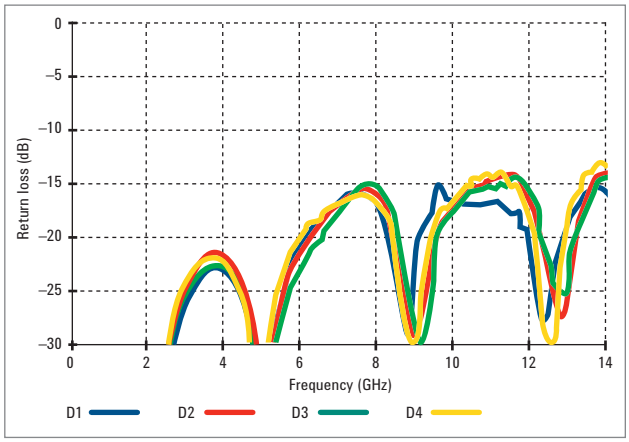


Figure 2. Data input return loss

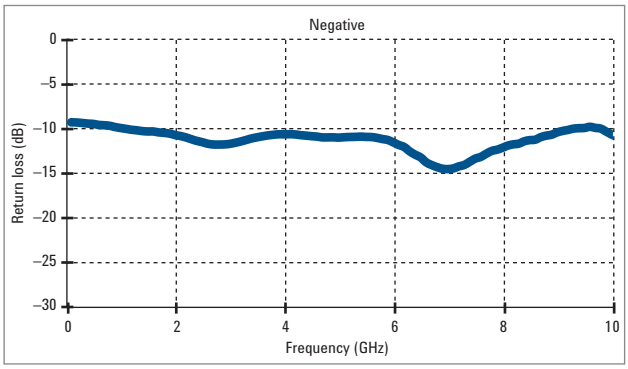


Figure 3. Clock output return loss

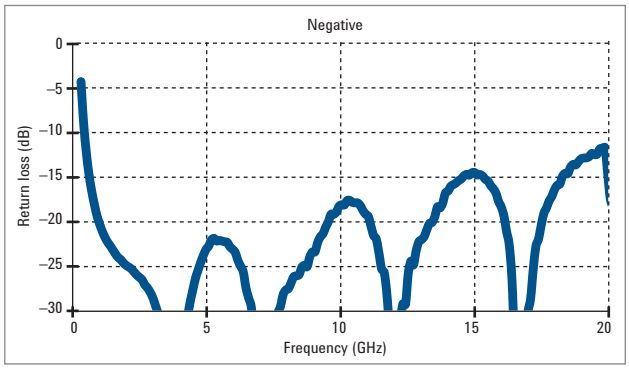


Figure 4. Clock input return loss

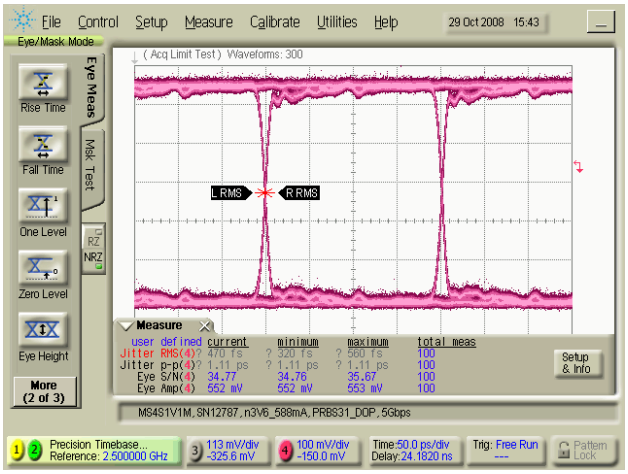


Figure 5. Data output waveform @ 5 Gb/s Four 1.25 Gb/s, 2 e31-1 data inputs

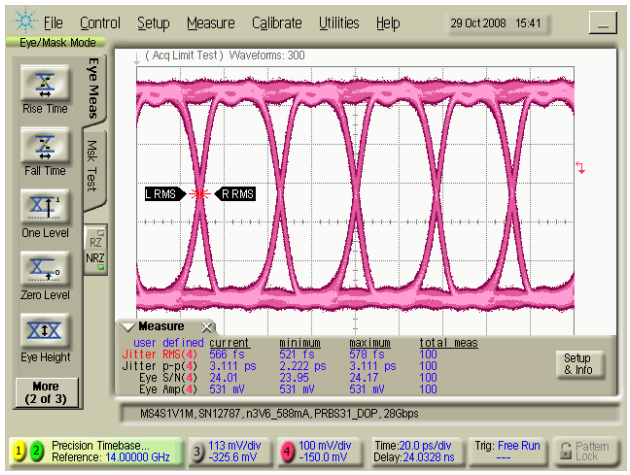


Figure 6. Data output waveform @ 28 Gb/s. Four 7 Gb/s, 2 e31-1 data inputs

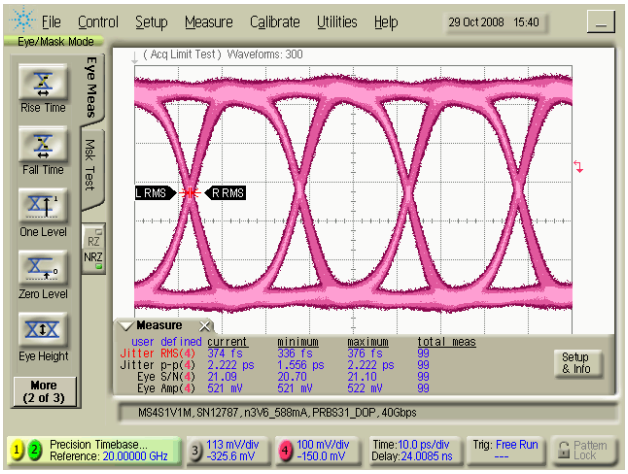


Figure 7. Data output waveform @ 40 Gb/s. Four 10 Gb/s, 2 e31-1 data inputs

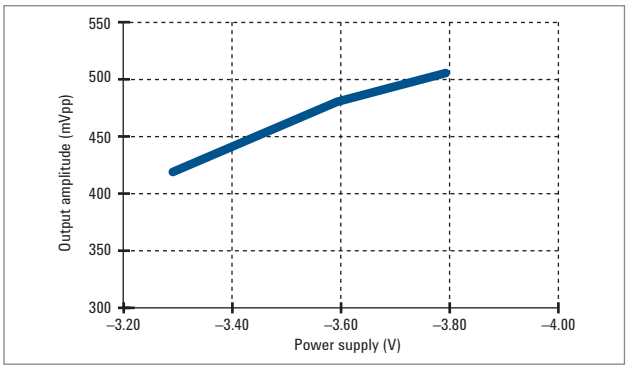


Figure 8. Data output amplitude vs power supply. Data rate @ 40 Gb/s

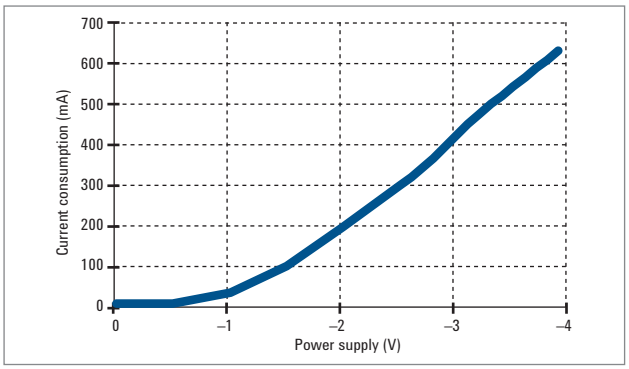


Figure 9. Power supply current vs voltage

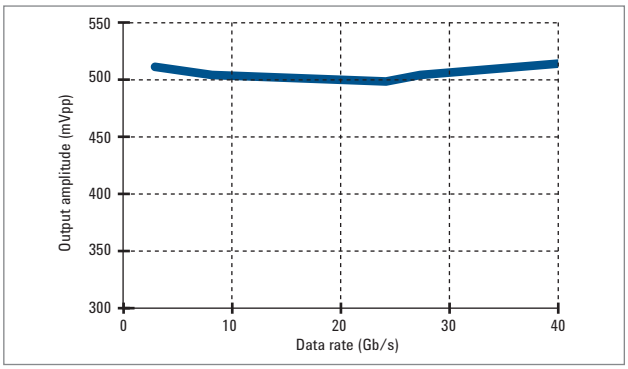


Figure 10. Data output amplitude vs data rate. Power supply @ –3.6 V

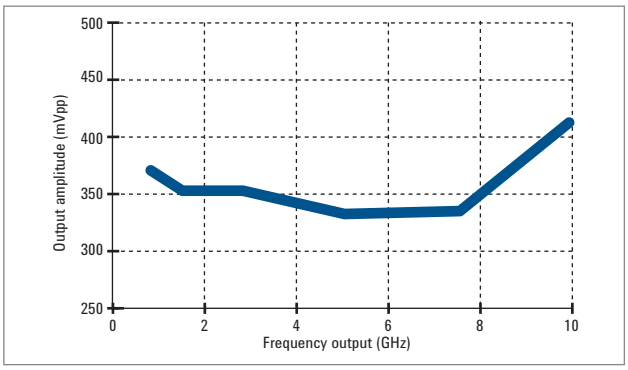


Figure 11. Clock output amplitude vs frequency. Power supply @ –3.6 V

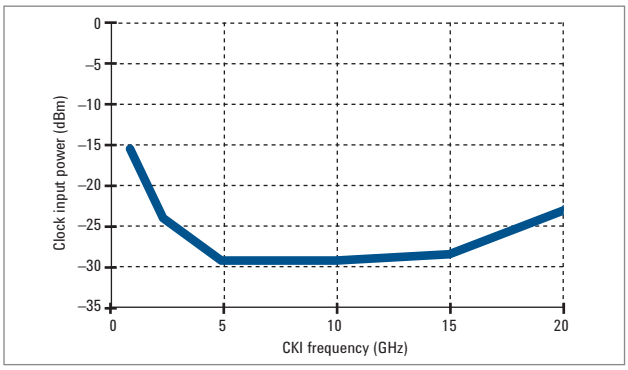


Figure 12. Clock input sensitivity vs frequency. Power supply @ –3.6 V

Timing diagram

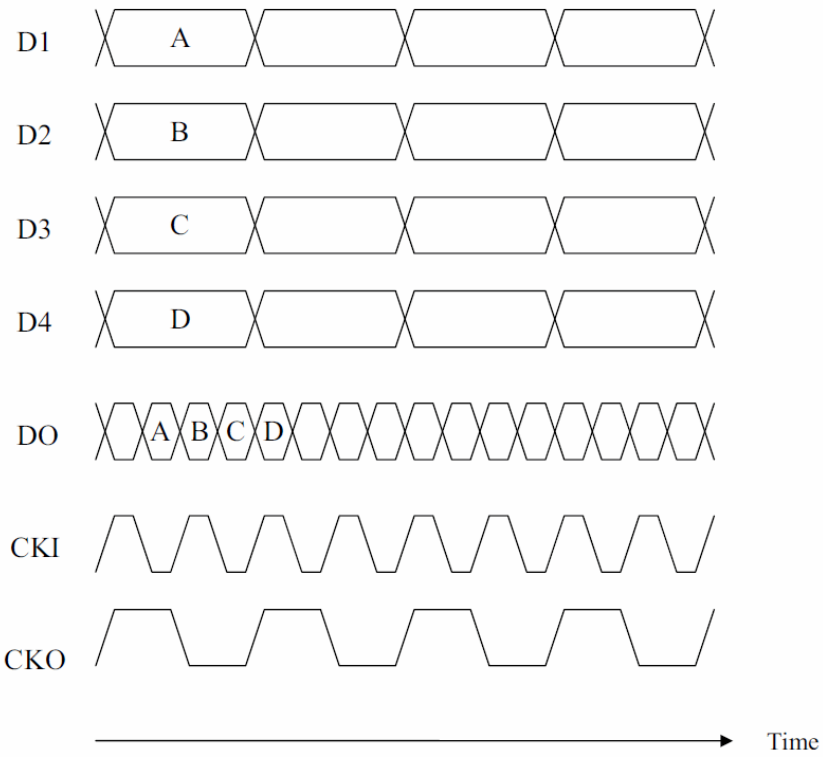


Figure 13. Timing diagram
Note: Phase relationship between signals not implied.

Functional block diagram

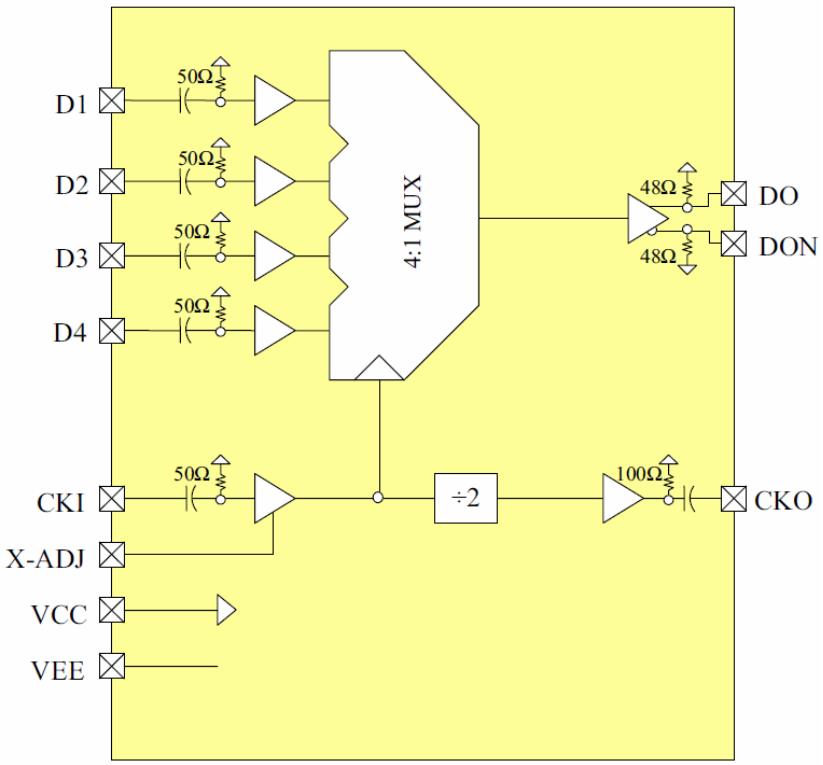


Figure 14. Functional block diagram

Clock cross-over adjustment

The duty cycle of the input clock can have adverse affects on eye quality when deviating from 50%. Non-50% duty cycle is referred to as “duty cycle distortion” (DCD). DCD on the input clock will directly translate to double-tracking on the output eye, because adjacent bits would have unequal pulse-widths. DCD can happen by various means. For example, amplifiers operating in the non-linear regime when driven with large signals can often lead to un-evenly clipped waveforms and hence DCD. As another example, mismatches in differential circuits can cause voltage offsets between the differential signals thus leading to DCD. For these reasons, DCD can vary with frequency, temperature, and process variations.

The N4983A-M40 multiplexer 4:1, 44 Gb/s (MS4S1V1M) addresses the issue of clock DCD by providing an analog cross-over control for the input clock. This control pin allows the user to correct for a wide range of clock DCD. The cross over control is terminated internally with a 25 Ω load, and can accommodate a voltage range of ± 40 mV. An external attenuator or resistor in series is recommended to prevent from overdriving and damaging this sensitive input (see figure for example). Note that the cross-over range is limited to the rise/fall times of the input clock.

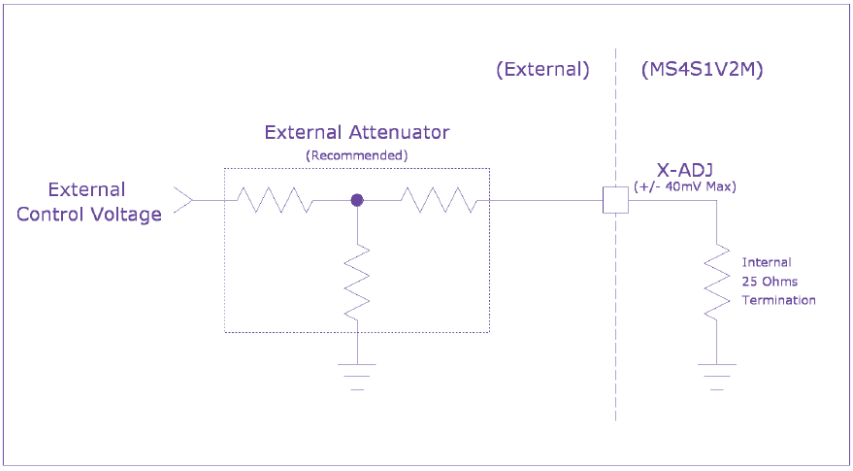


Figure 15. N4983A-M40 (MS4S1V1M) clock cross-over adjust control

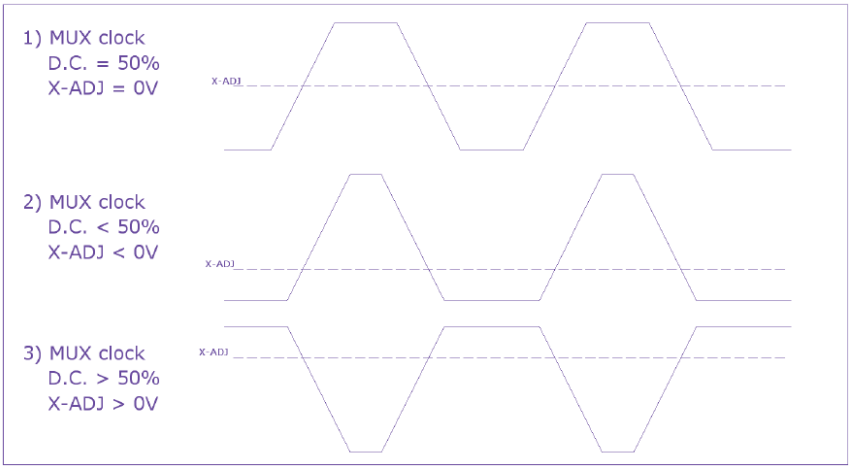


Figure 16. N4983A-M40 (MS4S1V1M) clock duty cycle waveforms

Module outline

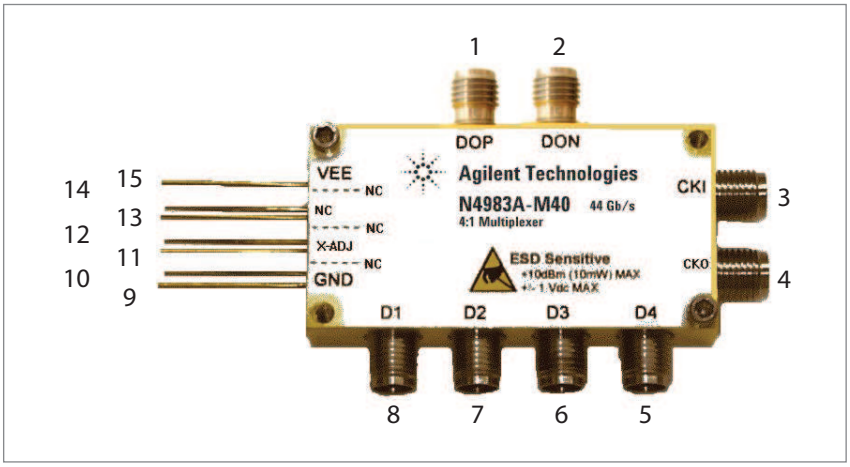


Figure 17. Outline

Absolute maximum ratings

Parameter	Value	Units
Supply voltage (VEE)	–4.0 V	V
Clock input power (CKI)	+10	dBm
Data input (D1, D2, D3, D4)	2.0	Vpp
DC voltage (CKI, D1, D2, D3, D4)	± 0.5 V	V
Operating temperature	0 to 70	°C
Storage temperature	–85 to 125	°C

Pin description

Name	PIN	Description	Notes	Connector
DOP	1	Data channel output	Positive terminal of differential output	2.92 mm (K)
DON	2	Data channel output	Negative terminal of differential output	2.92 mm (K)
CKI	3	Clock input	½ of bit rate, e.g. 22 GHz for 44 Gb/s, Single-ended input	2.92 mm (K)
CKO	4	Clock divided output	¼ of bit rate, e.g. 11 GHz for 44 Gb/s, Single-ended output	2.92 mm (K)
D4	5	Data channel input - bit position 4	Trailing/last serial data bit	2.92 mm (K)
D3	6	Data channel input - bit position 3	–	2.92 mm (K)
D2	7	Data channel input - bit position 2	–	2.92 mm (K)
D1	8	Data channel input - bit position 1	Leading/first serial data bit	2.92 mm (K)
VCC	9	RF & DC ground	Chassis/Module connection	–
X-ADJ	11	Clock cross-over adjust	± 40 mV max, 25 Ω	–
VEE	15	Negative supply voltage	–3.6 V @560 mA, DC PIN	–
NC	10, 12 to 14	No connect	–	–

Packaging information

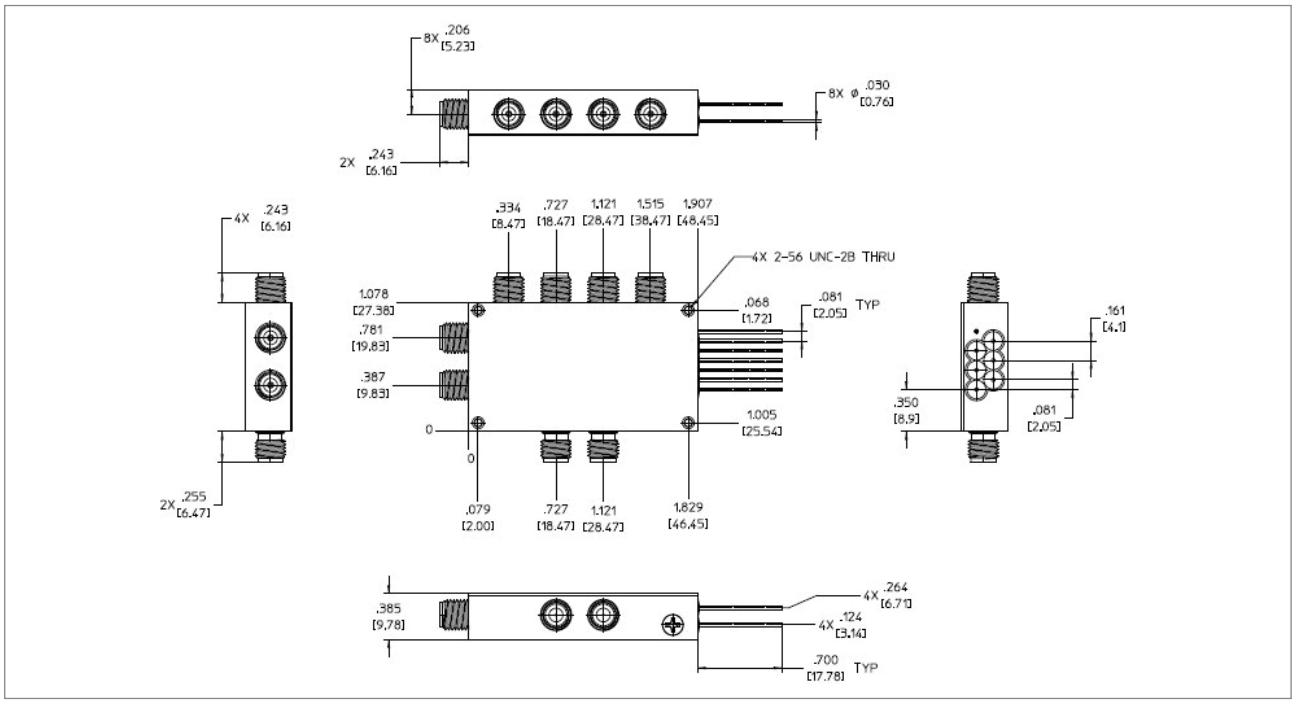


Figure 18. All measurements in inches [mm]

N4983A-D40 demultiplexer 1:4, 44 Gb/s

Features

- Half rate clock
- High input sensitivity
- Wide operating range, 2.6 to 44 Gb/s
- Low output jitter
- Low power consumption
- Fast output rise/fall times

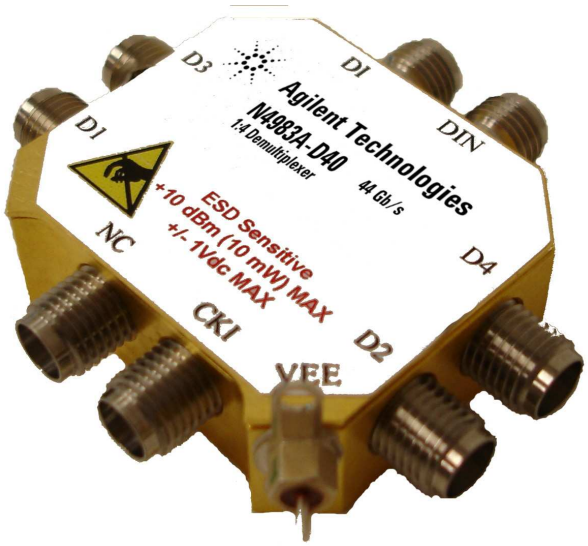
Description

The N4983A-D40 (MD1S4V1M) is a 1:4, 44 Gb/s demultiplexer. The module accepts input data rates from 2.6 to 44 Gb/s with an input sensitivity less than 200 mV-se. Differential data inputs are DC coupled and terminated with 50 Ω resistors to minimize reflections. The single-ended, half rate clock input is AC coupled and operates with low input power. The module features single-ended AC coupled outputs with ECL compatible signal levels. Data outputs, clock input, and high-speed inputs are accessed via high quality 2.9 mm (K) connectors.

Applications

The N4983A-D40 demulitplexer 1:4, 44 Gb/s (MD1S4V1M) can be used in SONET/SDH applications operating at transmission speeds within the demuliplexer's 2.6 to 44 Gb/s input rate.

Broadband test systems will benefit from the low power dissipation, precision connectors, and excellent output waveform characteristics. The compact size of the module allows the N4983AD40 demulitplexer 1:4, 44 Gb/s (MD1S4V1M) to be placed at the measurement plane, reducing or eliminating artifacts related to long cables.



Parameter	Minimum	Typical	Maximum	Units
Operating conditions				
Vee	–3.7	–3.5	–3.5	V
Key specifications @ 25 °C				
Vee = –3.6 V, Iee = 290 mA, Zo = 50 Ω				
Data input				
Bit rate	2.6	–	44	Gb/s
Amplitude (single-ended)	150	–	1000	mVpp
Clock input				
Frequency	1.3	–	22	GHz
Amplitude	200	–	1400	mVpp
Power	–10	–	+7	dBm
Data output				
Bit rate	0.65	–	11	Gb/s
Amplitude	210	240	270	mVpp
Jitter RMS	–	0.8	1.2	psec
Jitter Pk-Pk	–	6	8	psec
Rise time	–	8	10	psec
Fall time	–	8	10	psec
SNR	10	–	–	dB

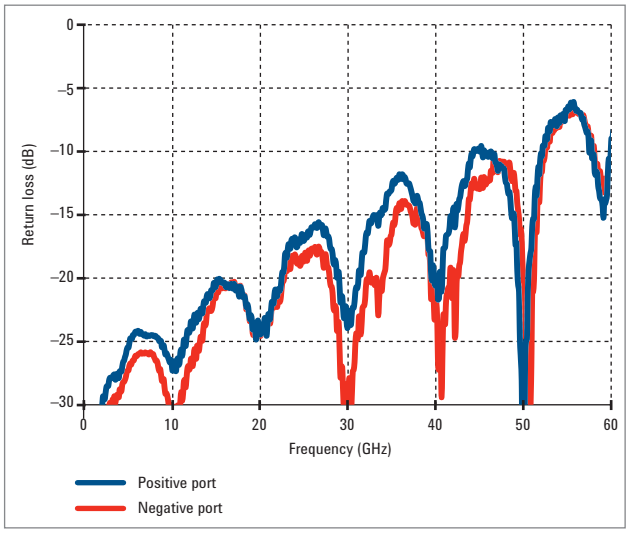


Figure 19. Data input return loss

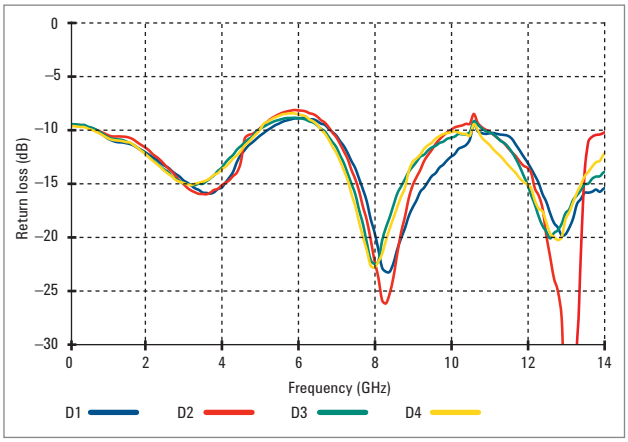


Figure 20. Data output return loss

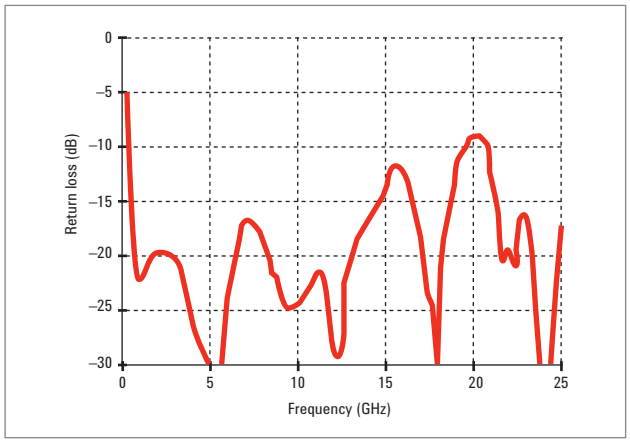


Figure 21. Clock input return loss

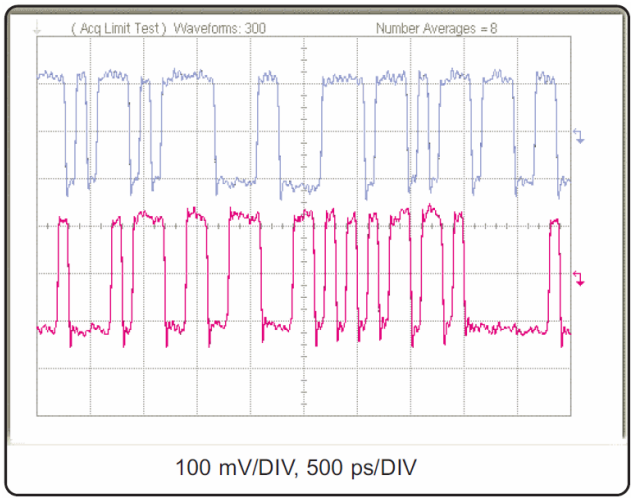


Figure 22. Data output waveforms @ 10 Gb/s. Top: D3, Bottom: D4

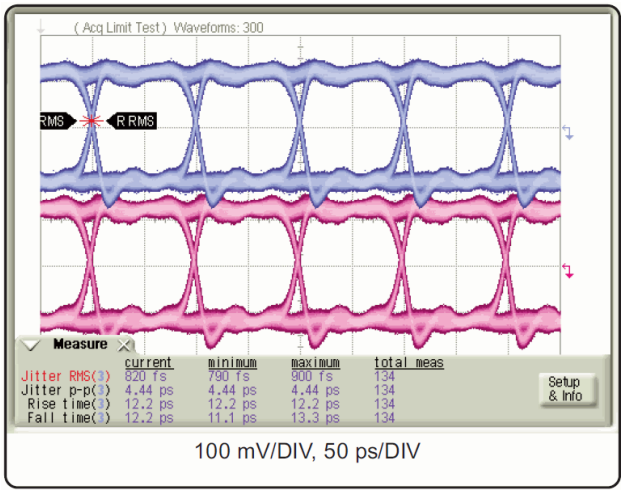


Figure 23. Data output eye diagrams @ 10 Gb/s. Top: D1, Bottom: D2

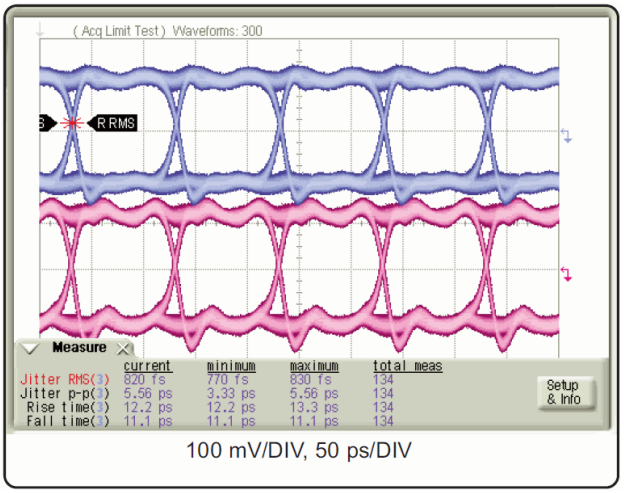


Figure 24. Data ouput eye diagrams @ 10 Gb/s. Top: D3, Bottom: D4

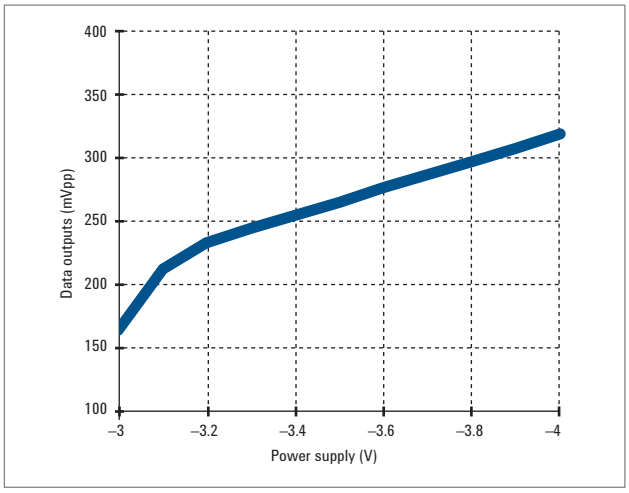


Figure 25. Data output amplitude vs power supply level. Output data rate @ 10 Gb/s

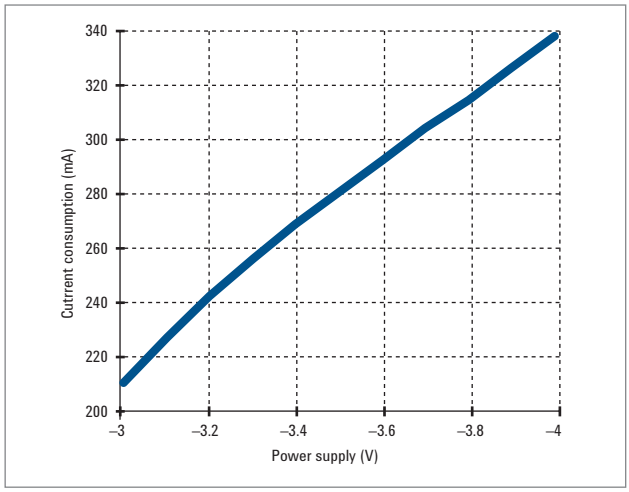


Figure 26. Total current consumption vs power supply level

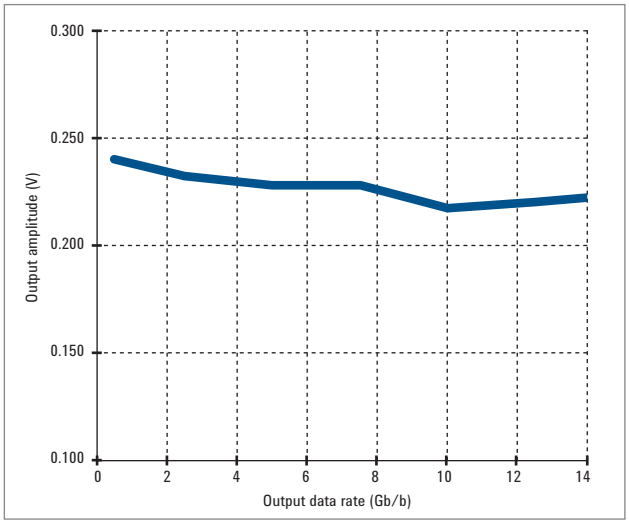


Figure 27. Data output amplitude vs data rate. Power supply @ –3.6 V.

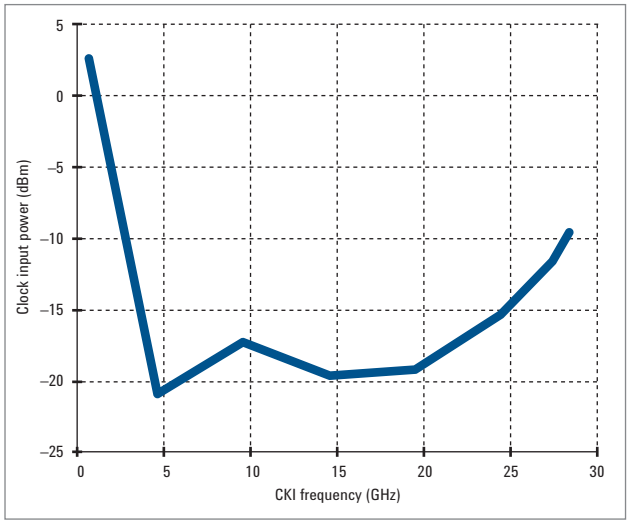


Figure 28. Clock input sensitivity vs frequency. Power supply @ –3.6 V.

Timing diagram

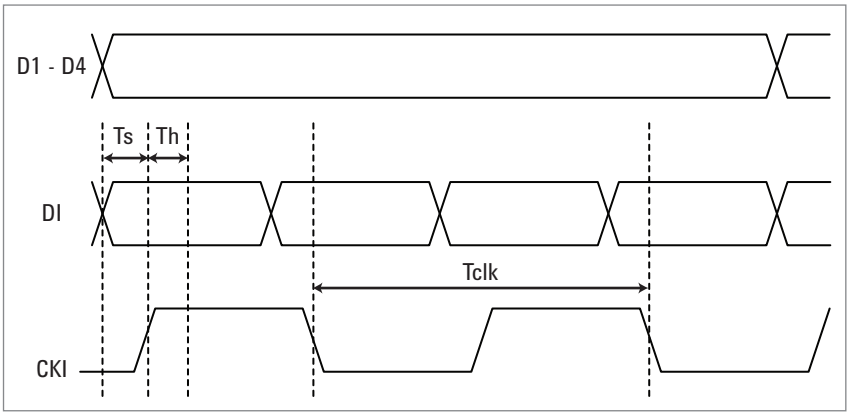


Figure 29. Timing diagram

Parameter	Description	Minimum	Typical	Maximum
Ts (ps)	Setup time	4	–	–
Th (ps)	Hold time	4	–	–
DI (Gb/s)	Input data	2.6	–	44
D1-D4 (Gb/s)	Output data	0.5	–	11
CKI (GHz)	Input clock	1	–	22

Functional block diagram

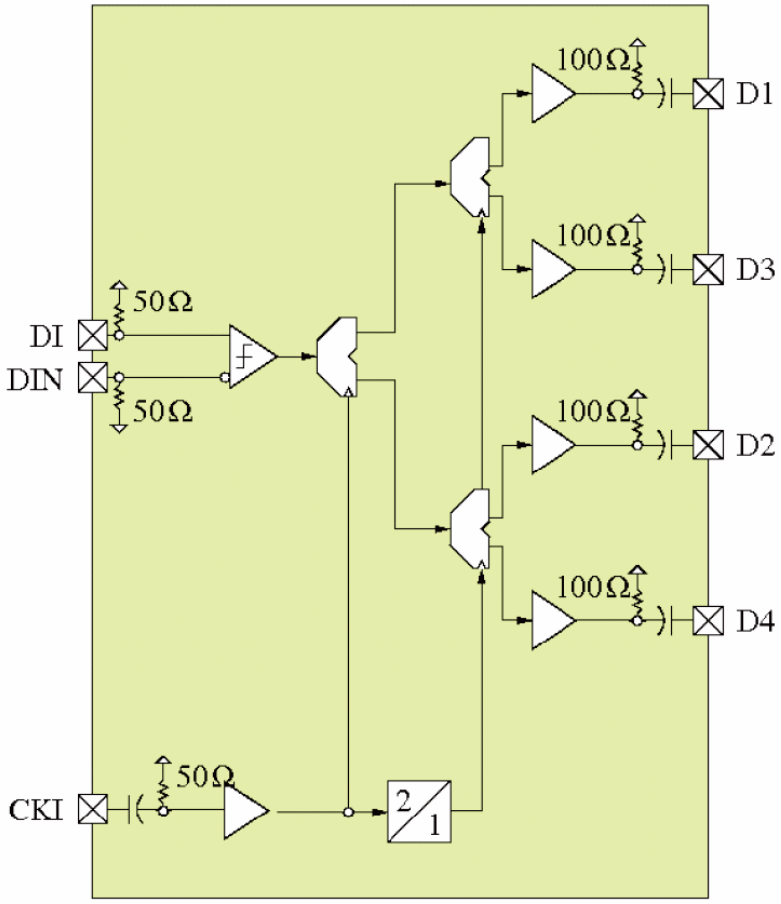


Figure 30. Block diagram

Module outline

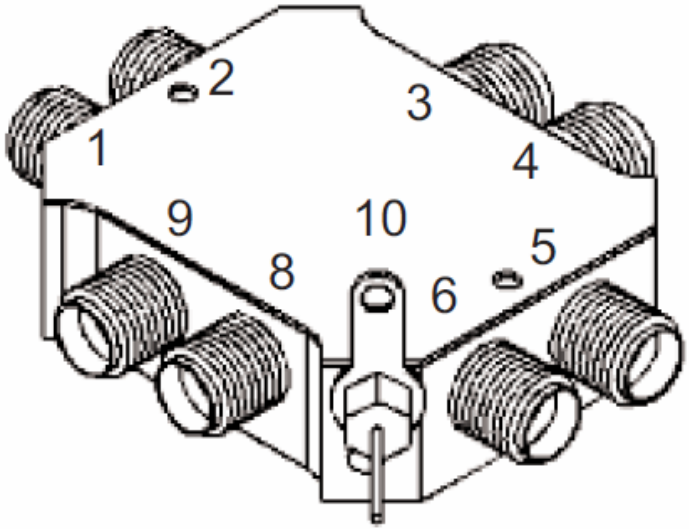


Figure 31. Module outline

Absolute maximum ratings

Parameter	Value	Unit
Supply voltage (VEE)	–4.0	V
Data input (DI, DIN)	2.0	Vpp
Clock input power (CKI)	+10	dBm
DC voltage (CKI, DI, DIN)	± 0.5	V
Operating temperature	–40 to 85	°C
Storage temperature	–85 to 150	°C

Pin description

Name	PIN	Description	Note	Connector
D1	1	Data channel output - bit position 1	Leading/first serial data bit	2.92 mm (K)
D3	2	Data channel output - bit position 3	Third bit	2.92 mm (K)
D1	3	Data channel input	Positive terminal of differential input	2.92 mm (K)
DIN	4	Data channel input	Negative terminal of differential input	2.92 mm (K)
D4	5	Data channel output - bit position 4	Trailing/Last bit	2.92 mm (K)
D2	6	Data channel output - bit position 2	Second bit	2.92 mm (K)
VEE	7	Negative supply voltage	DC pin, –3.6V @290 mA	–
CKI	8	Clock input	Half of bit rate, ie: 20 GHz for 40 Gb/s Single-ended input	2.92 mm (K)
VCC	9	RF & DC ground	Chassis/Module connection	–
NC	11	No connect	–	–

Packaging information

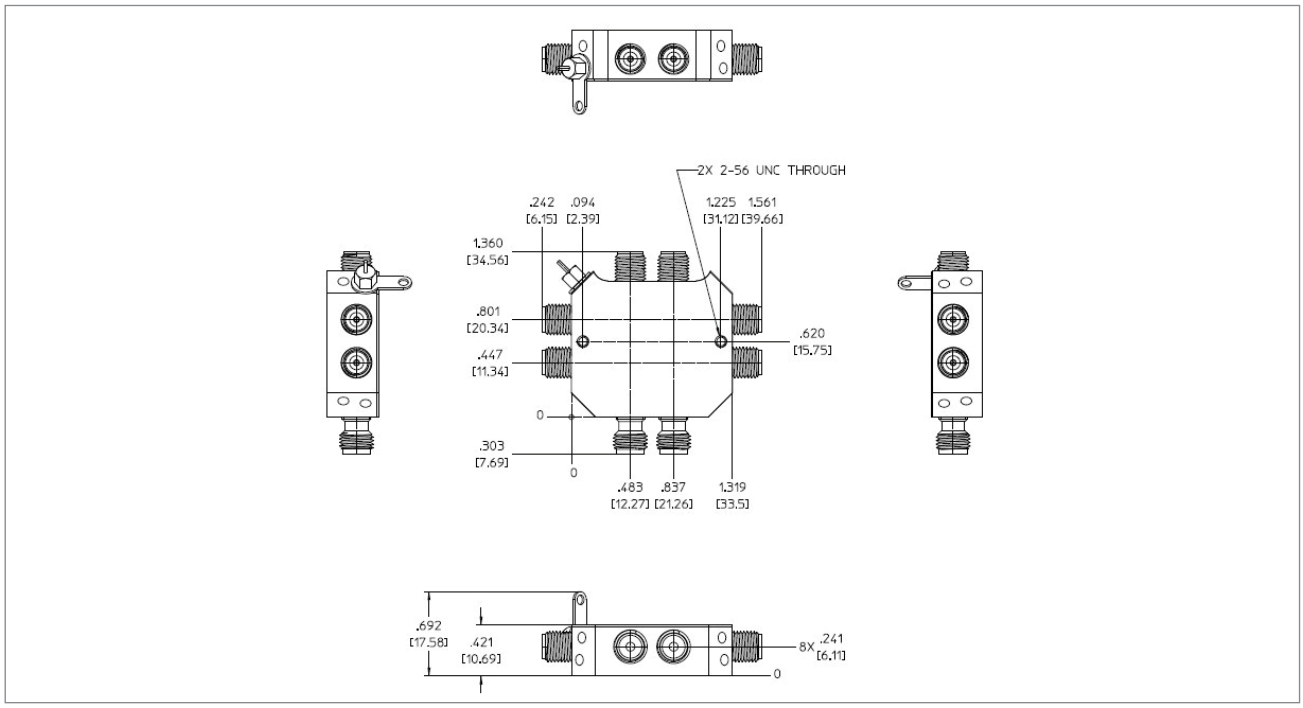


Figure 32. All measurements in inches [mm]

Ordering Information

N4983A multiplexer and demultiplexer (MS4S1V1M/MD1S4V1M), includes standard 1-year warranty.

Warranty and calibration service

For warranty and calibration service information, contact your local authorized Agilent distributor or Agilent sales department.

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