Agilent
N4984A Clock Divider

Data Sheet

For microwave, communications, and test applications

Features

- Divide by 1/2/4/8
- Wide operating range
- Fast rise/fall times
- Low jitter
- Excellent signal quality

N4984A-020
- 0.2 to 20 GHz
- Divide by 1/2/ 4/8 (TD20MCA)

N4984A-040
- 0.2 to 40 GHz
- Divide by 2/4/8 (TD40MCA)

Anticipate ___Accelerate ___Achieve

Agilent Technologies

N4984A-020 Clock Divider

Features

- Wide frequency range: 0.2 to 20 GHz
- High input sensitivity
- Very low phase noise
- Fast rise/fall times
- Divide-by-1/2/4/8 outputs
- AC power supply included
- Size: 3.5″ x 4.0″ x 1″

Description

The N4984A-020 clock divider (TD20MCA) divider is a general purpose test accessory designed for microwave, communications and test applications. The accessory provides divide-by-1, divide-by-2, divide-by-4, or divide-by-8 output. Inputs and outputs are AC coupled. The divider is self contained and plugs into standard AC power sources.

Application

The N4984A-020 clock divider (TD20MCA) divider can be used to extend the trigger range of high speed sampling oscilloscopes. Precision timebase measurements will benefit from the very low added jitter and fast waveform edges. The N4984A-020 clock divider (TD20MCA) can be used to generate synchronized, high frequency clocks from existing sinusoidal, synthesized sources. The low 1/f phase noise characteristics of the divider will benefit high frequency phase lock loop designs.

Key specifications (specifications pertain to measurements @ 25 °C)

Parameter	Description	Minimum	Typical	Maximum
F_{in} (GHz)	Input frequency	DC*	—	20
P_{in} (dBm)	Nominal input power	–10	0	+10
P_{out} (dBm)	Nominal output power	–5	+5	—
£(dBc/Hz)	SSB phase noise @10 kHz offset	—	–153	—
$P_{spitback}$ (dBm)	Freq/2 power spitback @input	—	TBD	—
$P_{fundamental}$ (dBm)	Fundamental feedthru @output	—	TBD	—

**Low frequency limit dependent on input edge speed*

Frequency Divider Application

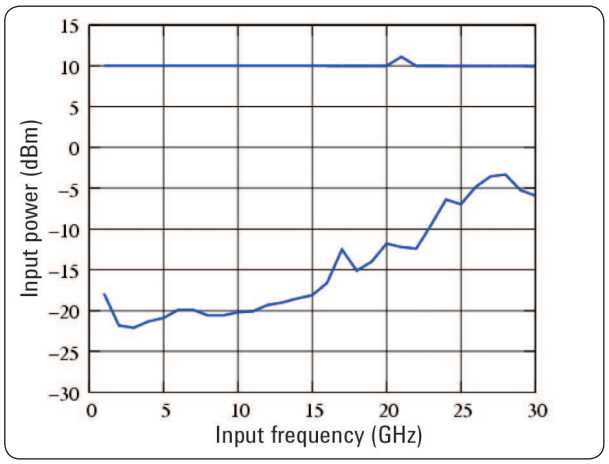

Figure 1. Min/Max single-ended power Input sensitivity window

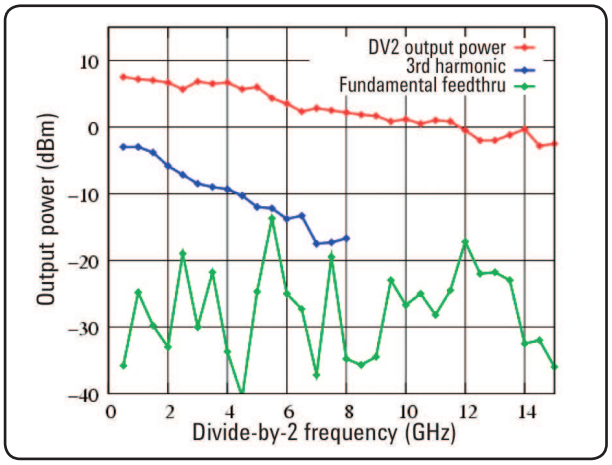

Figure 2. Binary divide-by-2 output power, 3rd harmonic & input feedthru

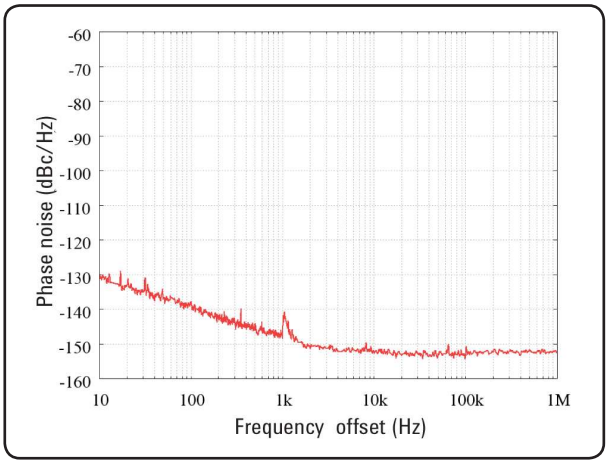

Figure 3. N4984A-020 clock divider (TD20MCA): SSB phase noise for binary divide-by-8 configuration input freq = 7.8 GHz, gain S21

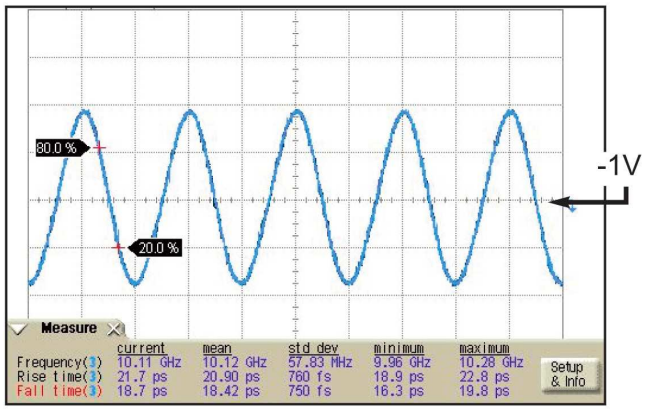

Figure 4. Binary divide-by-2 configuration Input freq = 20 GHz, 150 mV/div

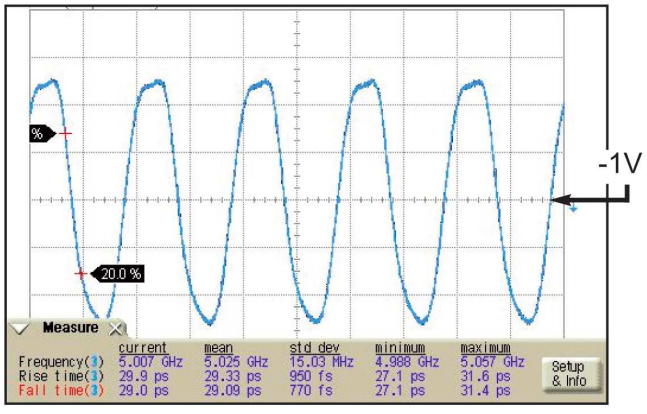

Figure 5. Binary divide-by-4 configuration Input freq = 20 GHz, 150 mV/div

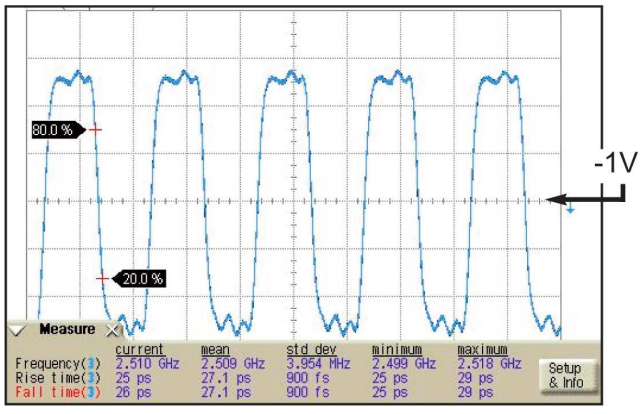

Figure 6. Binary divide-by-8 configuration Input freq = 20 GHz, 150 mV/div

N4984A-040 Clock Divider

Features

- Wide frequency range: 0.2 to 40 GHz
- High input sensitivity
- Very low jitter
- Fast rise/fall times
- Divide-by-2/4/8 outputs
- AC power supply included
- Size: 3.5″ x 4.0″ x 1″

Description

The N4984A-040 clock divider (TD40MCA) divider is a general purpose test accessory designed for microwave, communications and test applications. The accessory simultaneously provides divide-by-2, divide-by-4, and divide-by-8 outputs. The single-ended input is accessed from the rear via a 2.9 mm connector while the outputs are provided at the front panel via SMA connectors. All inputs and outputs are AC coupled. The divider is self contained and plugs into standard AC power sources.

Application

The N4984A-040 clock divider (TD40MCA) divider can be used to extend the trigger range of high speed sampling oscilloscopes. Precision timebase measurements will benefit from the very low added jitter and fast waveform edges. The N4984A-040 clock divider (TD40MCA) can be used to generate synchronized, high frequency clocks from existing sinusoidal, synthesized sources. The low 1/f phase noise characteristics of the divider will benefit high frequency phase lock loop designs.

Key specifications (specifications pertain to measurements @ 25 °C)

Parameter	Description	Minimum	Typical	Maximum
S11 (dB)	Input return loss	—	–10	—
S22 (dB)	Div-by-2 output return loss	—	–12	—
S33 (dB)	Div-by-4 output return loss	—	–10	—
S44 (dB)	Div-by-8 output return loss	—	–10	—
Jrms (fs)	Output RMS jitter	—	< 400	500
Trf (ps)	Output rise/fall times	—	30	35
F_{max} (GHz)	Maximum division frequency	38	40	—
P_{in} (dBm)	Nominal input power	—	0	+10
P_{out} (dBm)	Nominal output power	–6	–3	—
L (dBc/Hz)	SSB phase noise @ 100 kHz offset	—	–153	—

Frequency Divider Application

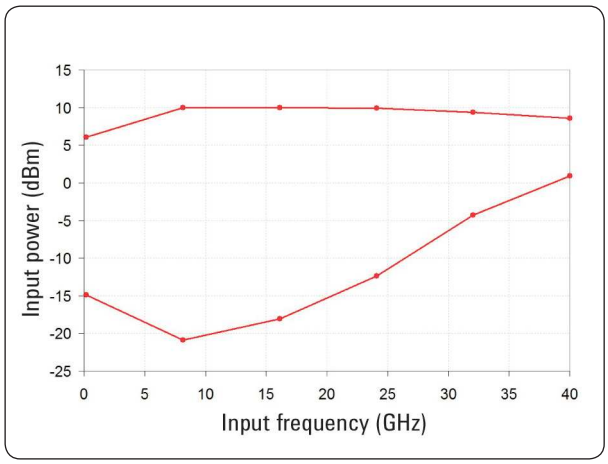

Figure 7. Input sensitivity window min/max single-ended input power

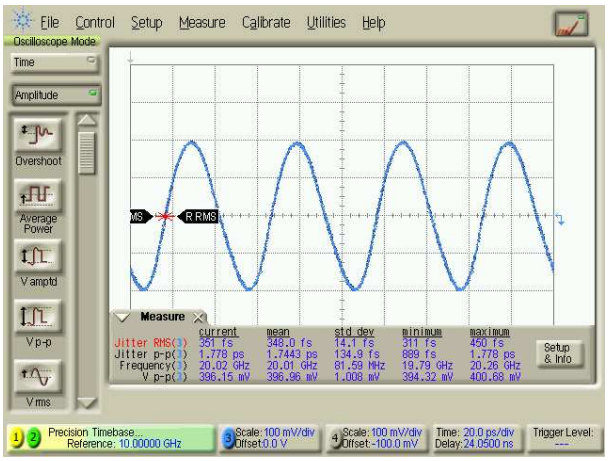

Figure 8. Divide-by-2 output waveform input signal: 40 GHz @ 0 dBm

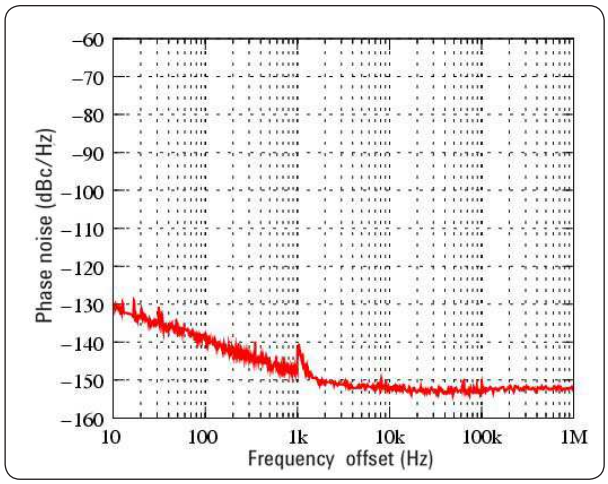

Figure 9. SSB phase noise of div-by-8 port input freq = 7.8 GHz

Figure 10. N4984A-040 clock divider (TD40MCA) front panel

Figure 11. N4984A-040 clock divider (TD40MCA) rear panel

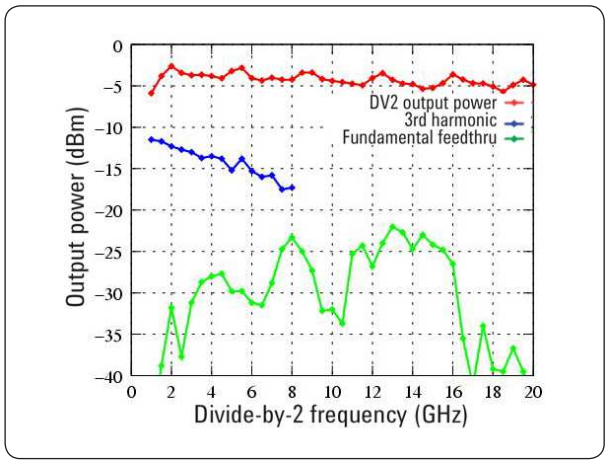

Figure 12. Divide-by-2 output power, 3rd harmonic & input feedthru

Functional Block Diagram

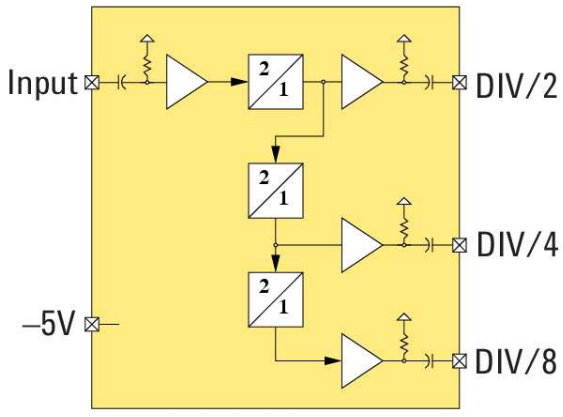

Figure 13. Functional block diagram

Specifications

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General and Mechanical Parameters	
Operating temperature	+10 to +40 °C
Storage temperature	–40 to +70 °C
Power requirements	42 W External AC Adaptor (included) • 100 to 240 V AC, 50 to 60 Hz, 0.6 A
Physical dimensions (W x H x D)	8.9 x 2.2 x 9.2 cm (3.5 x ⅞ x 3 ⅝ inches)
Weight	0.5 lbs

Regulatory Standards	
EMC	
Complies with European EMC Directive 2004/108/EC	• IEC/EN 61326-1 • CISPR Pub 11 Group 1, class A • AS/NZS CISPR 11 • ICES/NMB-001
This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.	

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Revised: January 6, 2012

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Published in USA, September 6, 2012
5991-0717EN

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