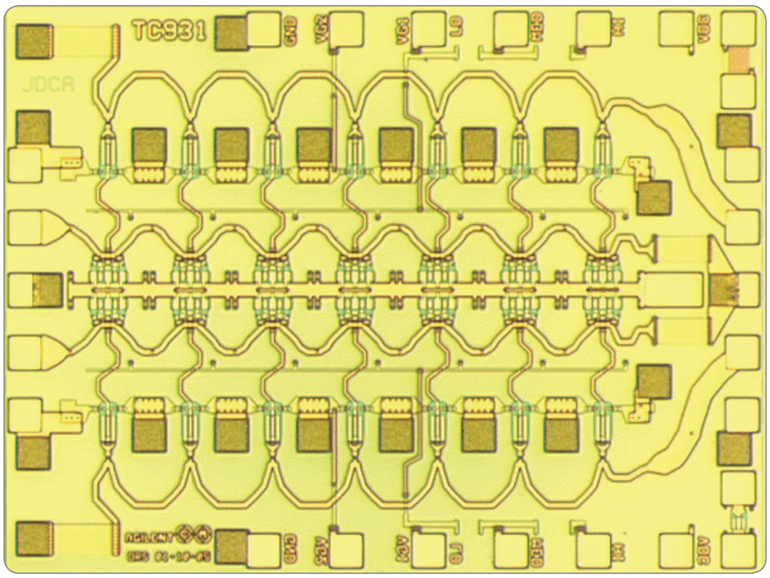
Agilent 1GG6-4080
0.155 – 43 Gb/s Differential I/O, High Power, Output Amplifier

Data Sheet

Features

- Frequency range: 50 GHz (single–ended), 30 GHz (diff.)
- Single–ended or fully differential I/O operation
- Low additive jitter: 600 fs, (43 Gb/s $2^{31} - 1$ PRBS, RMS typ.)
- Fast rise and fall times: t_r/t_f (10–90%, $V_{out, Diff} = 14V_{p-p}$) ≈ 15 ps
- Variable output amplitude control (differential operation): 2 to 14 V_{p-p}
- 20–80% cross–point adjust capability
- Average DC output voltage monitor pads
- Small signal gain: 8 dB (w/diff. input drive)
- High output power/high output diff. voltage:
21 dBm (S.E.) to 30 GHz
14 V_{p-p} (diff.) @ 43 Gb/s
- Output power response flatness: ±1 dB (to 30 GHz)
- Input/output return loss: > 12 dB (typ.)
- On-chip resistive & diode temperature sense capability



Chip size:	1880 × 1410 µm (74.1 × 55.5 mils)
Chip size tolerance:	±10 µm (±0.4 mils)
Chip thickness:	127 ± 15 µm (5 ±0.6 mils)
Pad dimensions:	70 × 70 µm (2.8 × 2.8 mils)

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Description

The 1GG6-4080 High Power, Differential I/O Amplifier is ideally suited as a MZ or LiNO3 Optical Modulator Driver for 10 & 43 Gb/s (NRZ OC-192 & OC-768) communication infrastructure and line-card amplification applications. Each fully differential I/O, integrated circuit is capable of amplifying high-speed clock and data signals with low additive jitter (< 600 fs RMS, PRBS) and fast edge speeds (~15 ps, 10–90% t_r/t_f).

These devices are fabricated using Agilent's PH9B GaAs PHEMT process to deliver ~8 dB differential small signal gain with up to 21 dBm S.E. P_{sat} up to 30 GHz. On-chip bias capabilities allow for variable output amplitude control, cross-point control, monitoring of average DC output voltages and on-chip temperature.

Absolute Maximum Ratings

		Cont. oper[1]		Damage lmt[2]		
Symbol	**Parameters/conditions**	**Min**	**Max**	**Min**	**Max**	**Units**
$R_{LOADA,B}$	Load Resistance to ground for each output	45	55	25	75	Ohms
$V_{G2A,B}$	Second gate voltage	–7.75	0	–9	+0.5	Volts
$V_{GIA,B}$	First gate voltage	–18	0	–25	+2	Volts
$V_{SSA,B}$	Common current source voltage	–14	0	–16	+0.5	Volts
$I_{G2A,B}$	Second gate current (per side)	–1	+1	–3	+3	mA
$I_{G1A,B}$	First gate current (per side)	–10	0	–12	+40	mA
$I_{SSA,B}$	Current source current	–350	0	–450	+20	mA
P_{DC}	DC power dissipation		4.55		60	Watts
P_{DIN}	Maximum CW input power (per side)		21		20	dBm
$V_{IN(Diff)}$	Maximum input AC voltage (differential)		14	1		V_{p-p}
CW	Continuous wave operation (sinewave input)	10		1		MHz
Duty cycle	Operating duty cycle in any 0.1usec time interval	45	55	35	65	%
T_{ch}	Operating junction temperature		+150			°C
T_{bs}[3]	Operating chip backside temperature	–10	+65	–20	+100	°C
T_{stg}	Storage temperature			–65	+165	°C
T_{max}	Maximum assembly temp. (for 60 seconds maximum)				300	°C

1. *Operation in excess of any one of these conditions may result in performance and reliability degradation to this component. MTTF degrades by a factor 2 for every 10 degree increase in operating temperature greater than Max. T_{bs}. Parameters specified for continuous operation at $T_{bs} \le 65$ °C*
2. *Operation in excess of any one of these conditions for ≥ 100 mSec may result in permanent damage to this component. Parameters specified at $T_A = 25$ °C, except for temperature specs.*
3. *Measured at chip backside metal to die attach material interface. Operation in excess of $T_{bs} = 65$ °C possible at $I_{SS} < 350$ mA. Contact Agilent for more information.*

DC Specifications/Physical Properties

(T_A= 25 °C, R_{LOAD} = 50 Ohms to 0V, Bias: $V_{G2A,B}$= –7.5 V, $V_{G1LowA,B}$ = –17 V, V_{SS} = Adjusted to I_{SS}= 300 mA[1], $V_{DIN,\overline{DIN}}$ = –3.75 V [unless otherwise specified])[2]

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
$I_{G1A,B}$	First gate current (per side)	–10	–6	–4	mA
ΔI_{G1}	Delta first gate current (I_{G1A}–I_{G1B})	–0.3	0	0.3	mA
$TC\Delta I_{G1}$	I_{G1} balance temperature coefficient: ($\Delta I_{G1[T1]}$–$\Delta I_{G1[T2]}$)/2 °C[3]	–5	0	5	µA/°C
$I_{G2A,B}$	Second gate current (per side)	–0.5	0	0.5	A
V_{SS}	Common source voltage	–14	–12.5	–10	mA
$I_{DIN,\overline{DIN}}$	Data input (data input bar) DC current	–85	–70	–55	mA
$I_{INDelta}$	Delta input DC current	–6	0	+6	mA
$V_{DOUT,\overline{DOUT}bal}$	Output DC voltage (balanced output)	–4.15	–3.55	–2.95	V
$V_{OUTDelta}$	Delta output DC voltage (balanced output, $V_{DOUT} – V_{\overline{DOUT}}$)	–0.75	0	+0.75	V
$I_{DOUT,\overline{DOUT}}$	DC output load current (per side)		75	100	mA
$V_{IN(Diff)}$	Min. differential input voltage to fully switch output		8.0		V_{p-p}
$V_{DOUT,\overline{DOUT}low}$[4]	Low output DC voltage (fully switched output)		–7.5	–7.0	V
$V_{DOUT,\overline{DOUT}high}$[4]	High output DC voltage (fully switched output)	–0.3	–0.01	0	V
$R_{G1A,B}$[5]	First gate DC input resistance (unbiased, per side)	1.6	2.2	2.8	K-ohms
$R_{G2A,B}$[6]	Second gate DC input resistance (unbiased, per side)	0.2	1.1	2.0	M-ohms
R_{SS}[7]	Source node DC input resistance (unbiased)	2.0	26	32	ohms
$R_{DIN,\overline{DIN}}$	Data input (data input bar) DC input resistance (unbiased, open circuit input)	35	47.5	60	ohms
$R_{DOUT,\overline{DOUT}}$[7]	Data output (data output bar) DC output resistance (unbiased, w/external 50Ω termination to 0V)	8	14	20	ohms

1. *VSS = ~ –12.5V.*
2. *All current polarities are positive into device.*
3. *Measured ΔI_{G1} @ T_1,T_2 where $T_2 – T_1$ = 2 °C for –5 °C ≤ T1, T2 ≤ +70 °C.*
4. *$V_{DIN,DIN}$ set to (0,–7.5) or (–7.5,0) to fully switch output High or Low. Device should not be operated continuously in the fully switched condition. Minimum frequency for fully switched operation >= 1 MHz.*
5. *All other nodes short circuited, V_{G1} = –1.0v, $R_{G1} = V_{G1}/I_{G1}$.*
6. *All other nodes short circuited, I_{G2} = +0.5 uA (positive current into device), $R_{G2}= V_{G2}/I_{G2}$. This node is highly non–linear and the resistance value measured is highly dependent on current injected from measurement equipment (i.e. handheld DVM, etc.).*
7. *All other nodes short circuited, V_{SS} = +0.1v, $R_{SS}= V_{SS}/I_{SS}$ or V_{DOUT}= +0.1v, $R_{DOUT}= V_{DOUT}/I_{DOUT}$.*

Frequency-domain RF specifications[1]

(TA = 25 °C, R_{LOAD} = 50 Ohms to 0V, Bias: $V_{G2A,B}$ = –7.5 V, $V_{G1LowA,B}$ = –17 V, V_{SS} = Adjusted to I_{SS} = 300 mA[2], $V_{DIN,\overline{DIN}}$ = –3.75 V [unless otherwise specified])[3]

Symbol	Parameters/conditions	Min.	Typ.	Max	Units
F_{min}[4]	Minimum operating frequency	10			MHz
$F_{max–Diff\ Gain}$	Maximum operating frequency (Diff. gain = Diff. gain (1 GHz) –2 dB		35		GHz
$F_{max–Diff}$	Maximum operating frequency (P_{Sat} = $P_{Sat\ (1\ GHz)}$ –2 dB)		30		GHz
$S21_{min}$	Small signal gain[5] (1– 35 GHz)	0	2.5		dB
ΔS_{21}	Small signal gain flatness (1–25 GHz)		±1.5	±3	dB
Delay	Group delay (1–35 GHz)		44		ps
ΔDelay	Group delay flatness (5–25 GHz)		±9		ps
TC_{Gain}	Temperature coefficient of gain (~25 GHz)		–0.029		ps
RL_{in}	Minimum input return loss (1–35 GHz)	10	18		dB
RL_{out}	Minimum output return loss (1–35 GHz)	10	13		dB
ISO	Reverse isolation (1–35 GHz)		17		dB
P_{1dB}	Output power at 1 dB gain compression (@ F = 25 GHz)		19		dBm
P_{Sat}	Saturated output power at 5 dB gain compression (@ F = 25 GHz)		21		dBm
P_{1dB}	Output power at 1 dB gain compression (@ F=30 GHz)		18		dBm
P_{Sat}	Saturated output power at 5 dB Gain Compression (@ F = 30 GHz)		21		dBm
$P_{Sat–Rolloff}$	Saturated output power roll–off (DC–30 GHz)		2	4	dB
$P_{Sat–Rolloff}$	Saturated output power roll–off (30–50 GHz)		10		dB

1. *Small–signal data obtained via Agilent 8510 series network analyzer, 8565E Spectrum analyzer, 4142 DC modular power supply system. All measurements, single-ended, except where noted. Large signal data obtained via Agilent 83650B 50 GHz source and 8565E 50 GHz spectrum analyzer and other associated test accessories.*
2. V_{SS} = ~ –12.5V.
3. *All current polarities are positive into device.*
4. *RF nodes are DC-coupled, however, device should not be operated continuously in a fully switch manner below 10 MHz.*
5. *Differential gain value is approximately 5 dB greater than S.E. value.*

Time–Domain AC Specifications[1, 2]

(T_A = 25 °C, R_{LOAD} = 50 Ohms to 0V, Bias: $V_{G2A,B}$= –7.5 V, $V_{G1LowA, B}$= –17 V, V_{SS} = Adjusted to I_{SS}= 300 mA[3], $V_{DIN,\overline{DIN}}$ = –3.75 V [unless otherwise specified])

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Data rate	OC–768 NRZ	43			Gb/s
$V_{Out–Max}$	Max. differential output amplitude, 43 Gb/s, 1010 pattern	12	14		V_{p-p}
V_{Amptd}	Eye amplitude, $2^{31} – 1$ PRBS pattern, differential	10	13		V_{p-p}
V_{Height}	Eye height, $2^{31} – 1$ PRBS pattern, differential	9	12		V_{p-p}
T_r/T_f	Rise and fall time (10–90% V_{out} = 13 $V_{p–p}$, 1010 pattern, V_{in}=3.2$V_{p–p}$)		14		psec
Jr_{RMS}	Additive random (intrinsic) RMS jitter (50% data crossing point, 43 Gb, 1010 pattern)		75		fsec
$Jr_{P–P}$	Additive random (intrinsic) peak–peak jitter (50% data crossing point, 43 Gb, 1010 pattern)		450		fsec
Jd_{RMS}	Additive deterministic (pattern dependent) RMS jitter (50% data crossing point, 43 Gb, $2^{31} – 1$ PRBS input jitter)		600		fsec
Jd_{p-p}	Additive deterministic (pattern dependent) peak–peak jitter (50% data crossing point, 43 Gb, $2^{31} – 1$ PRBS Input)		3.6		fsec

1. *All data obtained via single–ended I/O operating mode with unused RF I/O ports terminated into 50 ohms.*
2. *Data obtained via Agilent 81250 43 Gb/s parBERT series Data Pattern Generator and Agilent 86100B digital communications analyzer with low jitter timebase option and 86118A 70 GHz remote sampler head plugin module. Jitter and rise/fall times listed are deconvolved from measurements using the following formula: tr/tf DUT actual = [(tr/tf DUT meas.)2 – (tr/tf system)2]1/2. Test equipment tr/tf limit ~5.4 ps. System jitter RMS limit ~300 fs (1010 Pattern), 400 fs (2^{31}–1 PRBS pattern).*
3. *V_{SS} = ~ –12.5V.*

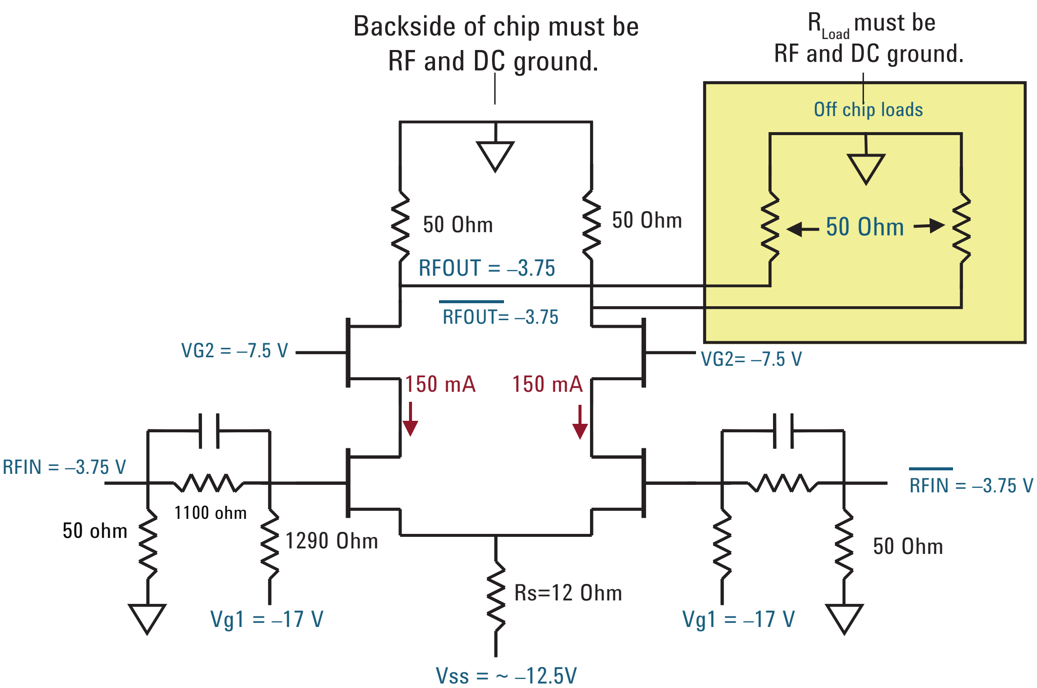

Figure 1. 1GG6-4080 simplified schematic

Applications

The 1GG6-4080 can be used in a variety of high output power, frequency-domain applications through 30 GHz or high-speed time-domain applications requiring good pulse fidelity and high output voltage swings through 43 Gb/s. The device is ideal as a differential I/O, LiNO3 Optical Modulator Driver Amplifier for 10 & 43 Gb/s (NRZ OC-192 & OC-768) communication line card applications.

Biasing and Operation

The device consists of ground referenced, multi–section, cascoded differential amplifier stage. The subscripts "A" & "B" listed in the following voltage descriptions refer to the two sides of the differential structure. $V_{G1A\&B}$ are the negative voltages applied to the common source FET gate networks of all cascoded stages; "A" along one side and "B" along the other side of the device. The $V_{G1A\&B}$ voltages may be varied to accommodate a wide range of common–mode input voltages, typically 3.75 to 0 volts. $V_{G2A\&B}$ are the negative voltages applied to the upper or second FET gates of all cascoded stages. V_{SS} is the negative source voltage bias applied to all cascode FET source contacts. The drains of all cascoded FET sections are terminated to the chip backside providing a "ground reference" design for improved pulse fidelity performance. Typical bias conditions are as follows: $V_{G1A\&B}$ = –17 volts, $V_{G2A\&B}$ = –7.5 volts, and V_{SS} adjusted to 300 mA I_{SS} (typically V_{SS} = –12.5 volts). For proper turn–on bias sequencing, the V_{G1} first gate voltages should be applied first, followed by the V_{G2} second gate voltages and then the V_{SS} source voltages. For turn–off, the reverse sequence should be followed.

DC ground connections to the chip top–side GND contact pads are NOT required due to the conductive backside ground vias available on the MMIC. Conductive die-attach is required.

The provided "Absolute Maximum" specification limits have been determined such that the safe operating region and recommended maximum channel temperature (150 °C) are not exceeded when the backside of the device is ≤ 75 °C. Operating this device beyond the specified maximum voltage and current limits may result in rapid performance degradation or permanent damage to the device due to electrical overstress.

The chip also includes optional temperature monitoring contact pads for either a diode-based or resistor-based temperature sensing structures.

Assembly Techniques

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly.

MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Agilent application note #54, *GaAs MMIC ESD, Die Attach and Bonding Guidelines* provides basic information on these subjects.

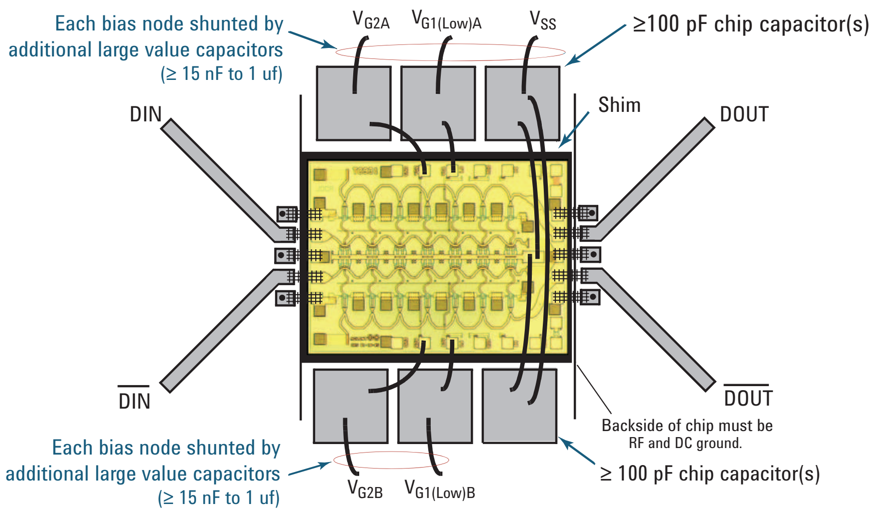

Figure 2. Default assembly and biasing configuration.

Notes

1. All bonds should be as short as possible to limit inductance.
2. Single wire bonds may be substituted for RF mesh bonds provided they are stacked on device pad and extend to corners of TF trace(s).
3. Device may be soldered to Au-Mo Shim using 80/20% Pb/Sn solder or Ablestik 84-1LMI Silver Epoxy (< 12 micron thick) cured for 1 hour @ 150 °C.
4. Shim should be epoxied to large heat-sink or microcircuit housing using 84-1LMI epoxy cured for 1 hour @ 150 °C.
5. All unused RF input or output ports should be DC terminated into 50 Ω.

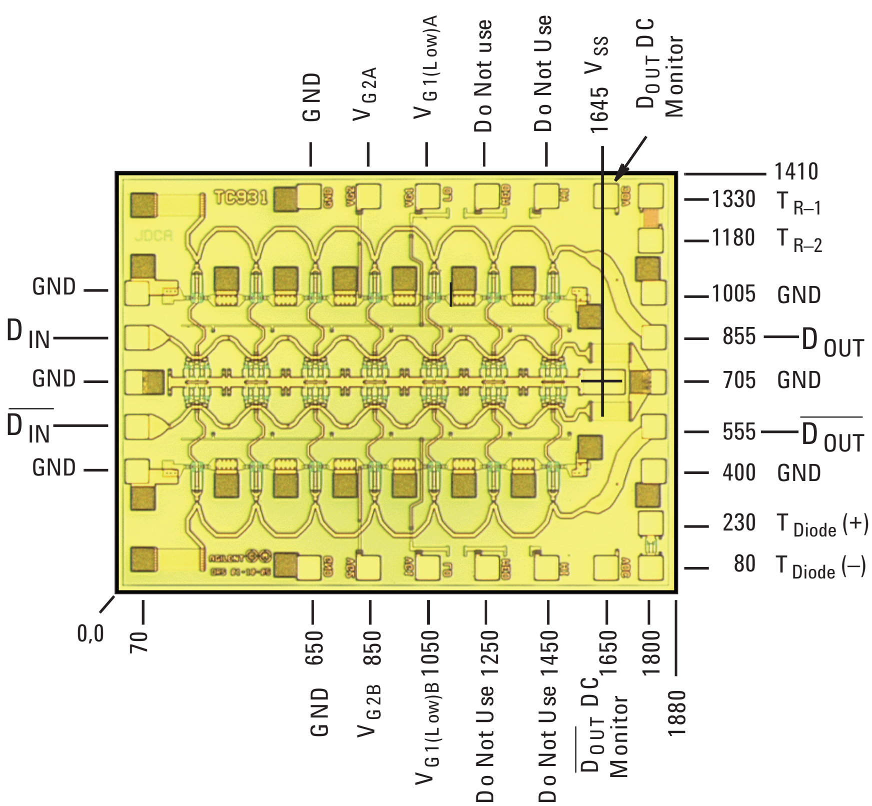

Figure 3. Bonding pad position (dimensions are in micrometers)

Notes

1. T_{R-1} & T_{R-2} are contact pads for the optional on-chip temperature monitoring thermal sensing structure.
2. T_{Diode}(+) & T_{Diode}(–) are contact pads for the anode and cathode, respectively of the optional on-chip temperature monitoring diode structure.

This data sheet contains a variety of *typical* and guaranteed performance data. The information supplied should not be interpreted as a complete list of circuit specifications. In this data sheet the term typical refers to the 50th percentile performance.

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