

Agilent

N4982A Clock Recovery Unit

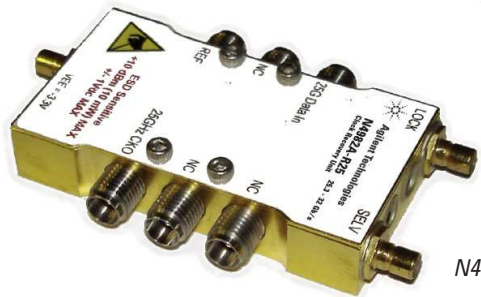
Data Sheet

For 100GE or SONET/
SDH Applications

- Low jitter output clock
- Low power dissipation
- Precision connectors
- Excellent signal quality



N4982A-R19 19 to 26 Gb/s (MC19R26M)



N4982A-R25 25.3 to 32 Gb/s (MC25R32M)



N4982A-R28 27.9 to 36 Gb/s (MC28R36M)



N4982A-R40 39.8 to 44 Gb/s (MC39R46M)



N4982A-R19 Clock Recovery Unit 19 to 26 Gb/s

Features

- 19 to 26 Gb/s data rates
- High input sensitivity
- Low jitter output clock
- Low power consumption
- Single -3.6 V power supply

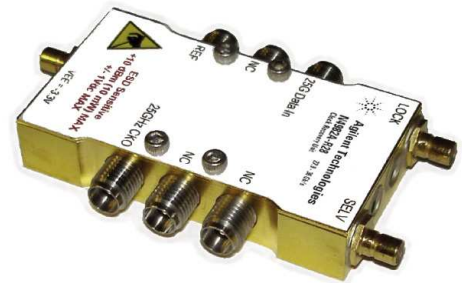


Figure 1. N4982A-R19 clock recovery unit 19 to 26 Gb/s

Description

The N4982A-R19 (MC19R26M) is a clock recovery unit (CRU) using silicon germanium (SiGe) process technology.

The module accepts input data rates at 25.8 Gb/s with an input sensitivity greater than 100 mVppk.

The data input is AC coupled and terminated with a 50 ohm resistor to minimize reflections. The full-rate recovered clock is AC-coupled at ECL compatible levels.

Applications

The N4982A-R19 clock recovery unit 19 to 26 Gb/s (MC19R26M) can be used to extract low jitter clock for 100 GE applications operating at transmission speeds of 25.8 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors and excellent signal quality.

Operating Conditions

Table 1

Parameter	Minimum	Typical	Maximum
Vee	-3.6 V	-3.3 V	-3.1 V

Key specifications at 33 °C

Table 2

Parameter	Minimum	Typical	Maximum	Units
Data input				
Bit rate	19	–	26	Gb/s
Amplitude	100	–	1400	mVpp
Reference clock input				
Frequency	9.5	–	13	GHz
Amplitude	200	–	1400	mVpp
Clock output				
Frequency	19	–	26	GHz
Amplitude	150	–	450	mVpp
Jitter RMS	–	–	0.5	psec
Jitter Pk-Pk	–	–	3	psec

Vee = -3.6 V, Iee = 265 mA, Zo = 50 Ω

N4982A-R19

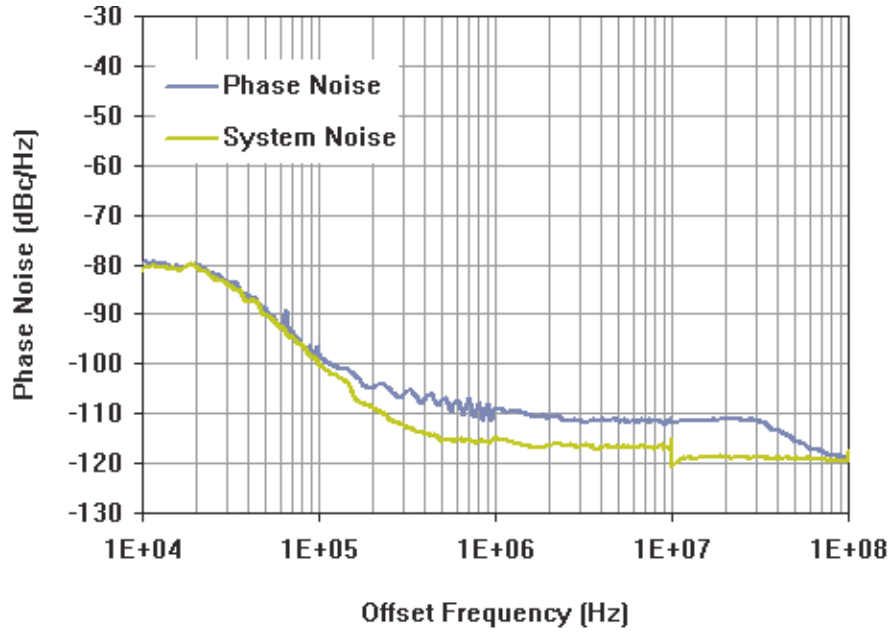


Figure 2. Phase noise of CKO at 25.78125 GHz locked to 2e31, 25.78125 Gb/s data

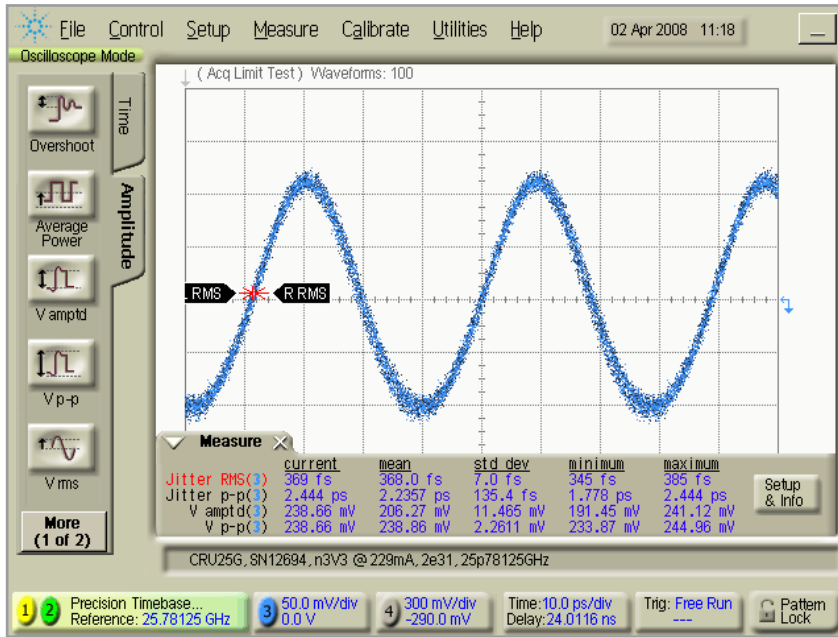
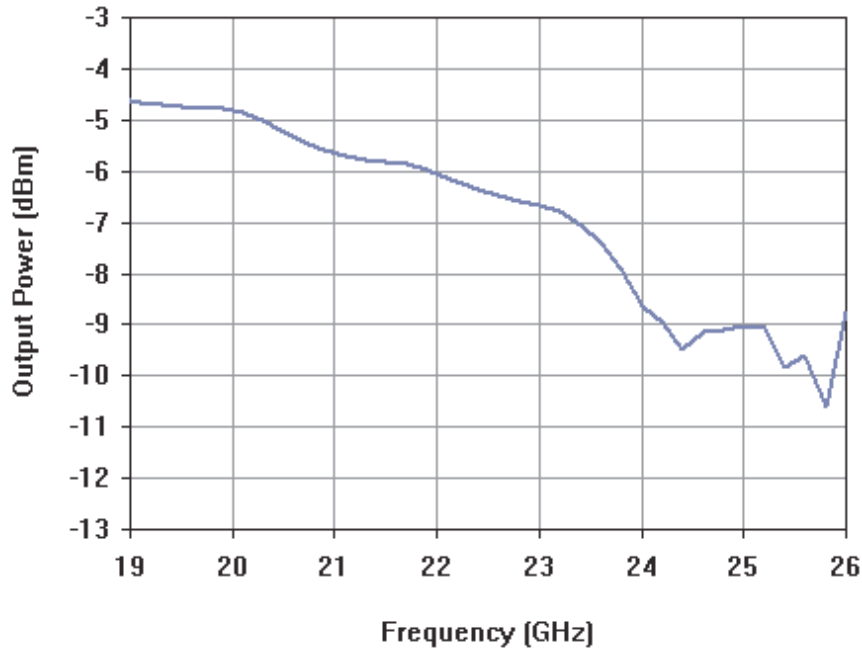


Figure 3. 25.78125 GHz clock output Locked to 2e31, 25.78125 Gb/s data

N4982A-R19



Absolute maximum ratings

Table 3

Parameter	Value
Supply voltage (VEE)	-3.8 V
Ref power (REF)	+10 dBm
DC voltage level (Din,REF,CKO)	±1 V
Operating temperature	0 to 70 °C
Storage temperature	-85 to 125 °C

Figure 4. Output power vs frequency

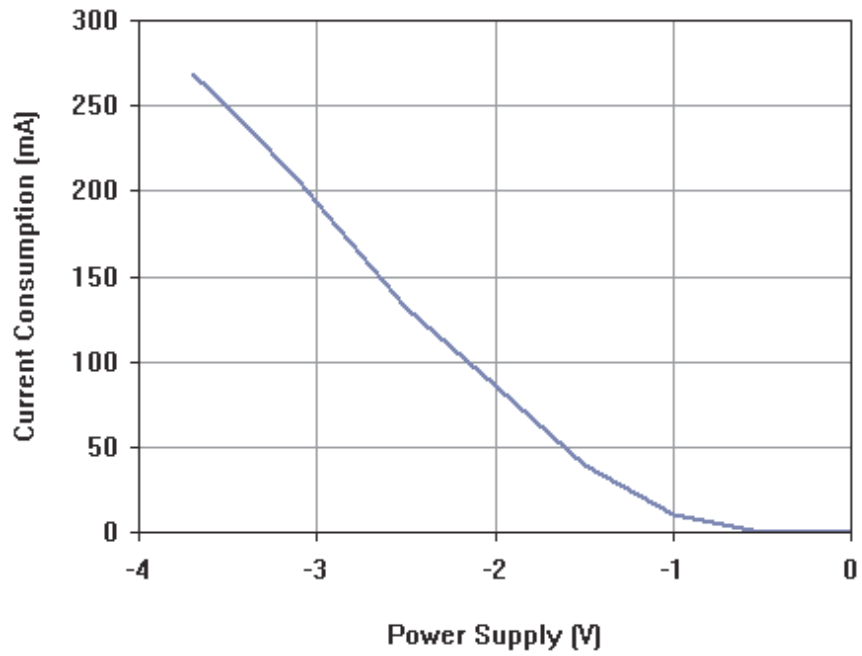


Figure 5. Total current consumption vs power supply level

N4982A-R19 functional block diagram

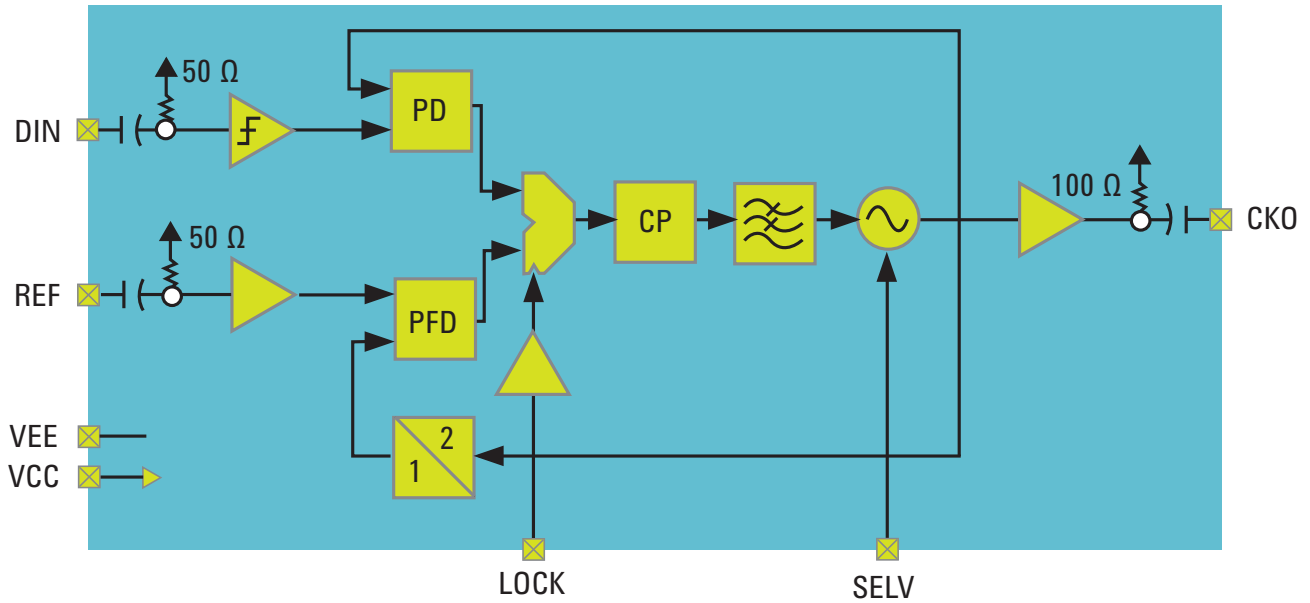


Figure 6. Functional block diagram

Pin description (see Figure 7 below)

Table 4

Name	Pin	Description	Note	Connector
LOCK	1	Reference input selector	Internal PLL reference selector between input data and reference clock	SMB
SELV	2	Frequency range selector	Selects between two VCOs for lower/upper band	SMB
CKO	5	Full-rate clock output	Single ended output	2.9 mm(K)
VEE	6	Negative supply voltage	Center pin -3.6 V, shield/case is ground	SMB
REF	7	Reference clock input	AC coupled input	2.9 mm(K)
DIN	9	Data input	Single ended input	2.9 mm(K)
NC	3, 4, 8	No connect		

LOCK logic

Table 5

Parameters	State	Min	Typ	Max
Low (default)	Reference clock	–	-3.3 V	–
High	Data	–	0 V	–

SELV logic

Table 6

Parameters	State	Min	Typ	Max
Low (default)	19 to 22.2 Gb/s	–	-3.3 V	–
High	22.2 to 26.0 Gb/s	–	0 V	–

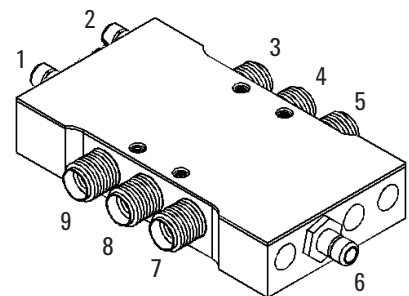


Figure 7. Module outline

N4982A-R19 application note

Clock recovery

The N4982A-R19 clock recovery unit 19 to 26 Gb/s (MC19R26M) has two loops with two separate inputs—one for training the loop to the right frequency, and the other for phase locking the loop to the actual data. Refer to data sheet for block diagram. The part requires a $\frac{1}{2}$ rate clock for training the CRU. Once the loop is trained, the input should be switched over to the data input by setting the LOCK pin (pin 1) High (or 0V).

Clock recovery procedure

1. Connect both data and reference inputs to the device. The reference clock should be $\frac{1}{2}$ of the data rate. For example, if data rate is 25 Gbps, then reference clock is 12.5 GHz (sine or square). Make sure that the LOCK pin (pin 1) is set to Low, or -3.3 V, or left open (it defaults to logic state Low).
2. Monitor the output frequency to see if the loop has locked to the desired frequency, which should be full-rate. For this example, the loop is locked if CKO is 25 GHz.
3. Once the loop is locked (i.e. trained), switch the LOCK pin to High, or 0 V, to lock onto the data input.

The N4982A-R19 (MC19R26M) may also be trained using $\frac{1}{4}$ or $\frac{1}{8}$ of the data rate as the reference clock input; however, the VCO capture range will be reduced.

Packaging information

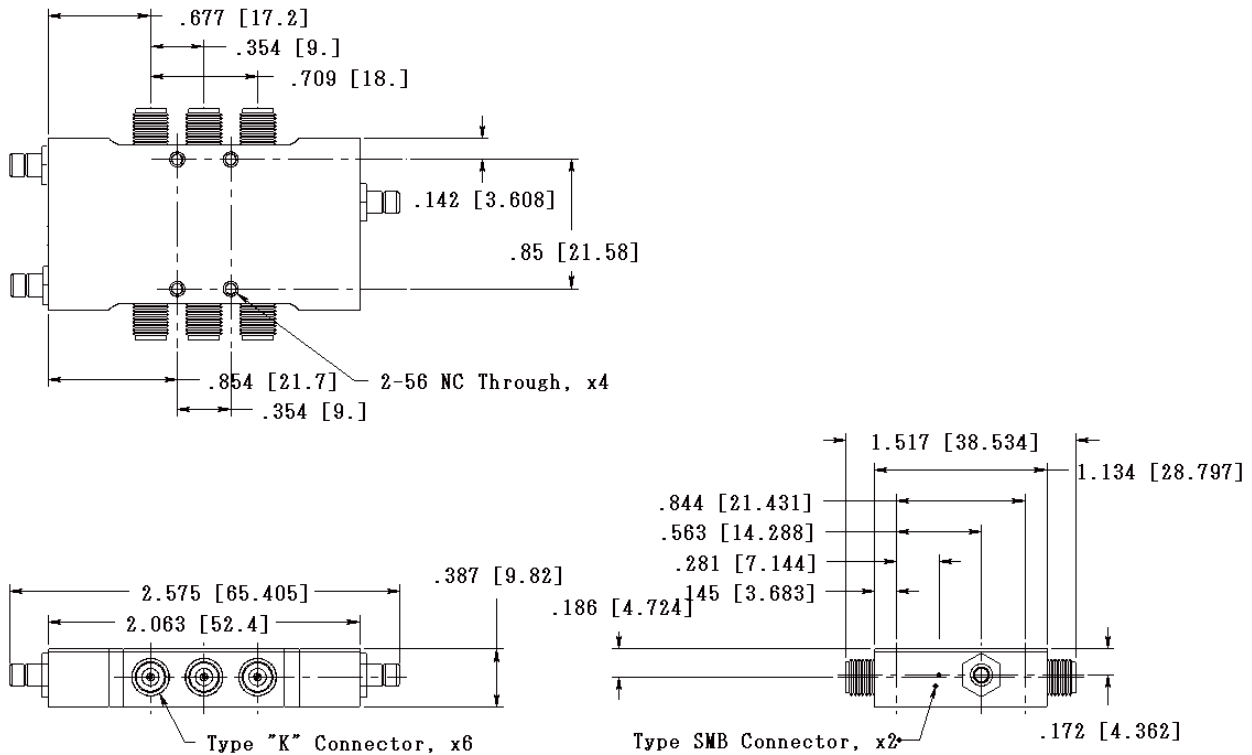


Figure 8. All measurements in inches (mm)

N4982A-R25 Clock Recovery Unit 25.3 to 32 Gb/s

Features

- 25.3 to 32.0 Gb/s data rates
- High input sensitivity
- Low jitter output clock
- Low power consumption
- Single -3.3 V power supply



Figure 9. N4982A-R25 clock recovery unit 25.3 to 32 Gb/s

Description

The N4982A-R25 (MC25R32M) is a clock recovery unit (CRU) using silicon germanium (SiGe) process technology. The module accepts input data rates from 25.3 to 32.0 Gb/s with an input sensitivity better than 50 mVppk. The data input is AC coupled and terminated with a 50 ohm resistor to minimize reflections. The half-rate recovered clock is AC-coupled at ECL compatible levels.

Applications

The N4982A-R25 clock recovery unit 25.3 to 32 Gb/s (MC25R32M) can be used to extract low jitter clock for 100GE applications with and without FEC operating at transmission speeds of 25.78125, 27.95, and 30.9375 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors and excellent signal quality.

Operating conditions

Table 7

Parameter	Minimum	Typical	Maximum
Vee	-3.6 V	-3.3 V	-3.0 V

Key specifications at 25 °C

Table 8

Parameter	Minimum	Typical	Maximum
Data input			
Bit rate	25.3 Gb/s	–	32.0 Gb/s
Amplitude	50 mVpp	–	1400 mVpp
Reference clock input			
Frequency	6.325 Gb/s	–	8.0 Gb/s
Amplitude	50 mVpp	–	1400 mVpp
Clock output			
Frequency	12.65 Gb/s	–	16.0 Gb/s
Amplitude	300 mVpp	–	600 mVpp
Jitter RMS	–	0.5 psec	0.6 psec
Jitter Pk-Pk	–	3 psec	6 psec

Vee = -3.3 V, Iee = 220 mA, Zo = 50 Ω

N4982A-R25

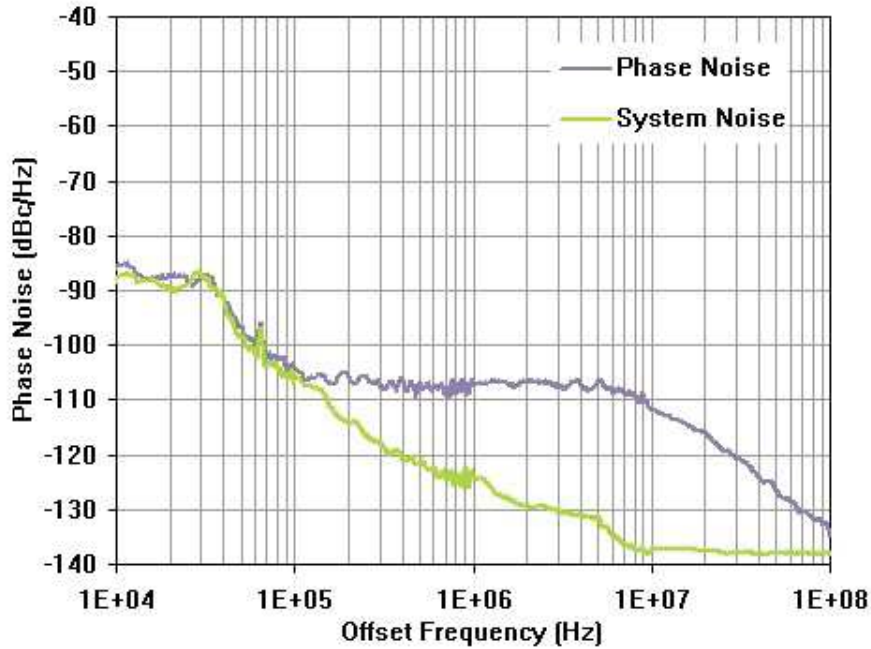


Figure 10. Phase noise of CKO at 13.975 GHz Locked to 2 e15, 27.95 Gb/s data

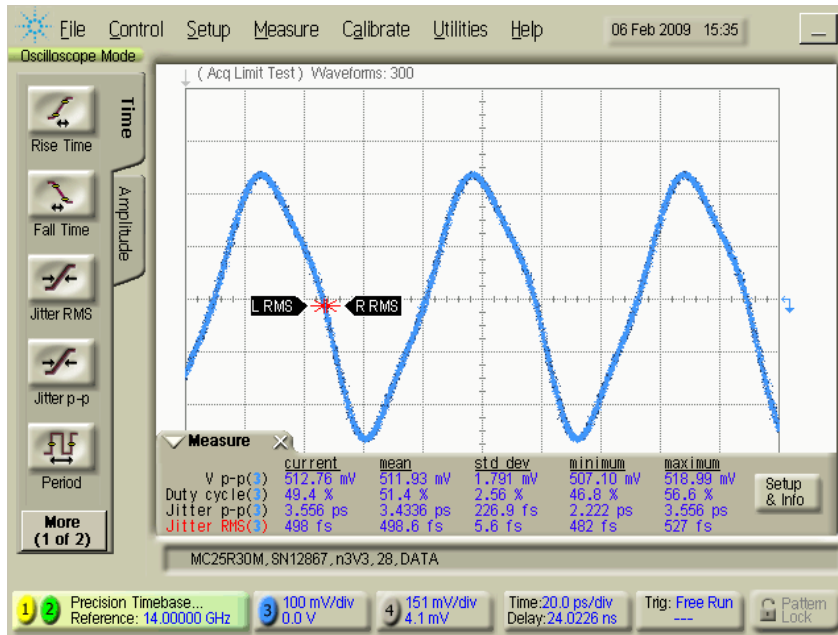


Figure 11. 13.975 GHz clock output Locked to 2 e15, 27.95 Gb/s data

N4982A-R25

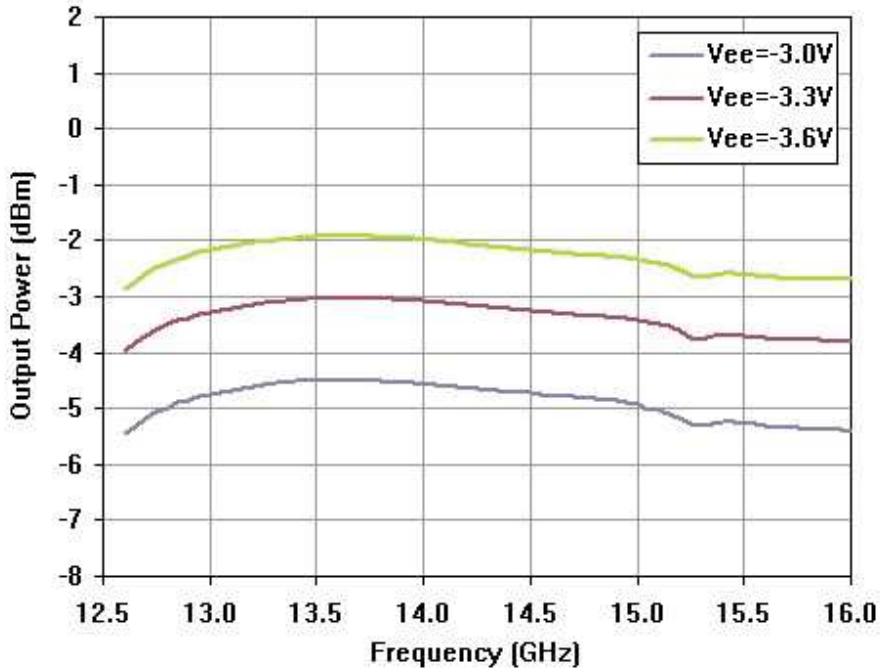


Figure 12. Output oower vs frequency

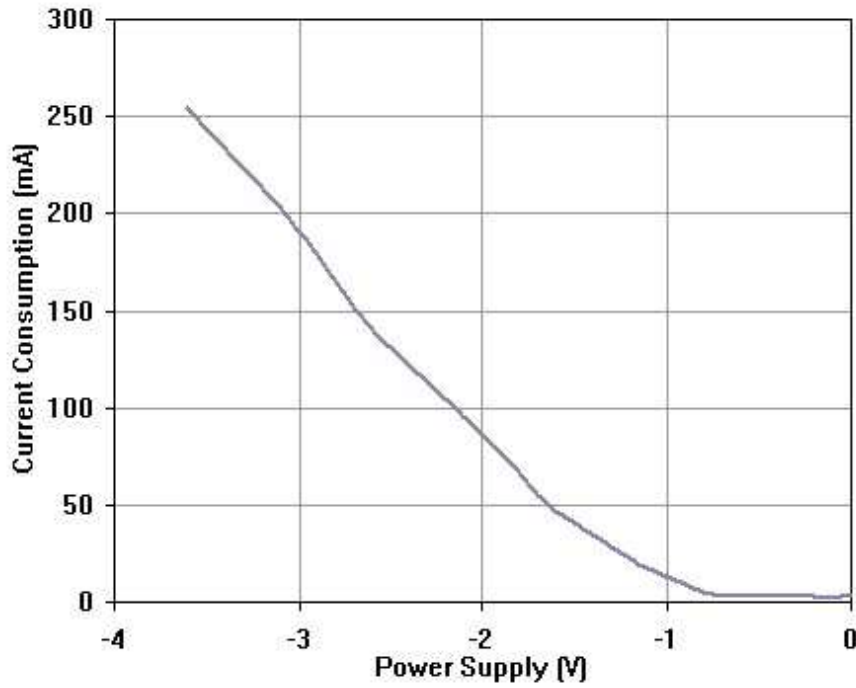


Figure 13. Total current consumption vs power supply level

Absolute maximum ratings

Table 9

Parameter	Value
Supply voltage (VEE)	-3.8 V
Ref power (REF)	+10 dBm
DC voltage level (Din,REF,CKO)	±1 V
Operating temperature	0 to 70 °C
Storage temperature	-85 to 125 °C

N4982A-R25 functional block diagram

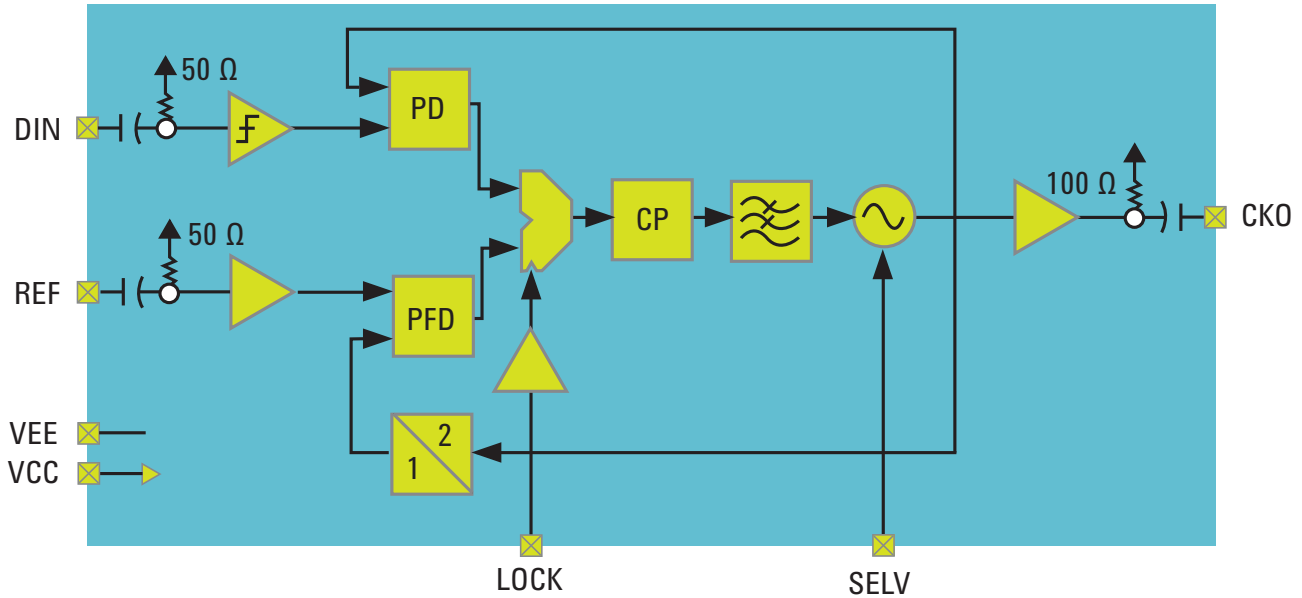


Figure 14. Functional block diagram

Pin description (refer to Figure 15, below)

Table 10

Name	Pin	Description	Note	Connector
LOCK	1	Reference input selector	Internal PLL reference selector between input data and reference clock	SMB
SELV	2	Frequency range selector	Selects between two VCOs for lower/upper band	SMB
CKO	5	Half-rate clock output	Single ended output	2.9 mm(K)
VEE	6	Negative supply voltage	Center pin -3.3 V, shield/case is ground	SMB
REF	7	Reference clock input	Positive differential input	2.9 mm(K)
DIN	9	Data input	Single ended input	2.9 mm(K)
NC	3, 4, 8	No connect		

LOCK logic

Table 11

Parameters	State	Min	Typ	Max
Low (default)	Reference clock	–	-3.3 V	–
High	Data	–	0 V	–

SELV logic

Table 12

Parameters	State	Min	Typ	Max
Low (default)	27.5 to 32.0 Gb/s	–	-3.3 V	–
High	25.3 to 30.0 Gb/s	–	0 V	–

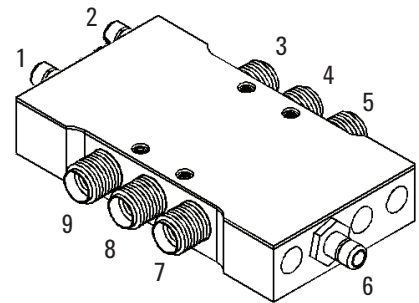


Figure 15. Outline

N4982A-R25 application note

Clock recovery

The N4982A-R25 clock recovery unit 25.3 to 32 Gb/s (MC25R32M) has two loops with two separate inputs—one for training the loop to the right frequency, and the other for phase locking the loop to the actual data. Refer to page 3 for block diagram. The part requires a $\frac{1}{4}$ rate clock for training the CRU. Once the loop is trained, the input should be switched over to the data input by setting the LOCK pin (pin 1) High (or 0 V).

Clock recovery procedure

1. Connect both data and reference inputs to the device. The reference clock should be $\frac{1}{4}$ of the data rate. For example, if data rate is 27.95 Gbps, then reference clock is 6.9875 GHz (sine or square). Make sure that the LOCK pin (pin 1) is set to Low, or -3.3 V, or left open (it defaults to logic state Low).
2. Monitor the output frequency to see if the loop has locked to the desired frequency, which should be half-rate. For this example, the loop is locked if CKO is 13.975 GHz.
3. Once the loop is locked (i.e. trained), switch the LOCK pin to High, or 0 V, to lock onto the data input.

The N4982A-R25 (MC25R32M) may also be trained using $\frac{1}{8}$ or $\frac{1}{16}$ of the data rate as the reference clock input; however, the VCO capture range will be reduced.

Packaging information

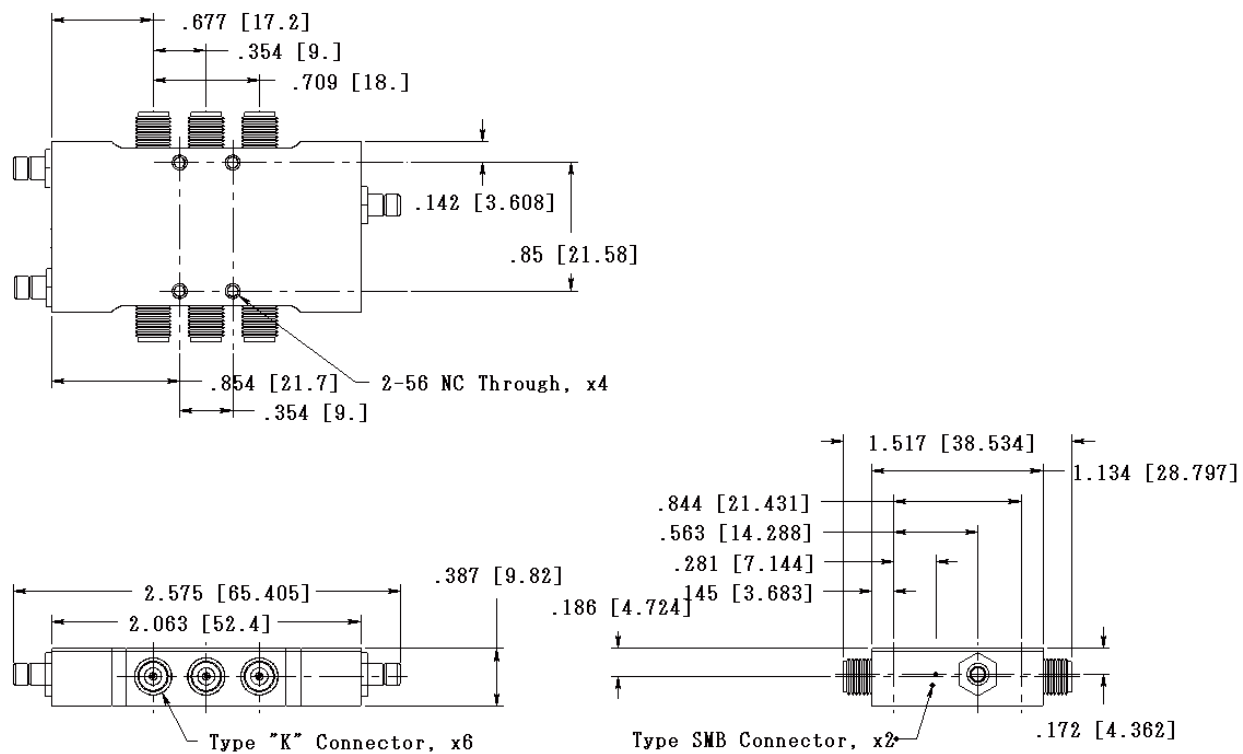


Figure 16. All measurements in inches (mm)

N4982A-R28 Clock Recovery Unit 27.9 to 36 Gb/s

Features

- 27.9 to 36.0 Gb/s data rates
- High input sensitivity
- Low jitter output clock
- Low power consumption
- Single -3.3 V power supply

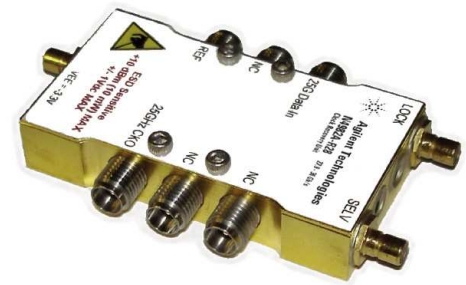


Figure 17. N4982A-R28 Clock Recovery Unit 27.9 to 36 Gb/s

Description

The N4982A-R28 clock recovery unit 27.9 to 36 Gb/s (MC28R36M) is a clock recovery unit (CRU) using silicon germanium (SiGe) process technology. The module accepts input data rates at 27.95 Gb/s with an input sensitivity greater than 50 mVppk. The data input is AC coupled and terminated with a 50 ohm resistor to minimize reflections. The half-rate recovered clock is AC-coupled at ECL compatible levels.

Applications

The N4982A-R28 clock recovery unit 27.9 to 36 Gb/s (MC28R36M) can be used to extract low jitter clock for 100 GE applications operating at transmission speeds of 27.95 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors and excellent signal quality. The N4982A-R28 clock recovery unit 27.9 to 36 Gb/s (MC28R36M) also locks to half-rate data to cover 16 Gb/s Fibre Channel (16 GFC).

Operating conditions

Table 13

Parameter	Minimum	Typical	Maximum
Vee	-3.6 V	-3.3 V	-3.0 V

Key specifications at 25 °C

Table 14

Parameter	Minimum	Typical	Maximum
Data input			
Bit rate	27.9 Gb/s	–	36.0 Gb/s
Amplitude	50 mVpp	–	1400 mVpp
Reference clock input			
Frequency	6.975 Gb/s	–	9.0 Gb/s
Amplitude	50 mVpp	–	1400 mVpp
Clock output			
Frequency	13.95 Gb/s	–	1980 Gb/s
Amplitude	300 mVpp	–	600 mVpp
Jitter RMS	–	0.4 psec	0.6 psec

Vee = -3.3 V, Iee = 220 mA, Zo = 50 Ω

N4982A-R28

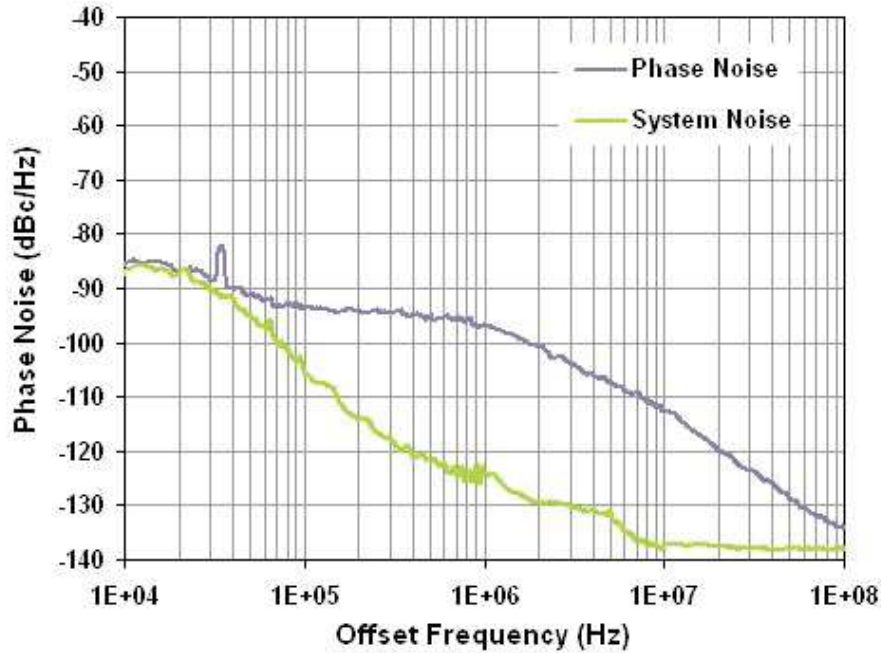


Figure 18. Phase noise of CKO at 14.0 GHz Locked to 2e15, 28.0 Gb/s data

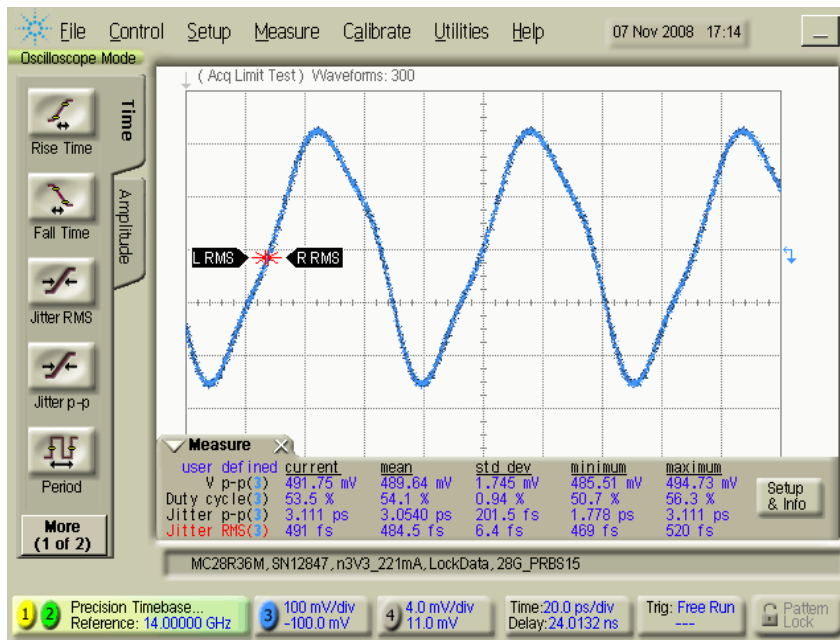


Figure 19. 14.0 GHz clock output Locked to 2e15, 28.0 Gb/s data

N4982A-R28

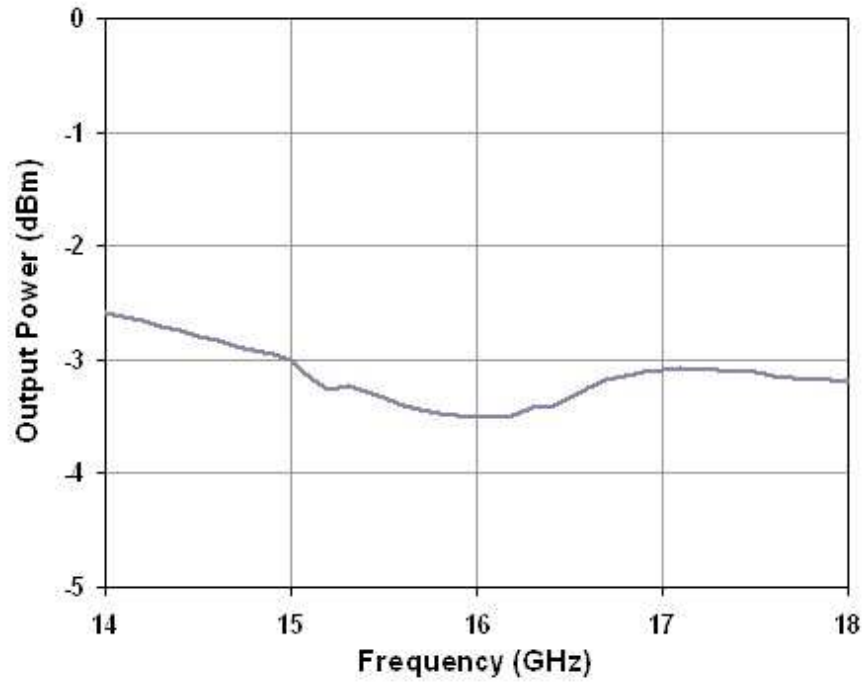


Figure 20. Output power vs frequency

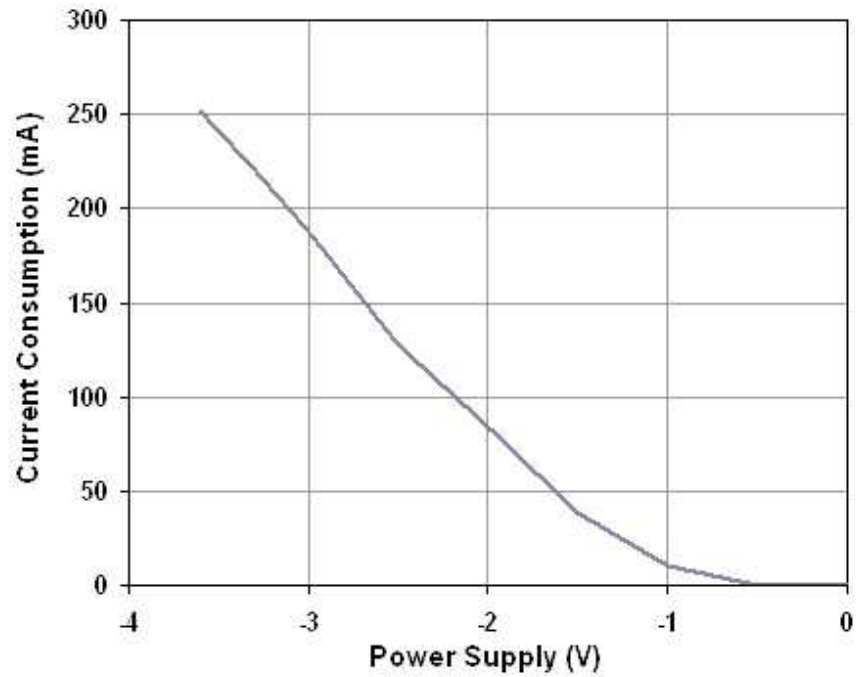


Figure 21. Total current consumption vs power supply level

Absolute maximum ratings

Table 15

Parameter	Value
Supply voltage (VEE)	-3.8 V
Ref power (REF)	+10 dBm
DC voltage level (Din,REF,CKO)	±1 V
Operating temperature	0 to 70 °C
Storage temperature	-85 to 125 °C

N4982A-R28 functional block diagram

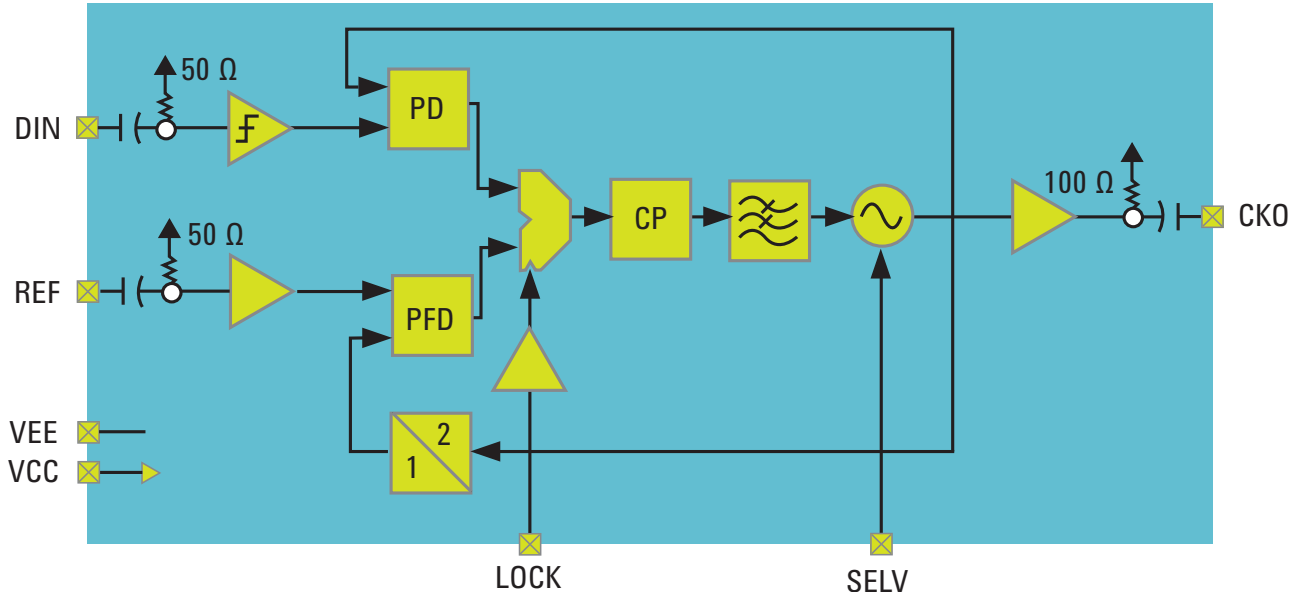


Figure 22. Functional block diagram

Pin description (refer to Figure 23 below)

Table 16

Name	Pin	Description	Note	Connector
LOCK	1	Reference input selector	Internal PLL reference selector between input data and reference clock	SMB
SELV	2	Frequency range selector	Selects between two VCOs for lower/upper band	SMB
CKO	5	Half-rate clock output	Single ended output	2.9 mm(K)
VEE	6	Negative supply voltage	Center pin -3.3 V, shield/case is ground	SMB
REF	7	Reference clock input	Positive differential input	2.9 mm(K)
DIN	9	Data input	Single ended input	2.9 mm(K)
NC	3, 4, 8	No connect		

LOCK logic

Table 17

Parameters	State	Min	Typ	Max
Low (default)	Reference clock	–	-3.3 V	–
High	Data	–	0 V	–

SELV logic

Table 18

Parameters	State	Min	Typ	Max
Low (default)	27.5 to 32.0 Gb/s	–	-3.3 V	–
High	25.3 to 30.0 Gb/s	–	0 V	–

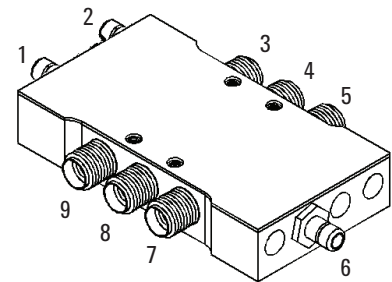


Figure 23. Outline

N4982A-R28 application note

Clock recovery

The N4982A-R28 clock recovery unit 27.9 to 36 Gb/s (MC28R36M) has two loops with two separate inputs—one for training the loop to the right frequency, and the other for phase locking the loop to the actual data. Refer to page 3 for block diagram. The part requires a $\frac{1}{4}$ rate clock for training the CRU. Once the loop is trained, the input should be switched over to the data input by setting the LOCK pin (pin 1) High (or 0 V).

Clock recovery procedure

1. Connect both data and reference inputs to the device. The reference clock should be $\frac{1}{4}$ of the data rate. For example, if data rate is 27.95 Gbp/s, then reference clock is 6.9875 GHz (sine or square). Make sure that the LOCK pin (pin 1) is set to Low, or -3.3 V, or left open (it defaults to logic state Low).
2. Monitor the output frequency to see if the loop has locked to the desired frequency, which should be half-rate. For this example, the loop is locked if CKO is 13.975 GHz.
3. Once the loop is locked (i.e. trained), switch the LOCK pin to High, or 0 V, to lock onto the data input.

The N4982A-R28 (MC28R36M) may also be trained using $\frac{1}{8}$ or $\frac{1}{16}$ of the data rate as the reference clock input; however, the VCO capture range will be reduced.

Packaging information

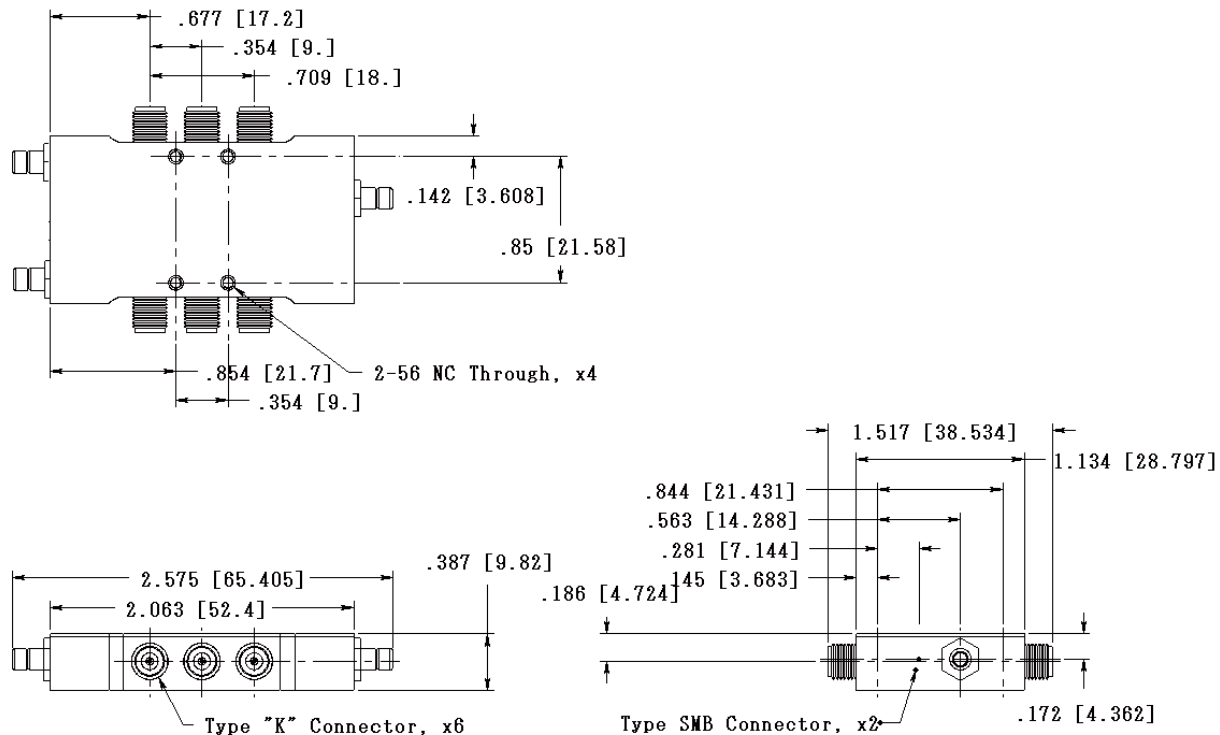


Figure 24. All measurements in inches (mm)

N4982A-R40 Clock Recovery Unit 39.8 to 44 Gb/s

Features

- 39.8 to 44 Gb/s data rates
- High input sensitivity
- Low jitter output clocks
10 and 20 GHz
- Low power consumption
- Single -3.3 V power supply



Figure 25. N4982A-R40 Clock Recovery Unit 39.8 to 44 Gb/s

Description

The N4982A-R40 clock recovery unit 39.8 to 44 Gb/s (MC39R46M) can be used to extract low jitter clock for SONET and SDH applications operating at transmission speeds of 40 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors and excellent signal quality.

Applications

The N4982A-R40 clock recovery unit 39.8 to 44 Gb/s (MC39R46M) is a clock recovery unit (CRU) using silicon germanium (SiGe) process technology. The module accepts input data rates at 40 Gb/s with an input sensitivity greater than 100 mVppk. The data input is AC coupled and terminated with a 50 ohm resistor to minimize reflections. Recovered clocks at 10 and 20 GHz are output via AC coupled outputs with ECL compatible signal levels.

Operating Conditions

Table 19

Parameter	Minimum	Typical	Maximum
Vee	–	-3.3 V	–

Key specifications at 33 °C

Table 20

Parameter	Description	Minimum	Typical	Maximum
Din (Gb/s)	Input data rate	39.8	–	44
Vin (mVppk)	Data input level	100	–	400
V20 G(mVppk)	20 GHz output voltage swing	100	200	–
V10 G(mVppk)	10 GHz output voltage swing	150	300	–
S11 (dB)	Data input return loss	–	-15	-10
S22 (dB)	20 GHz clock output return loss	–	-10	-7
S33 (dB)	10 GHz clock output return loss	–	-10	-7
S44 (dB)	Reference clock return loss	-10	0	$+10$

Vee = -3.3 V, Iee = 220 mA, Zo = 50 Ω

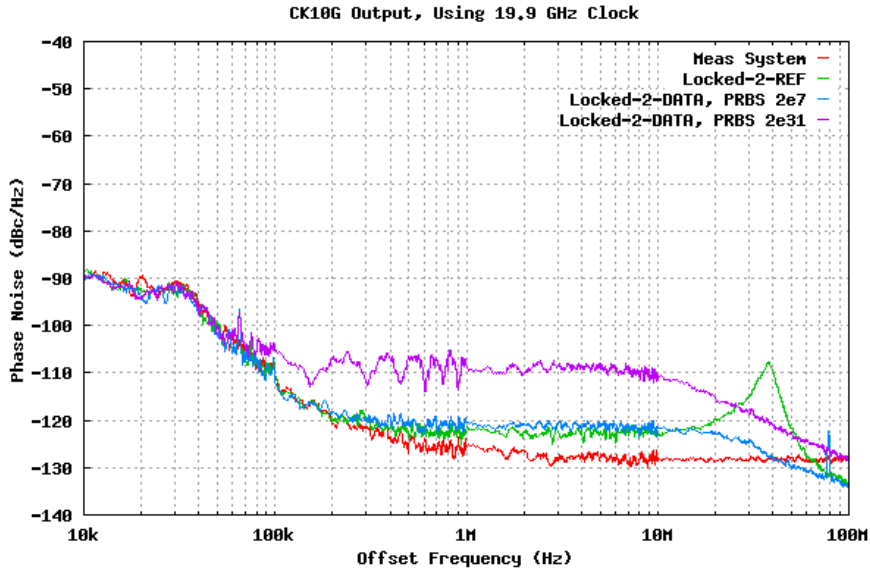


Figure 26. Phase noise of CKO10G Carrier frequency = 19.9 GHz

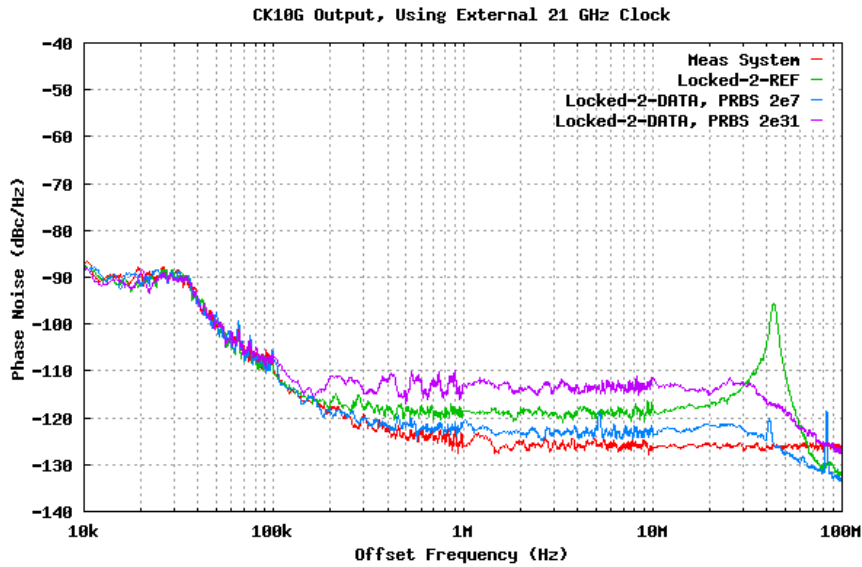


Figure 27. Phase noise of CKO10G Carrier frequency = 21 GHz

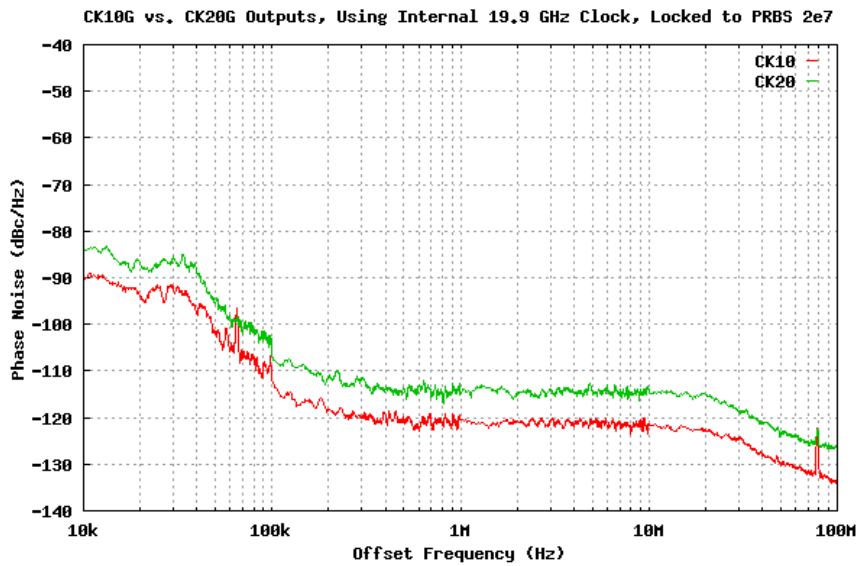


Figure 28. Phase noise of CKO10G and CKO20G Locked to 2e7, 39.8 Gb/s data

Table 21

Parameter	Value
Supply voltage (V _{EE})	-4.0 V
Ref power (REF, REFN)	+10 dBm
DC voltage level (Din,REF,REFN,CK10 G,CK20 G)	±1 V
Operating temperature	-40 to 80 °C
Storage temperature	-85 to 150 °C

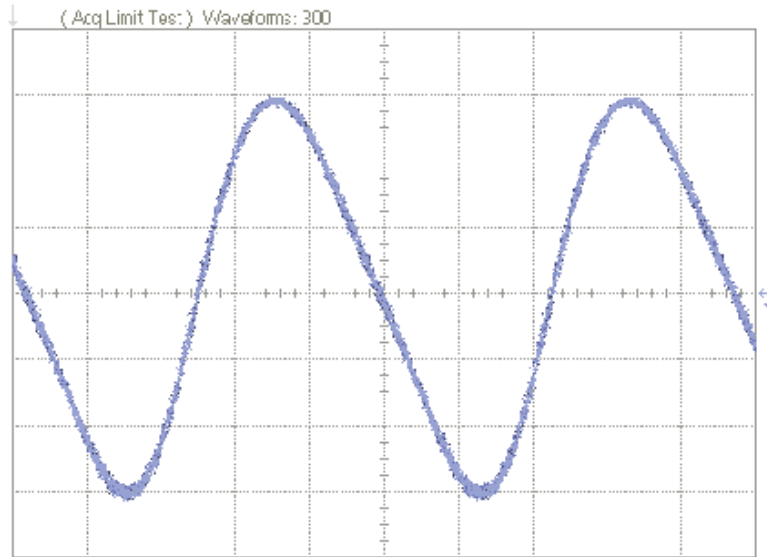


Figure 29. 21 GHz clock output Locked to 2.625 GHz reference; 50 mV/DIV, 10pS/DIV

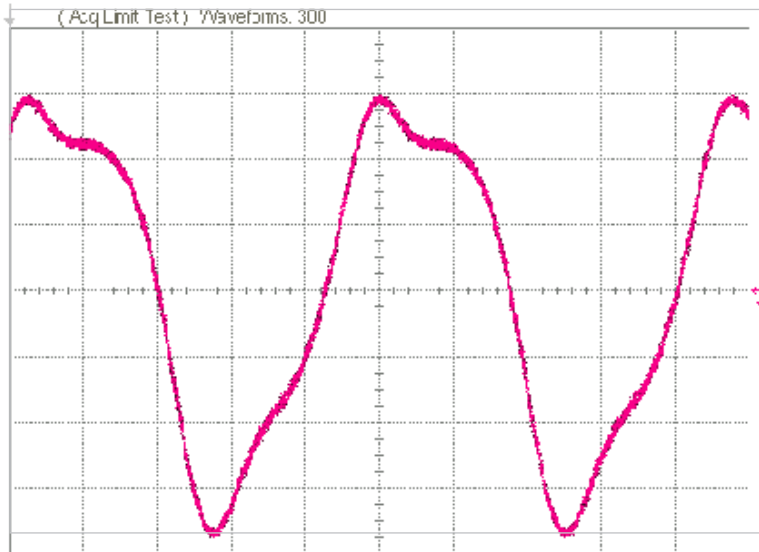


Figure 30. 10.5 GHz clock output Locked to 2.625 GHz reference; 50 mV/DIV, 20pS/DIV

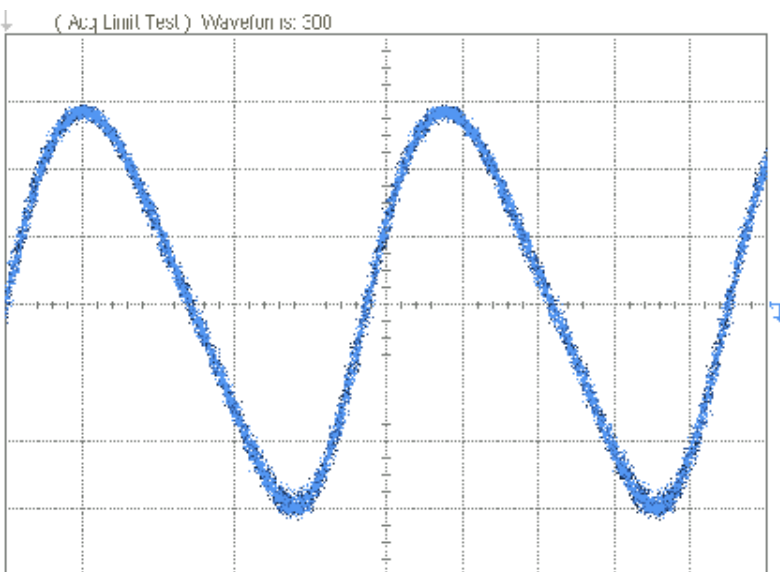


Figure 31. 21.0 GHz clock output Locked to 2e31, 42 Gb/s data; 50 mV/DIV, 10pS,DIV

N4982A-R40 functional block diagram

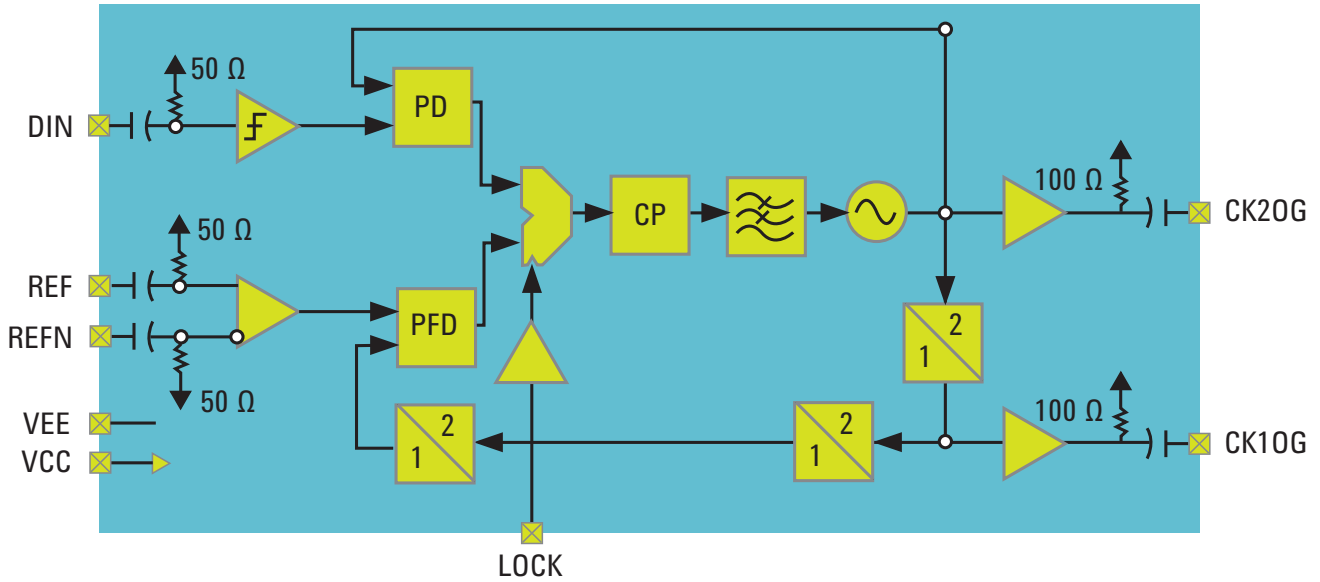


Figure 32. Functional block diagram

Pin description (refer to Figure 33 below)

Table 22

Name	Pin	Description	Note	Connector
LOCK	1	Reference input selector	Internal PLL reference selector between input data and reference clock	SMB
REF	2	Reference clock input	Positive differential input	2.9 mm(K)
REFN	3	Reference clock input	Negative differential input	2.9 mm(K)
CK10 G	4	10 GHz clock output*	Single ended input	2.9 mm(K)
VEE	5	Negative supply voltage	Center pin -3.3 V, shield/case is ground	SMB
CK20 G	6	20 GHz clock output**	Single ended input	2.9 mm(K)
NC	7	No connect		
DIN	8	Data input	Single ended input	2.9 mm(K)

*CK20 G/2 output

**Half of data rate (i.e. 40 Gbp/s data rate 20 GHz clock speed)

LOCK logic

Table 23

Parameters	State	Min	Typ	Max
Low	Data	-	-3.3 V	-
High (default)	Reference clock	-	0 V	-

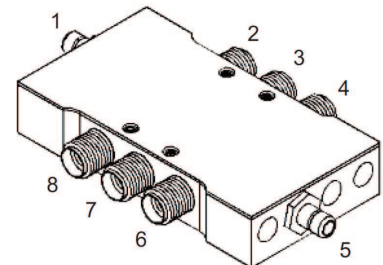


Figure 33. Outline

N4982A-R40 application note

Clock recovery

The N4982A-R40 clock recovery unit 39.8 to 44 Gb/s (MC39R46M has two loops with two separate inputs—one for training the loop to the right frequency, and the other for phase locking the loop to the actual data. Refer to data sheet for block diagram. The part requires a 1/16 rate clock for training the CRU. Once the loop is trained, the input should be switched over to the data input by setting the LOCK pin (pin 1) Low (or -3.3 V).

Clock recovery procedure

1. Connect both data and reference inputs to the device. The reference clock should be 1/16 of the data rate. For example, if data rate is 40 Gbp/s, then reference clock is 2.5 GHz (sine or square). Make sure that the LOCK pin (pin 1) is set to High, or 0 V, or left open (it defaults to logic state High).
2. Monitor one of the output frequencies to see if the loop has locked to the desired frequency, which should be either $\frac{1}{2}$ rate or $\frac{1}{4}$ rate, depending on which output you are monitoring. For this example, $\frac{1}{2}$ rate is 21.5 GHz, and $\frac{1}{4}$ rate is 10.75 GHz.
3. Once the loop is locked (i.e. trained), switch the LOCK pin to Low, or -3.3 V, to lock onto the data input.

* The N4982A-R40 (MC39R46M) may also be trained using 1/32 to 1/64 of the data rate as the reference clock input; however, the characteristic of the VCO capture range will be reduced.

Packaging information

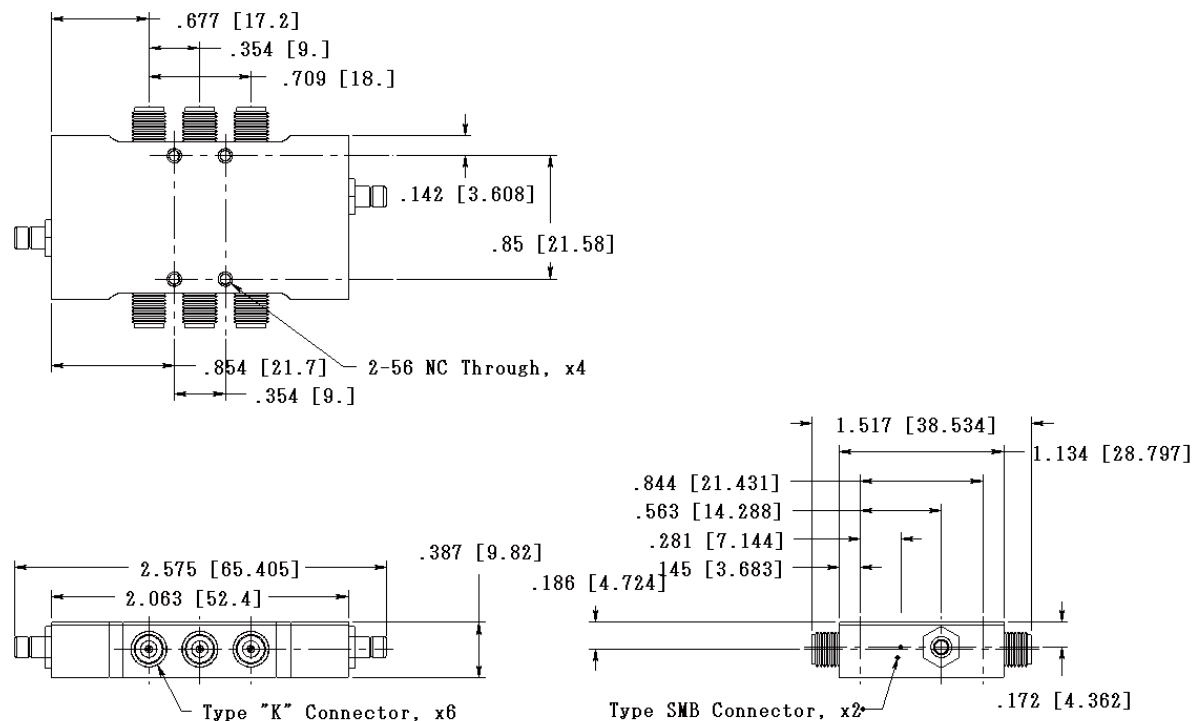


Figure 34. All measurements in inches (mm)



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