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N4967A Serial BERT System 40 Gb/s

40G BER test system (SB40B)

Data Sheet

Complete cost effective solution for 40, 28, and 25 Gb/s device characterization and production testing

Key features

- Operates at data rates from 22 to 44 Gb/s
- True PRBS pattern generation at full data rate
- Supports differential or single ended inputs and outputs
- High voltage drivers available for laser modulator testing
- Remote control through USB or GPIB
- Automatic receiver clock phase alignment
- High speed clock option for continuous operation from 22 to 44 Gb/s
- Compact size

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Modular system architecture

The N4967A serial BERT system 40 Gb/s (SB40B) is formed from three main components:

- **N4974A PRBS Generator 40 Gb/s**
  Provides a true PRBS pattern at full data rate to stimulate the device under test.
- **N4968A 40 Gb/s clock and data demultiplexer 44 Gb/s**
  De-multiplexes the full rate output data stream from the device under test into 4x 10 Gb/s sub-rate data streams. Also divides the high speed clock to provide 10 GHz clock output.
- **N4965A 12.5 Gb/s multi-channel BERT 12.5 Gb/s**
  Measures the bit error rate of the 4x 10 Gb/s de-multiplexed data streams and provides clock control for the 40 Gb/s clock / data demultiplexer.

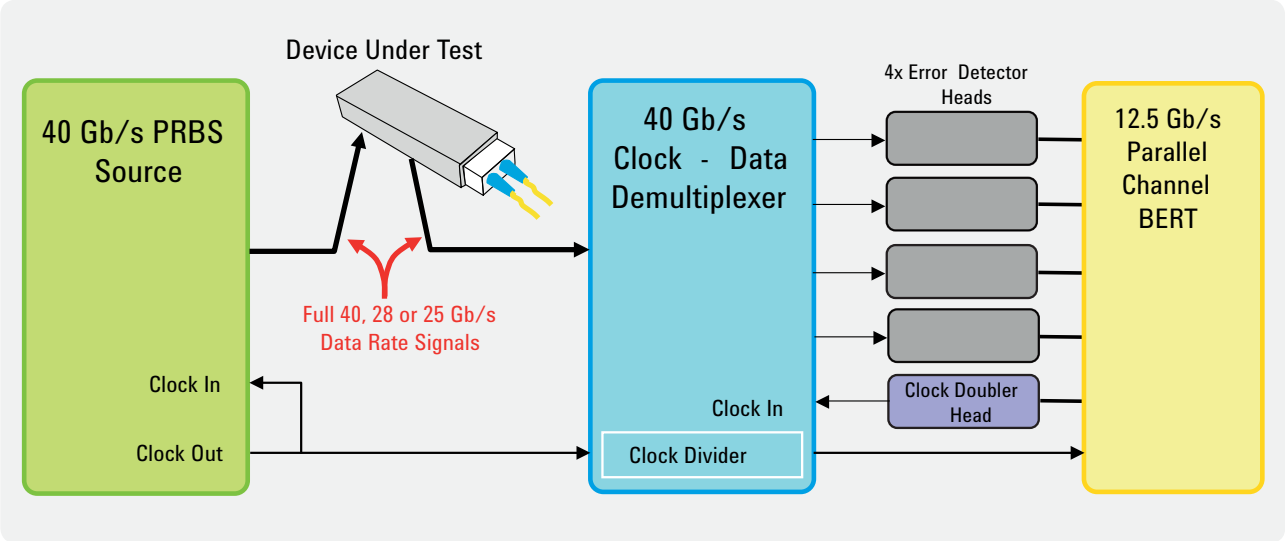

Figure 1. Typical test setup

System configuration

The **N4974A PRBS generator 40 Gb/s (TG1P4A)** source can produce PRBS 7, 15, or 31 patterns, providing flexible trade-off between test duration and pattern dependent stress level. An internal low jitter clock source provides operation at 39.8 Gb/s. Ordering options are available to substitute clock frequencies to support 28 and 25.78125 Gb/s operation. Alternatively the generator can be clocked from an external source for operation at any rate between 22 and 44 Gb/s (half-rate clock required).

Data outputs are differential, and can be used in single-ended applications by terminating the unused output with a 50 ohm load. The PRBS source also provides pattern trigger and clock outputs, which can be used to trigger a sampling oscilloscope to view the bit stream or a classic eye diagram.

Figure 2. N4974A

Figure 3. N4968A

The **N4965A multi-channel BERT 12.5 Gb/s (PCB12500)** with 4x **N4956A-E12 12.5 Gb/s error detector remote heads (TR2P1A)** monitors the demultiplexer data outputs bit error ratio. The **N4957A-C12 clock doubler remote head (TG3C1A)** facilitates electronic phase adjust of the N4968A clock and data demultiplexer 44 Gb/s (TR1D4A) clock input for optimizing clock-data phase for the N4968A clock and data demultiplexer 44 Gb/s (TR1D4A).

The N4965A multi-channel BERT 12.5 Gb/s (PCB12500) can be controlled manually through the front panel, or remotely through IEEE-488 (GPIB) or USB.

The **N4968A clock and data demultiplexer 44 Gb/s (TR1D4A)** can accept differential or single ended input signals, and has 4x data outputs at ¼ of the bit rate. Also included in the N4968A clock and data demultiplexer 44 Gb/s (TR1D4A) are separate clock dividers which can be used to provide the correct divided-clock rate for the BERTs measuring the data outputs.

Electronic control of the high speed clock phase shifter allows for automatic clock-data timing of the N4968A clock and data demultiplexer 44 Gb/s (TR1D4A) clock and data inputs.

Figure 4. N4965A

System automation

In both production testing as well as engineering characterization, automation of the system for instrument control and results data collection are essential.

Tools are provided with the N4967A serial BERT system 40 Gb/s (SB40B) system to simplify the setup and integration into an automated test system.

The N4980A multi-instrument BERT software provides a complete user control interface for performing multi-channel BER testing for the N4967A serial BERT system 40 Gb/s (SB40B). The application computes the BER at the full 40 Gb/s data rate.

Bar graphs display the computed BER of the full rate data stream, as well as BER on each de-multiplexed data output - giving a quick visual indication of any sub rate related bit errors.

Figure 5. N4980A multi-instrument BERT software

Specifications

The following tables list specifications of the individual instruments relevant to application in the 40G BERT system. For complete specifications relevant to other applications, refer to the individual product data sheets.

N4974A PRBS generator 40 Gb/s (TG1P4A)		
Data output signal configuration		Differential. Will operate in single ended mode with unused output terminated
Data line coding		Non-return to zero (NRZ)
Data patterns		2^N–1 PRBS patterns (N=7, 15, 31)
Data rate range		22 to 44 Gb/s
Data output amplitude		500 mV p-p typical, 450 mV p-p minimum
Data output levels	High	0 mV typical, –50 mV minimum
	Low	–450 to –600 mV
Data rise / fall time		6 ps typical, 8 ps maximum
Data RMS jitter		400 fs typical, 1000 fs maximum
Data output connector type		V female (1.85 mm)
Internal clock data rate		39.8 Gb/s standard 28 Gb/s (OPTC28) 25.78125 Gb/s (OPTC26)
External clock input	Frequency	Half-rate input (11 to 22 GHz)
	Power	+13 dBm minimum, +16 dBm maximum
Pattern trigger	Rate	1/64 * pattern repetition rate
	Pulse Width	64 * UI
Power requirements		100 to 240 V AC, 50 to 60 Hz, 1.35 A maximum
N4968A clock and data demultiplexer 44 Gb/s (TR1D4A)		
Data output signal configuration		Differential. Will operate in single ended mode with unused input terminated
Data input bit rate		3.5 to 44 Gb/s
Data input amplitude range		150 to 1000 mV single ended
Data input connector type		V female (1.85 mm)
Clock input	Frequency	Half-rate input (1.725 to 22 GHz)
	Amplitude	470 to 1200 mV p-p
Data output	Bit rate	Half-rate input (11 to 22 GHz)
	Configuration	Single ended. Unused outputs must be terminated
	Amplitude	210 to 270 mV, 240 mV nominal
	Connector type	K female (2.92 mm)
Clock outputs	Configuration	Differential. Can be used single ended. All unused outputs must be terminated.
	Divide ratio	Configurable - divide by 2/4/8/16
	Amplitude	500 mV single ended, typical
	Connector type	K female (2.92 mm)
Power requirements		100 to 240 V AC, 50 to 60 Hz, 1.35 A maximum
N4965A-CTR multi-channel BERT controller (PCB12500) with N4956A-E12 12.5 Gb/s error detector remote head (TR2P1A), N4957A-C12 clock doubler remote head (TG3C1A)		
Data rate	1.5 to 12.5 Gb/s	
Data line coding	Non-return to zero (NRZ)	
Data patterns	2^N–1 PRBS patterns (N=7, 10, 15, 23, 31)	
Data input sensitivity	0.1 to 2.0 V, single ended	
Data output amplitude	500 mV p-p typical, 450 mV p-p minimum	
Data threshold adjustment	–1.0 to +1.0 V, 1mV steps	
Data delay adjustment	–1000 to +1000 UI, 1 mUI steps	
Autoalign	Sets optimum data threshold and data delay	
BER measurement period	0 to 99,999.999 seconds in 1 msec steps	
BER results	Bit error rate, error count, bit count, measurement seconds	
Data connectors	K female (2.92 mm)	
Remote control interface	IEEE-488 (GPIB) or USB2.0	
Power requirements	100 to 240 V AC, 50 to 60 Hz, 1.35 A maximum	

Physical and Environmental

Temperature, operating	+10 °C to +40 °C
Temperature, non-operating	–40 °C to +70 °C

Dimensions (height, width, and depth)		
N4974A PRBS generator 40 Gb/s (TG1P4A)	(TG1P4A)	63.5 mm (2.5 in) x 230.2 mm (8 in) x 254 mm (10 in)
N4968A clock and data demultiplexer 44 Gb/s	(TR1D4A)	63.5 mm (2.5 in) x 254 mm (10 in) x 254 mm (10 in)
N4965A-CTR multi-channel BERT controller	(PCB12500)	100 mm (3.9 in) x 214 mm (8.4 in) x 425 mm (16.7 in)
N4956A-E12 12.5 Gb/s error detector remote head	(TR2P1A)	33 mm (1.3 in) x 72 mm (2.8 in) x 130 mm (5.1 in)
N4957A-C12 clock doubler remote head	(TG3C1A)	33 mm (1.3 in) x 72 mm (2.8 in) x 130 mm (5.1 in)

Mass		
N4974A PRBS generator 40 Gb/s	(TG1P4A)	2.7 kg (6 lbs)
N4968A clock and data demultiplexer 44 Gb/s	(TR1D4A)	3.2 kg (7 lbs)
N4965A-CTR multi-channel BERT controller	(PCB12500)	3.3 kg (7.1 lbs)
N4956A-E12 12.5 Gb/s error detector remote head	(TR2P1A)	0.38 kg (13.4 oz)
N4957A-C12 clock doubler remote head	(TG3C1A)	0.38 kg (13.4 oz)

Regulatory standards

EMC

- CISPR Pub 11 Group 1, Class A
- AS/NZS CISPR 11
- ICES/NMB-001

This ISM device complies with Canadian ICES-001.
Cet appareil ISM est conforme a la norme NMB-001 du Canada.

Ordering Information

Model	Description
Serial BERT System 40 Gb/s (SB40B)	1x N4974A PRBS generator 40 Gb/s (TG1P4A) 1x N4968A clock and data demultiplexer 44 Gb/s (TR1D4A) 1 x N4965A multi-channel BERT controller (PCB12500) 4x N4956A-E12 12.5 Gb/s error detector remote head (TR2P1A) 1x N4957A-C12 clock doubler remote head (TG3C1A) 1x Accessory kit containing: • 1x 10 dB coupler SMA • 1x male-male SMA adapter • 1x 25.4 cm (10″) RF cable SMA male-male for splitting internal clock to go to generator clock in • 2x 91.5 cm (36″) RF cable SMA male-male for connecting clocks to N4968A clock and data demultiplexer 44 Gb/s (TR1D4A) and N4965A multi-channel BERT controller (PCB12500) • 2x 14.0 cm (5.5″) RF cable 1.85 mm male-male for connecting N4974A PRBS Generator 40 Gb/s (TG1P4A) to N4968A clock and data demultiplexer 44 Gb/s (TR1D4A) in loopback mode • 1x CD with LabView drivers, manuals, setup guide.
N4974A PRBS generator 40 Gb/s (TG1P4A)	1x power supply with AC power cable 1x Semi-rigid RF cable SMA male-male for connecting internal clock out to generator clock in 1x 3 dB attenuator 1.85 mm male-female for providing termination when connecting to AC coupled devices 1x 50 Ω terminator 1.85 mm male for unused output when driving single ended devices 1x adjustment tool for phase delay control 1x manual
N4968A clock and data demultiplexer 44 Gb/s (TR1D4A)	1x Power supply with AC power cable 2x 1.85 mm to 2.92 mm RF adapters for adapting to lower data rate devices 1x 50 Ω terminator 1.85 mm male for unused input when driven from single ended devices 4x SMA 50 Ω terminators SMA male for unused de-multiplexed data outputs 3x Semi-rigid RF cables SMA male-male for configuring clock output dividers & routing 1x Allen wrench for locking phase adjustment control 1x manual Standard 1 year warranty.
N4965A multi-channel BERT controller (PCB12500)	1x AC power cord 1x printed quick start guide 1x CD with LabView drivers, users guide, quick start guide
N4956A-E12 12.5 Gb/s error detector remote head (TR2P1A)	2x 12.7 cm (5 in) RF cables SMA male-male 1x SMA male-male 50 Ω terminator
N4957A-C12 clock doubler remote head (TG3C1A)	2x 12.7 cm (5 in) RF cables SMA male-male 1x SMA male-male 50 Ω terminator

Product Options

N4967A serial BERT system 40 Gb/s (SB40B)

N4967A-101 internal clock change for operation at 25.78125 Gb/s

N4967A-102 internal clock change for operation at 28 Gb/s

N4974A-300 high speed clock for continuous operation from 22 to 44 Gb/s
Includes N4963A clock synthesizer 13.5 GHz (TG1C1A); N4965A-CTR multi-channel BERT controller (PCB12500); N4957A-C12 clock doubler remote head (TG3C1A); N4985A-S30 30 GHz system amplifier (TA0L30VA)

Typical configurations

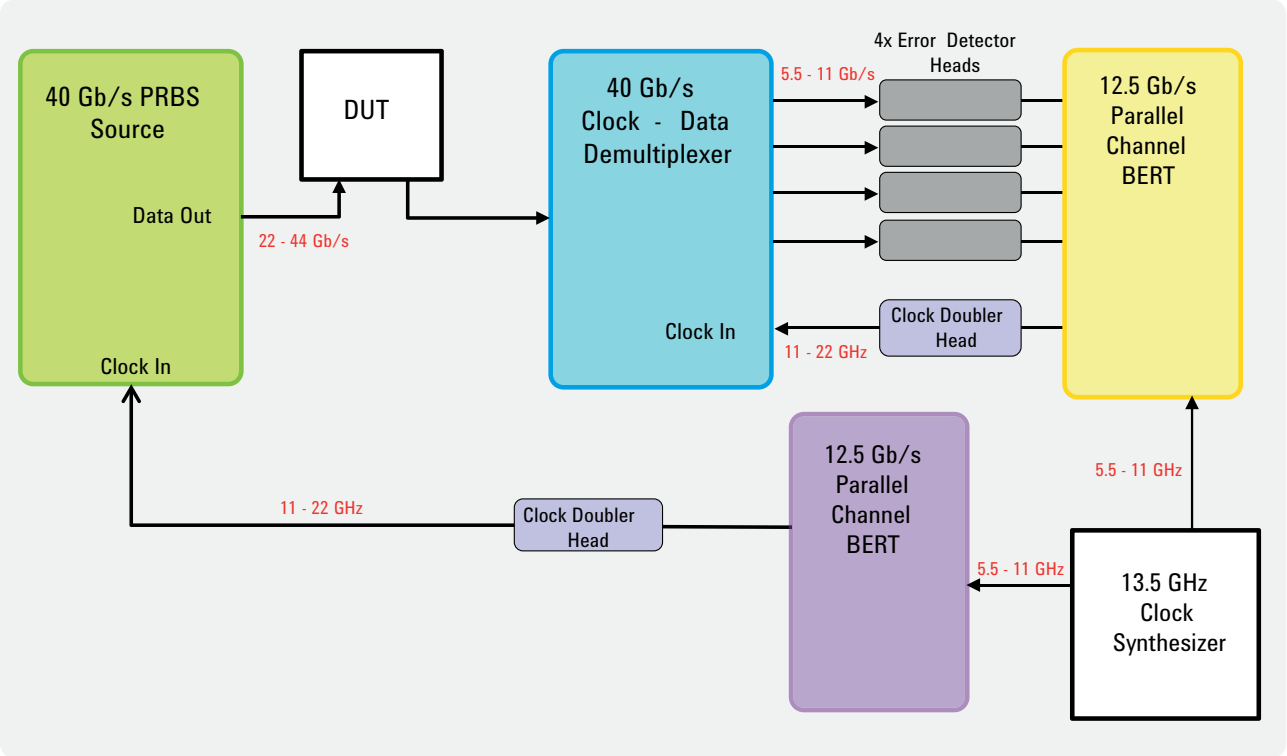

Figure 6. Typical test setup with OPTHSC high speed clock option

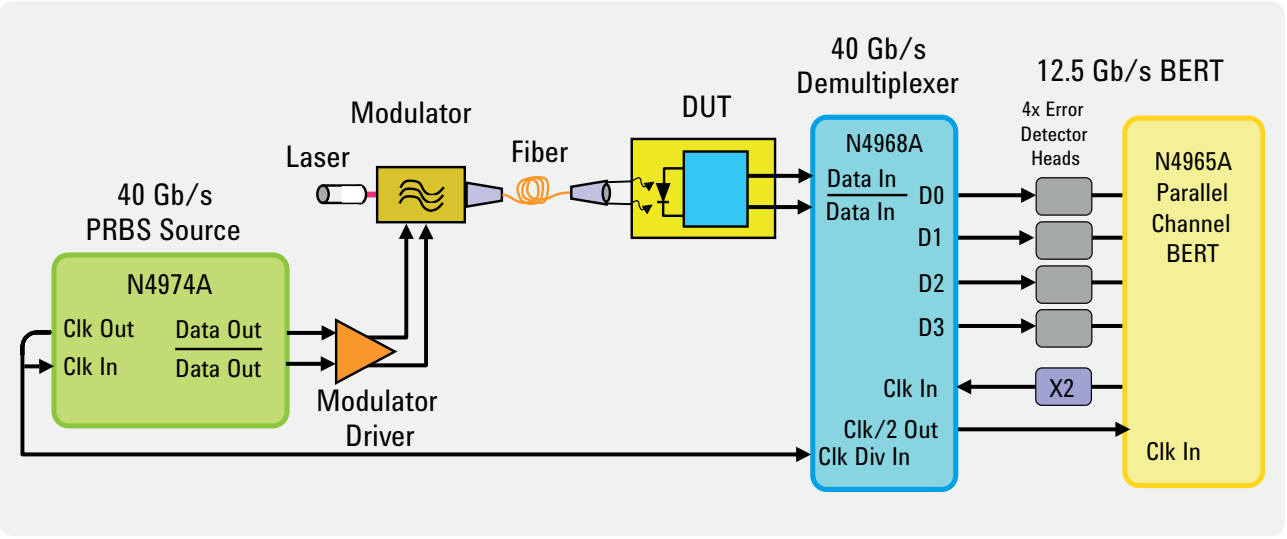

Figure 7. Typical BER test system for 40 Gb/s optical receiver

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