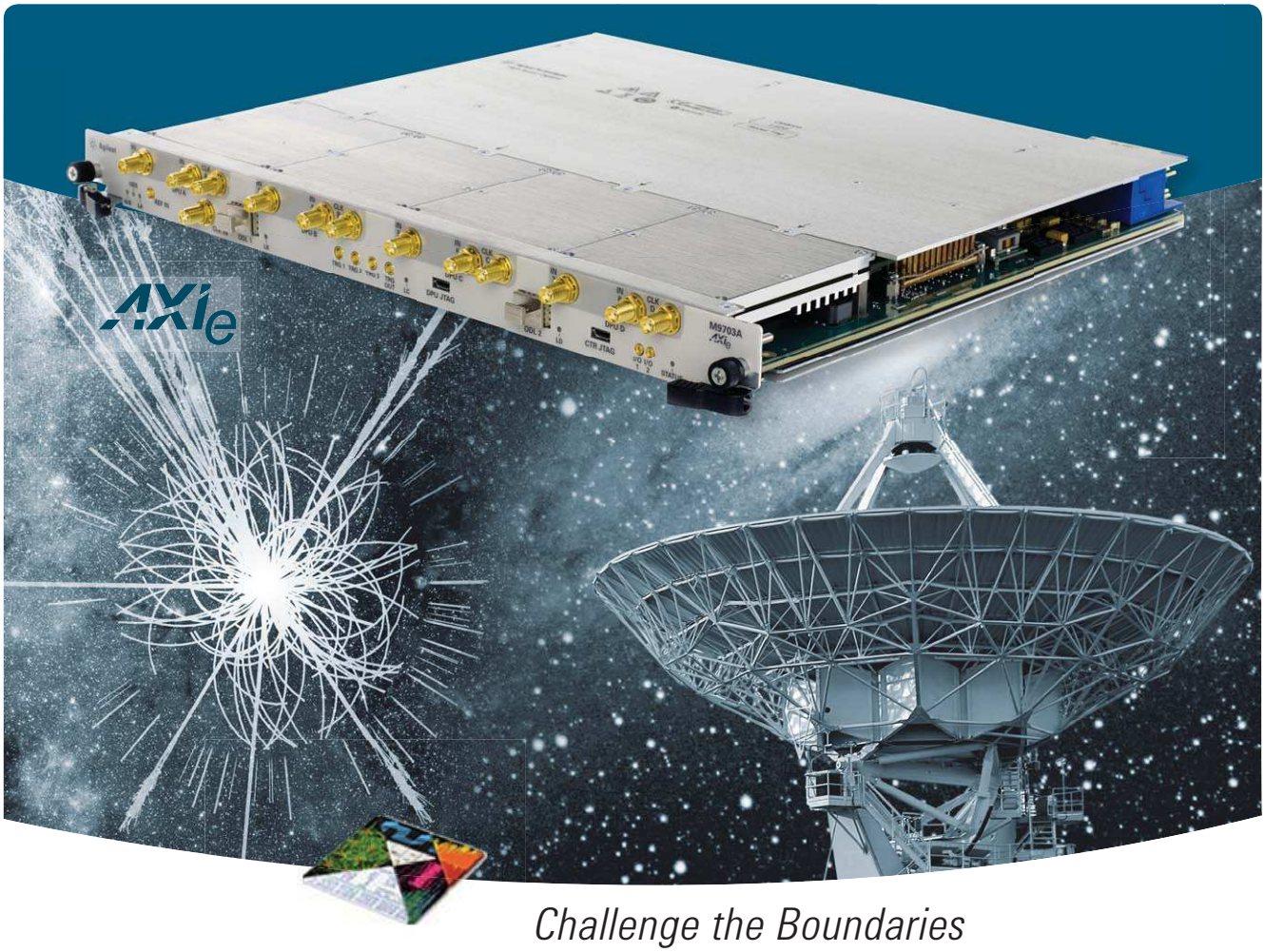
Agilent M9703A

AXIe High-Speed Digitizer

Data Sheet

8 channels, 12-bit,
Up to 3.2 GS/s, DC-2 GHz



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OVERVIEW

Introduction

The Agilent M9703A is the fastest versatile DC-coupled 12-bit digitizer, providing exceptional measurement fidelity and wide bandwidth. Based on the AXIe standard, offering eight acquisition channels in a single-slot card it provides excellent channel density and flexible scalability. This allows the creation of many GHz speed channels in a small volume, making the M9703A high-speed digitizer ideal for large-scale applications in advanced physics and aerospace & defense.

Product Description

The Agilent M9703A is a revolutionary 8-channel, 12-bit digitizer, able to capture signals from DC up to 2 GHz at 1.6 GS/s with exceptional measurement accuracy. An interleaving capability allows two channels to be combined to acquire at 3.2 GS/s on four channels from DC to 1 GHz with high measurement accuracy.

The M9703A high-speed digitizer also provides very long acquisition memory and real-time data processing capability with four Virtex 6 FPGAs.

The on-board FPGAs can feature an optional real-time digital downconverter (DDC) that allows tuning and zooming on the signal to be analyzed. The DDC functionality improves the dynamic range, reduces the noise floor, extends the capture time, and accelerates the measurement speed.

The M9703A high-speed digitizer can also be combined with the Agilent 89600 VSA software for advanced multi-channel measurement analysis.

Applications

- Advanced research experiments such as hydrodynamics or plasma fusion
- Radar and satellite communication application such as multi-antenna calibration/test or beam-forming
- Multi-channel phase-coherent back-forming R&D

Features

- 8 channels (4 when interleaving)
- 12-bit resolution
- Up to 3.2 GS/s sampling rate (with -SR2 and -INT options)
- DC to 2 GHz input frequency range (with -F10 option in non interleaved acquisition)
- 1 V / 2 V selectable full scale range (FSR)
- Accurate time-to-trigger interpolator (TTI)
- Up to 4 GB (256 MSamples/ch) on-board memory
- PCIe backplane providing >650 MB/s data transfer speed
- Wideband digital downconverter (DDC)
  - 8 phase-coherent channels with independent local oscillators (LO) setting, tunable with 0.01 Hz resolution
  - Adjustable analysis bandwidth from 300 MHz down to less than 1 kHz
  - Magnitude trigger

Customer Values

- Measure wideband and fast signals with high dynamic range
- Easily scale phase-coherent acquisition channels in small space
- High measurement throughput
- Long acquisition memory
- Reduced test time by tuning and zooming on signals (requires -DDC option)
  - Isolate the signal of interest
  - Improve the dynamic range
  - Extend the capture time, or reduce the amount of transferred data
  - Trigger on the signal of interest

EASY SETUP ... TEST ... AND MAINTENANCE

Hardware Platform

Product overview

The M9703A is a flexible modular AXIe 12-bit digitizer offering scalable features depending on application requirements. The standard configuration implements 8 channels of DC to 650 MHz (-3 dB analog bandwidth) input frequency range, and acquiring data at 1 GS/s. If higher speed is required, the -SR2 option enables the eight channels to sample at 1.6 GS/s. An interleave option (-INT) also allows two channels to be combined and reach 3.2 GS/s in 4-channel acquisition mode. For higher frequency signals, the -F10 option provides an extended input frequency range of DC up to 2 GHz in non interleaved mode, or DC to 1 GHz when interleaving channels[1].

Data processing

The M9703A implements five Xilinx Virtex-6 FPGAs; one controlling the module functionality and data flow, and four dedicated to real-time data processing. The four data processing units (DPU) implement a standard digitizer functionality firmware by default, allowing digitization of the signal, storage of the resulting data in the on-board memory and transfer through the PCIe backplane bus.

The four DPUs may optionally feature a real-time digital downconverter (DDC) IP algorithm if ordered with the -DDC option. The DDC allows tuning and zooming on the signals to be analyzed, improving the dynamic range, reducing the noise floor, extending the capture time, and accelerating the measurement speed.

Compliance

The M9703A is compliant with AXIe and AdvancedTCA (ATCA) formats. Designed to benefit from fast data interfaces, the product can be integrated into AXIe or ATCA chassis slots. Based on ATCA, the AXIe standard implements extensions for instrumentation and test, and uses clever techniques to add powerful timing features.

Software Platform

IO Libraries

Agilent IO Libraries Suite offers FAST and EASY connection to instruments and the newest version extends that capability to include modular instruments.

The Agilent IO Libraries Suite helps you by displaying ALL of the modules in your system, whether they are PXI, PXIe, or AXIe. From here you can view information about the installed software or launch the modules' soft front panel directly from Agilent Connection Expert.

In addition, the Agilent Connection Expert (ACE) offers an easy way to find the correct driver for your instrument.

Drivers

The M9703A AXIe digitizer is supplied with a comprehensive portfolio of module drivers, documentation, examples, and software tools to help you quickly develop test systems with your software platform of choice. The module comes with IVI-C, IVI-COM, and LabVIEW software drivers to work in the most popular development environments, such as MATLAB, LabVIEW, Microsoft C/C++ or C#. These drivers are provided for Windows and Linux operating systems.

Easy software integration

To help you get started and complete complex tasks quickly, the module software is provided with context sensitive help, complete documentation and code examples that allow a quick module set up and basic acquisition functionalities. These code examples can be easily modified, so that the card can be quickly integrated into a measurement system. Included are application code examples for LabVIEW, LabWindows/CVI, Visual Studio C, C++, and C#, and MATLAB which provide digitizer set up and basic acquisition functionality.

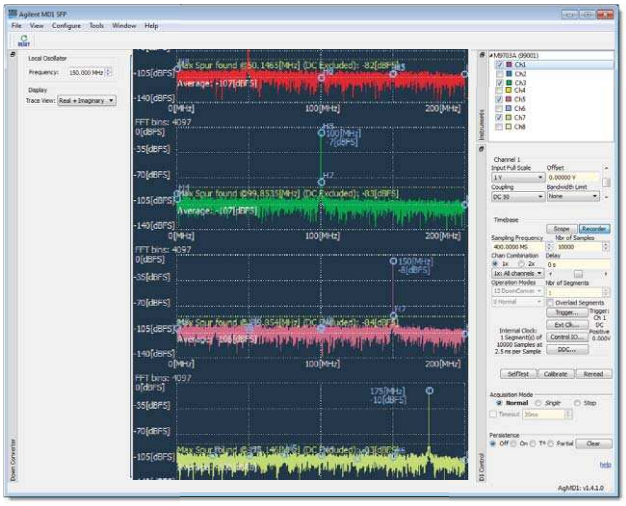


Figure 1. Agilent M9703A MD1 software front panel (SFP) interface.

Software applications

In addition, the M9703A includes the Agilent MD1 soft front panel (SFP) graphical interface. This simple software application can be used to control, verify the functionality and explore the capabilities of the Agilent modular high-speed digitizers. The MD1 SFP provides several different measurement and display capabilities, one being an FFT plot of the acquired signal. For advanced measurement analysis, the M9703A AXIe high-speed digitizer can be combined with Agilent's 89600 Vector Signal Analysis software, the industry's standard for signal analysis and demodulation.

[1] *The fact that there is less frequency range when interleaving channels is due to internal characteristics of the analog-to-digital converter chipset that filters at 1 GHz when combining channels.*

Firmware options

The M9703A high-speed digitizer provides two firmware options:

- DGT: Digitizer firmware (standard)
- DDC: Digital downconverter

The -DGT option features a standard digitizer firmware that is included in the default configuration. The digitizer firmware allows standard data acquisition, including: Digitizer initialization, setting of the acquisition and clocking modes, management of channel triggering for the best synchronization, storing the data in the internal memory and/or transferring them through the backplane bus. The digitizer firmware also implements segmented acquisition functionality. The digitizer firmware supports fixed internal clocking frequency with internal, external or backplane reference, and variable frequency external clock.

The -DDC option, in addition to the basic digitizer functionality, implements a real-time digital decimation and filtering on the digitized data, allowing the user to tune and zoom on the signals of interest. This exclusive IP algorithm provides very powerful and flexible digital downconversion on all 8 channels. The filters and local oscillators (LO) are synchronized to maintain constant phase and timing relationships to allow phase-coherent post processing. The DDC provides three main functions:

- **Data reduction (zoom)**

Reducing the bandwidth and sample rate to match the analyzed signal decreases the amount of data that needs to be transferred for a given capture duration, in turn accelerating post-processing operations.

- **Frequency shifting (tune)**

Independently shifting each channels IF signal into baseband, allows the analysis bandwidth to be set around the signal of interest.

- **Magnitude trigger**

Setting the magnitude level that a signal needs to achieve at a specified frequency and bandwidth allows triggering only on the signal of interest.

These three functions allow isolating the signal of interest from other signals in crowded spectrum, and improving the dynamic range as the integrated noise is reduced, increasing the SNR and effective number of bits (ENOB). The resulting advantage for your application is a reduced test time, while improving overall test efficiency.

The M9703A high-speed digitizer with the digital downconverter option may also be used as a digital IF when combined with external RF conversion hardware, such as the Agilent M9362A-D01 quad downconverter.

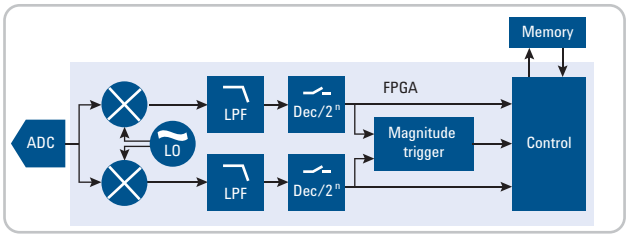


Figure 2. Single channel digital downconverter (DDC) simplified block diagram.

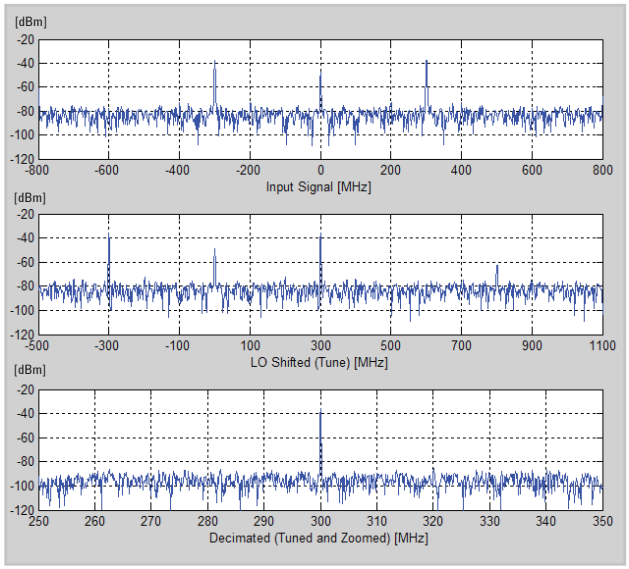


Figure 3. Example of the DDC functionality. The 1st graph shows the FFT of a 300 MHz sinusoid signal being digitized at 1.6 GS/s, then the LO is set to shift the center frequency at the signal frequency and finally a decimation ratio of 16 is applied, reducing the analyzed bandwidth to 100 MHz around the signal of interest.

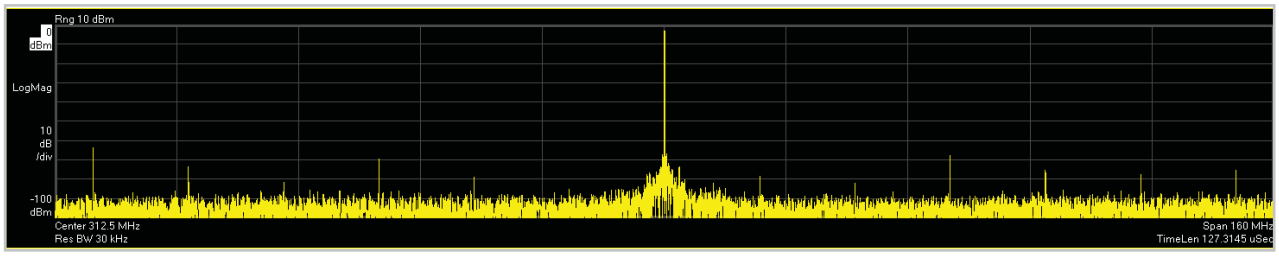


Figure 4. Spectrum of a 300 MHz sinusoid signal acquired with the Agilent 89600 VSA software. The DDC LO frequency and decimated sampling rate settings are directly accessible from the VSA user interface by providing the desired center frequency and frequency span. In this case, the analysis bandwidth is 160 MHz around a center frequency of 312.5 MHz, showing the excellent noise level performance of the M9703A digitizer.

TECHNICAL SPECIFICATIONS AND CHARACTERISTICS

Analog Input (IN1 to IN8 SMA connectors)

Number of channels			8 (eight), 8 or 4 (with INT option)
Impedance			50 Ω ±2 %
Coupling			DC
Full scale ranges (FSR)			1 V and 2 V
Maximum input voltage			1V FSR: 3 V RMS, ± 3.6 Vpk 2V FSR: 4.3 V RMS, ± 6.3 Vpk
Input frequency range (–3 dB bandwidth)			DC to 1.9 GHz *(typical)* in 1V FSR at 1 GS/s or 1.6 GS/s DC to 2.0 GHz *(typical)* in 2V FSR at 1 GS/s or 1.6 GS/s DC to 1.2 GHz *(typical)* in 1V FSR at 2 GS/s or 3.2 GS/s DC to 1.1 GHz *(typical)* in 2V FSR at 2 GS/s or 3.2 GS/s
DC gain accuracy			± 0.5% *(typical)* in 1V FSR ± 0.7% *(typical)* in 2V FSR
Offset accuracy			± 0.5% in 1V FSR ± 1.5% in 2V FSR
Time skew [1]	Channel-to-channel skew [2] Channel-to-channel skew stability [3]		± 50 ps *(nominal)* ± 200 fs pk *(nominal)* 75 fs RMS *(nominal)*
Phase offset	Channel-to-channel offset (@ 400 MHz) Channel-to-channel offset stability [3]		± 7.2° *(nominal)* ± 0.03° pk *(nominal)* 0.01° RMS *(nominal)*
Input voltage offset			–2xFSR to +2xFSR
Bandwidth limit filters (BWL)			650 MHz *(nominal)*
Frequency response flatness			± 1 dB from DC to 650 MHz
Effective bits (ENOB) [4]		@ 48 MHz	9.0 *(typical)*
		@ 100 MHz	9.1 *(typical)*
		@ 410 MHz	8.2 *(8.9, typical)*
Signal to Noise Distortion (SNR) [4]		@ 48 MHz	58 dB *(typical)*
		@ 100 MHz	58 dB *(typical)*
		@ 410 MHz	54 dB *(56 dB, typical)*
Spurious Free Dynamic Range (SFDR) [4]		@ 48 MHz	59 dBc *(typical)*
		@ 100 MHz	63 dBc *(typical)*
		@ 410 MHz	52 dBc *(60 dBc, typical)*
Total Harmonic Distortion (THD) [4]		@ 48 MHz	–59 dB *(typical)*
		@ 100 MHz	–62 dB *(typical)*
		@ 410 MHz	–60 dB *(typical)*
Noise spectral density (NSD)		@ 48 MHz	–147.6 dBm/Hz *(nominal)*
		@ 100 MHz	–147.6 dBm/Hz *(nominal)*
		@ 410 MHz	–146.7 dBm/Hz *(nominal)*

[1] The channel-to-channel skew is defined as the magnitude of time delay difference between two digitized channel inputs, granted the same signal is provided to each channel at the exact same time.

[2] The measurement represents the maximum time skew between 8 channels of a single unit, measured with a Sinefit method on 100k samples, for a sinusoid signal at 400 MHz and averaged 10 times.

[3] Skew and offset stability are measured at 25 °C in a climatic chamber. The skew and offset between channels are measured every 5 minutes over 12 hours and after 1hour stabilization time and the values represent the dispersion of the measurements.

[4] Measured at 1.6 GS/s for a -1 dBFS input signal in internal clock mode with F10 option.

TECHNICAL SPECIFICATIONS AND CHARACTERISTICS, CONTINUED

Digital Conversion

Resolution		12 bits
Acquisition memory (total)		1 GB (standard, 64M real samples/ch) 2 GB option (M20, 128M real samples/ch) 4 GB option (M40, 256M real samples/ch)
Sample clock sources		Internal or external
Internal clock source		Internal, external or backplane reference
Max. real-time sampling rates		1 GS/s per channel (standard) 1.6 GS/s per channel option (SR2) 1-2 GS/s option (INT) 1.6-3.2 GS/s option (INT, SR2)
Sampling jitter		225 fs *(nominal)* [1]
Clock accuracy		±1.5 ppm
External clock source (CLK IN SMA connector)		
Impedance		50 Ω *(nominal)*
Frequency range [2]		1.8 GHz to 2 GHz (standard) 1.8 GHz to 3.2 GHz (SR2)
Signal level		+5 dBm to +15 dBm *(nominal)*, 0 V DC
Coupling		AC
External reference clock (REF IN MCX connector)		
Impedance		50 Ω *(nominal)*
Frequency range		100 MHz ±100 kHz *(nominal)*
Signal level		–3 dBm to +3 dBm *(nominal)*
Coupling		AC
Time stamps		48-bit sample counter
Acquisition modes		Single shot, sequence (up to 65536 segments. Segment maximum length = memory size/number of channels)

Digital Downconverter (DDC option only)

Acquisition modes		Basic digitizer or DDC digitizer [3, 4]
Number of synchronous DDC channels		8
Frequency tuning range (LO)		DC to 1.6 GHz (with F10)
Center frequency tuning resolution		0.01 Hz
Independent channel center frequency tuning		Yes
Frequency span (decimated bandwidth)	-SR1 -SR2	180 MHz [5] and $100/2^n$ MHz (n = 0, 1, ..., 18) 300 MHz [5] and $160/2^n$ MHz (n = 0, 1, 2, ...,18)
Decimated sampling rate	-SR1 -SR2	250 MS/s [5] and $125/2^n$ MS/s (n = 0, 1, ..., 18) 400 MS/s [5] and $200/2^n$ MS/s (n = 0, 1, 2, ...,18)
Independent channel span		No
Maximum acquisition memory time	-SR1 -SR2	1.024 s and $1.024*2^n$ s (n = 0,1,2,...,18) 0.64 s and $0.64*2^n$ s (n = 0,1,2,...,18)

[1] Jitter figure based on phase noise integration from 100 Hz to 1600 MHz.

[2] The sampling rate corresponds to half of the external clock frequency in 8-channel mode (non interleaved channels). In interleaved mode (only available with the INT option), the sampling rate corresponds to the frequency of the external clock signal.

[3] The real-time DDC is active only for 1 GS/s and 1.6 GS/s sampling rate modes (non-interleaved mode).

[4] In DDC mode, each sample is a pair or I & Q samples. Each sample is coded on 64 bits (32-bit I and 32-bit Q) when the decimation factor is >4, otherwise the coding is made on 32 bits (16-bit I and 16-bit Q).

[5] Limited aliasing protection at 250 MS/s and 400 MS/s for signals wider than 250 MHz and 400 MHz respectively.

DDC Decimation Steps

Decimated sampling rate	Analysis bandwidth	Maximum number of samples	Maximum accquisition time
400 MS/s*	300 MHz*	134216951	0.336 s
200 MS/s	160 MHz	67108087	0.336 s
100 MS/s	80 MHz	67108087	0.671 s
50 MS/s	40 MHz	67108087	1.342 s
25 MS/s	20 MHz	67108087	2.684 s

Table 1. Five first steps of decimated sampling rates with corresponding analysis bandwidth and maximum memory achieved when using the DDC with the -SR2 option (1.6 GS/s).

** The decimation by 4 filter has full tuning resolution, but has limited aliasing protection for signals wider than 400 MHz.*

Trigger

Trigger modes	Edge (positive, negative), level, magnitude [1]
Trigger sources	External, Software, channel
Channel trigger frequency range	DC to 250 MHz
External trigger (TRG 1, TRG 2, TRG 3 MCX connectors)	
Coupling	DC
Impedance	50 Ω *(nominal)*
Level range	± 5 V *(nominal)*
Amplitude	0.5 V pk-pk
Frequency range	DC to 2 GHz
Trigger time resolution	6 ps *(nominal)*
Rearm time [2]	1 us *(nominal)* in non-interleaved channels mode 0.8 us *(nominal)* in interleaved channels mode
Trigger out (TRG OUT MCX connector) [3]	
Signal level	1.15 Vpk–pk *(nominal)*
Rise/fall time	9 ns / 19 ns *(nominal)*

Control IO (I/O A and I/O B MMCX connectors)

Functions	Output	Acquisition active Trigger is armed Trigger accept resynchronization 10 MHz reference clock Low level High level

[1] *Only with -DDC option.*
[2] *With -DGT option at 1.6 GS/s.*
[3] *At 10 MHz on a 50 Ω load.*

TECHNICAL SPECIFICATIONS AND CHARACTERISTICS, CONTINUED

Environmental and Physical [1]

Temperature Range	Operating Non-operating	0 °C to +45 °C –40 °C to +70 °C
EMC		Complies with European EMC Directive 2004/108/EC • IEC/EN 61326-1 • CISPR Pub 11 Group 1, class A • AS/NZS CISPR 11 • ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.

Power Dissipation

–48 V	Total Power
3.4 A *(typical)*	161 W *(typical)*, with -DGT option
3.6 A *(nominal)*	170 W *(nominal)*, with -DDC option

Mechanical Characteristics

Form Factor	1 slot AXIe
Size	30 mm W x 322.2 mm H x 280 mm D
Weight	3 kg (6.61 lbs)

System Requirements

Operating Systems	Windows® XP, Service Pack 3	Windows® Vista, SP1 and SP2, Windows® 7 (32-bit and 64-bit), All versions	Linux Kernel 2.6 or higher (32 or 64-bit), Debian 6.0, CentOS 5
Processor speed	600 MHz or higher required 800 MHz recommended	1 GHz 32-bit (x86), 1 GHz 64-bit (x64), no support for Itanium 64	As per the minimum requirements of the chosen distribution
Available Memory	256 MB minimum (1 GB or greater recommended)	1 GB minimum	As per the minimum requirements of the chosen distribution
Available Disk Space [3]	1.5 GB available hard disk space, includes: • 1 GB available for Microsoft .NET Framework 3.5 SP1 [2] • 100 MB for Agilent IO Libraries Suite	1.5 GB available hard disk space, includes: • 1 GB available for Microsoft .NET Framework 3.5 SP1 [2] • 100 MB for Agilent IO Libraries Suite	100 MB
Video	Super VGA (800x600) 256 colors or more	Support for DirectX 9 graphics with 128 MB graphics memory recommended (Super VGA graphics is supported)	Does not require graphics (headless system). X Windows with 1280x1024 recommended for SFP
Browser	Microsoft® Internet Explorer 6.0 or greater	Microsoft® Internet Explorer 7 or greater	Distribution supplied browser

[1] *Samples of this product have been type tested in accordance with the Agilent Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.*

[2] *NET Framework Runtime Components are installed by default with Windows Vista. Therefore, you may not need this amount of available disk space.*

[3] *Because of the installation procedure, less disk space may be required for operation than is required for installation. The amount of spacelisted above is required for installation.*

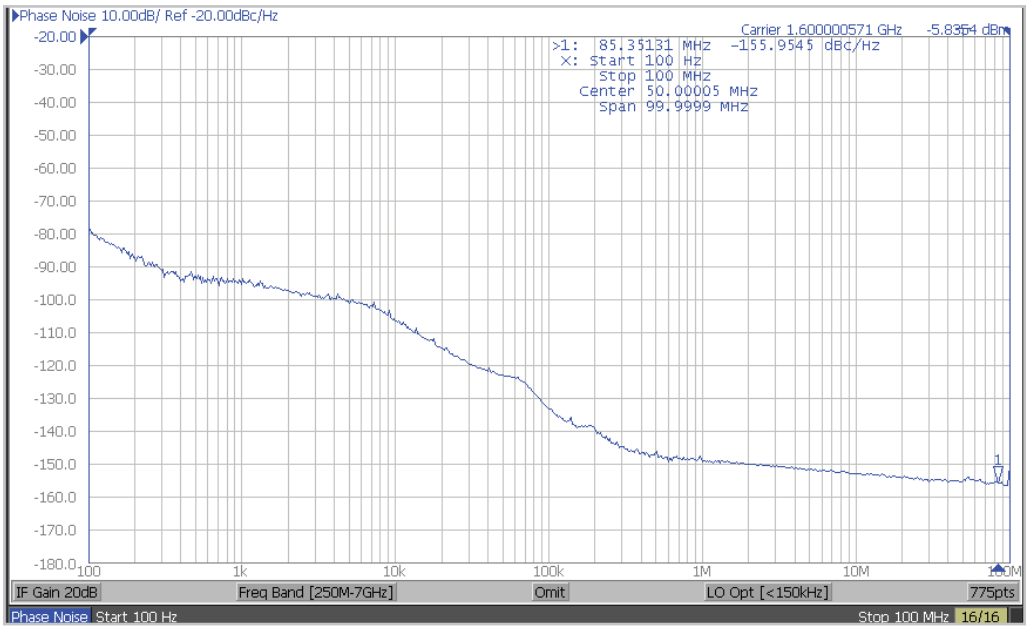


Figure 5. Measured sampling clock phase noise with an internal reference clock.

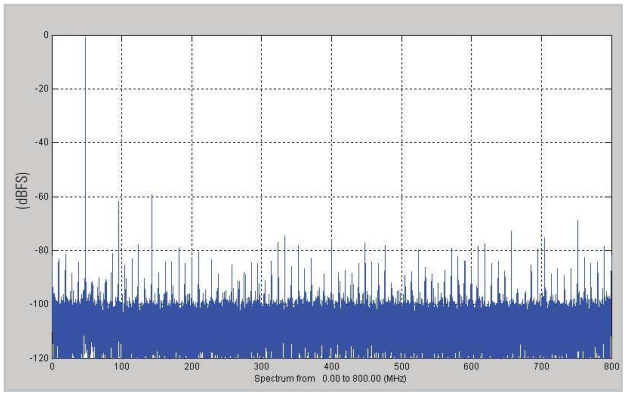


Figure 6. M9703A nominal dynamic performance in 1 V FSR for a –1 dBFS input signal at 48 MHz.

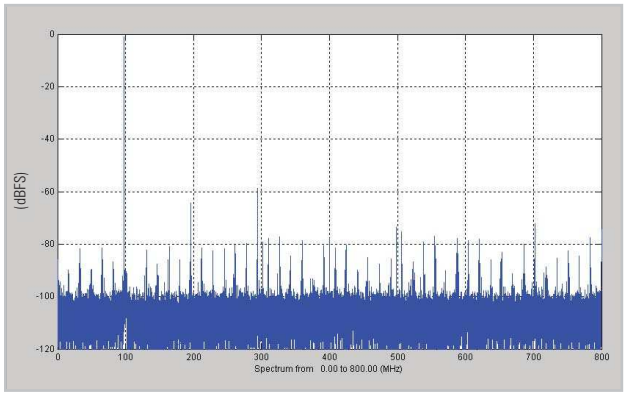


Figure 7. The FFT plot for a -1 dBFS input signal at 100 MHz in 1 V FSR shows the excellent dynamic range of the M9703A high-speed digitizer.

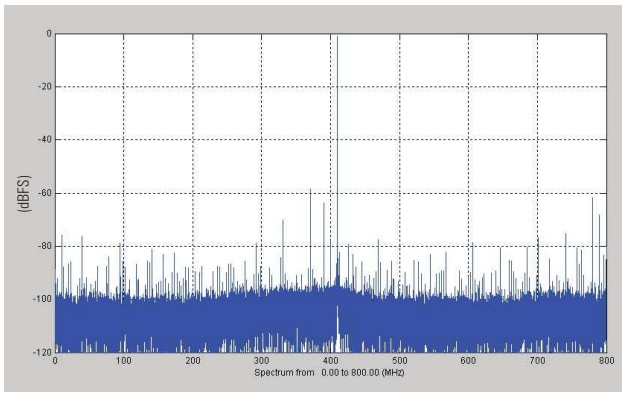


Figure 8. M9703A nominal dynamic performance in 1 V FSR for a –1 dBFS input signal at 410 MHz. Note how the dynamic range is still excellent for high frequency signals.

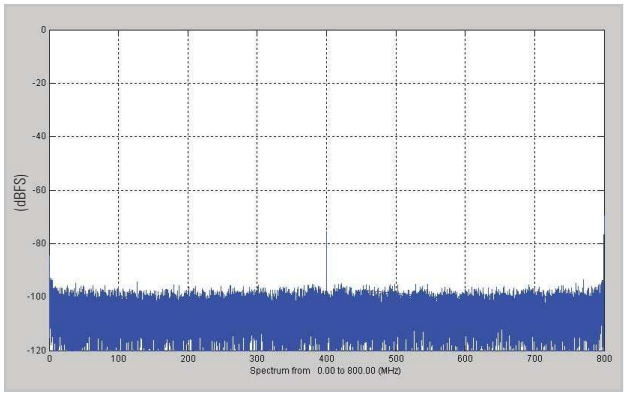


Figure 9. The M9703A nominal dynamic performance in 1 V FSR with no input signal (open input) shows a very low noise floor.

Front Panel Connectors

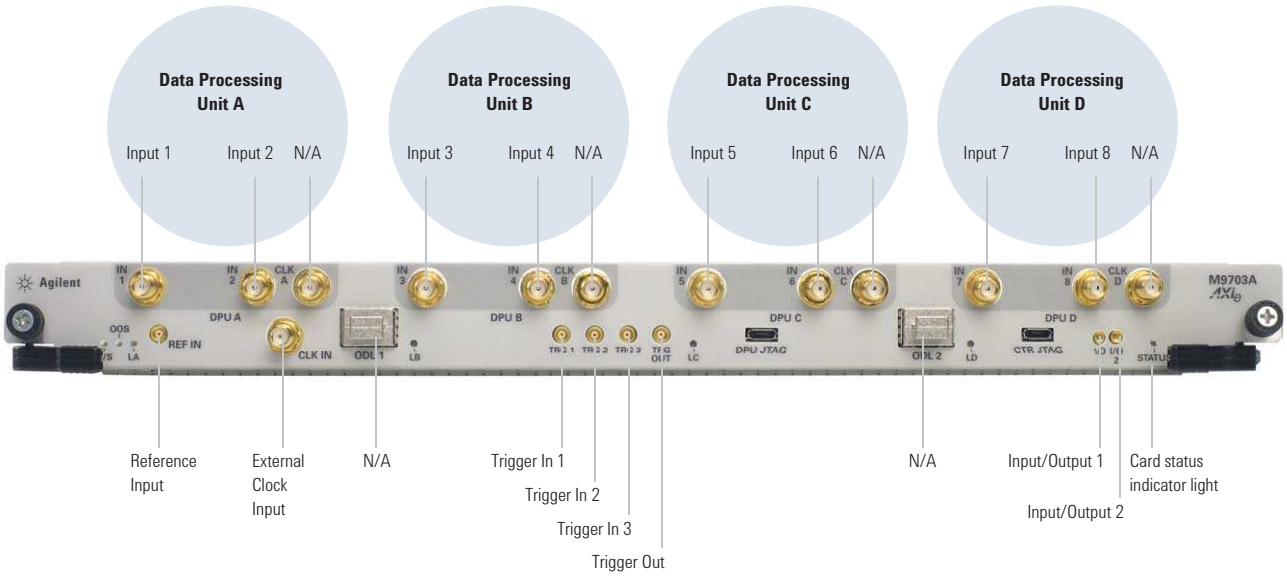


Figure 10. Five Agilent M9703A AXIe 12-bit digitizers installed in the Agilent M9505A 5-slot AXIe chassis to form a 40-channel 12-bit acquisition system.

Figure 11. One Agilent M9703A AXIe 12-bit digitizers and one M9536A embedded AXIe controller installed in the Agilent M9502A 2-slot AXIe chassis.

Definitions for specifications

Specifications describe the warranted performance of calibrated instruments that have been stored for a minimum of 2 hours within the operating temperature range of 0 to 45 °C, unless otherwise stated, and after a 45 minute warm-up period. Data represented in this document are specifications unless otherwise noted.

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics are often referred to as Typical or Nominal values.

- ***Typical*** describes characteristic performance, which 80% of instruments will meet when operated over a 20 to 30 °C temperature range. Typical performance is not warranted.

- ***Nominal*** describes representative performance that is useful in the application of the product when operated over a 20 to 30 °C temperature range. Nominal performance is not warranted.

Note: All graphs contain measured data from several units at room temperature unless otherwise noted.

Calibration intervals

The M9703A is factory calibrated and shipped with a calibration certificate.
Calibration is recommended every year in order to verify product performance.

CONFIGURATION AND ORDERING INFORMATION

Software Information

Chassis Slot Compatibility: AXIe, ATCA

Supported operating systems	Microsoft Windows® XP (32-bit) Microsoft Windows® 7 (32/64-bit) Microsoft Windows® Vista (32/64-bit) Linux
Agilent IO Libraries	Includes: VISA Libraries, Agilent Connection Expert, IO Monitor

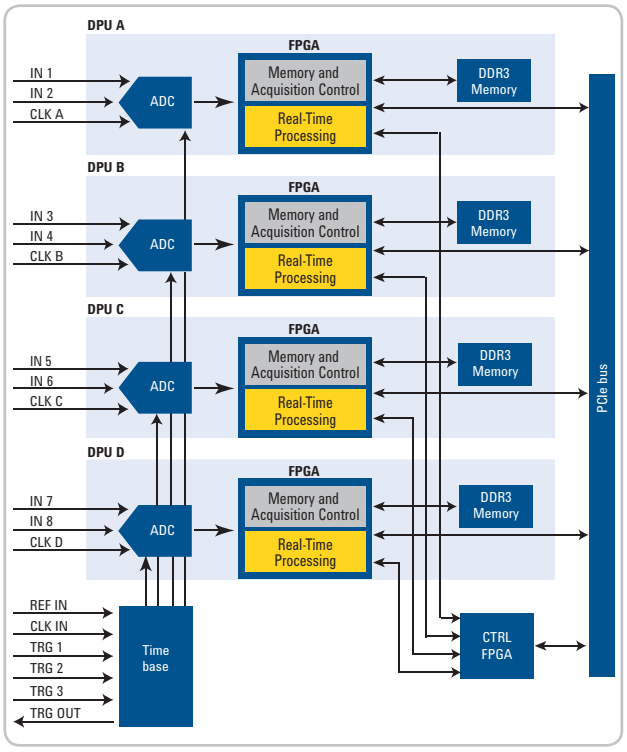


Figure 12. Simplified block diagram of the M9703A AXIe Digitizer.

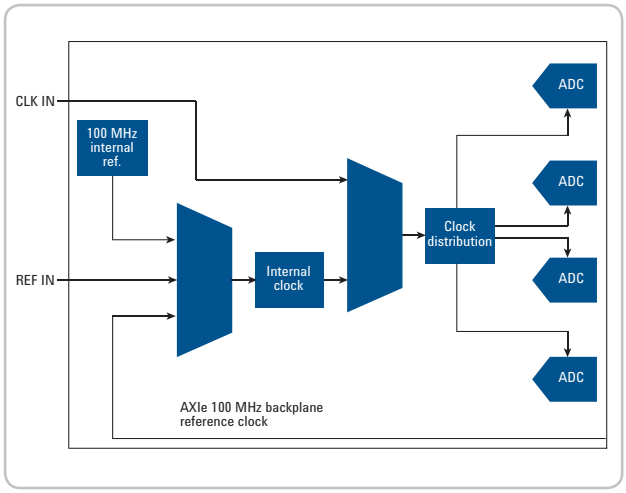


Figure 13. M9703A clocking mode simplified block diagram.

Ordering Information

Model [1]	Description
Typical Product Configuration	
M9703A	AXIe 12-bit Digitizer
M9703A-SR1 [1]	1 GS/s sampling rate
M9703A-SR2	1.6 GS/s sampling rate
M9703A-INT	Interleaved channel sampling functionality
M9703A-F05 [1]	Input frequency: DC to 650 MHz
M9703A-F10	Input frequency: DC to 2 GHz (not interleaved) DC to 1 GHz (interleaved)
M9703A-M10 [1]	1 GB (64 MS/ch) acquisition memory
M9703A-M20	2 GB (128 MS/ch) acquisition memory
M9703A-M40	4 GB (256 MS/ch) acquisition memory
M9703A-DGT [1]	Digitizer firmware
M9703A-DDC	Digital down-conversion firmware

[1] *These options represent the standard configuration of the M9703A.*

Typical System Configuration

M9703A	8-channel, 12-bit, AXIe Digitizer
M9505A	5-slot AXIe chassis
M9047A	PCIe desktop PC adapter: Gen 2, x 8

Related Products

M9502A	2-slot AXIe chassis
M9505A	5-slot AXIe chassis
M9536A	Embedded AXIe controller
U1092A	AcqirisMAQS Multichannel Acquisition Software
89601B	89600 VSA software, transportable license

Accessories

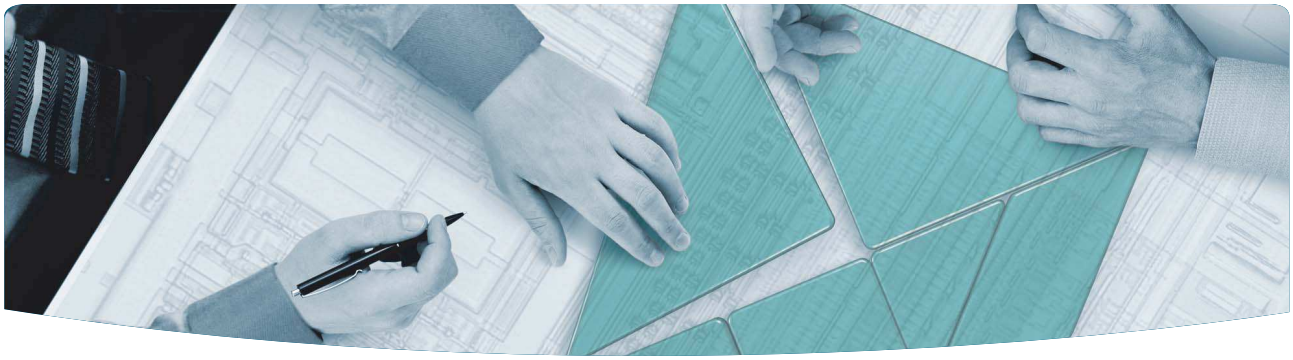
Software and product information on CD (included)

Advantage Services: Calibration and Warranty

Agilent Advantage Services is committed to your success throughout your equipment's lifetime.

Warranty

M9703A-UK6	Commercial calibration certificate calibration with test data
R-51B-001-3C	1-year, return-to-Agilent warranty extended to 3 years
R-51B-001-5C	1-year, return-to-Agilent warranty extended to 5 years



The Modular Tangram

The four-sided geometric symbol that appears in this document is called a tangram. The goal of this seven-piece puzzle is to create identifiable shapes—from simple to complex. As with a tangram, the possibilities may seem infinite as you begin to create a new test system. With a set of clearly defined elements—hardware, software—Agilent can help you create the system you need, from simple to complex.

Challenge the Boundaries

Agilent Modular Products

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