

Protection in Portable Electronics Applications.

FEATURES

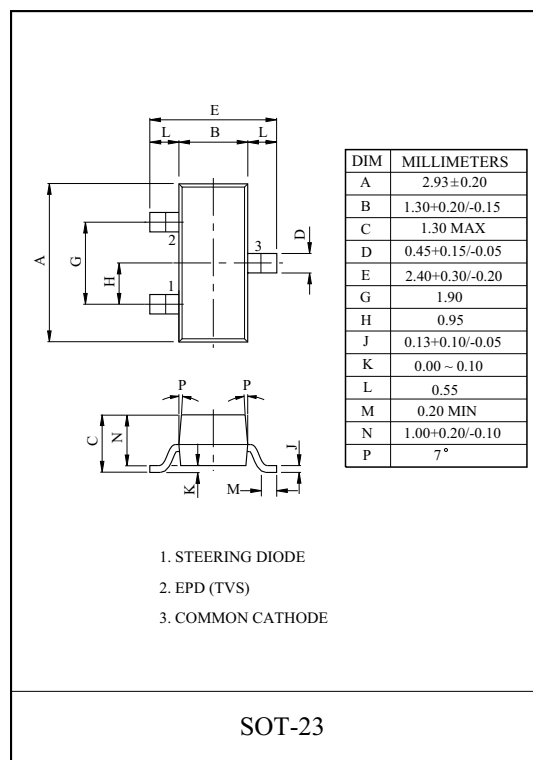
- EPD(Enhanced Punch-Through Diode) Structure.
- 400 Watts peak pulse power ($t_p=8/20\mu s$)
- Transient protection for high-speed data lines to
IEC 61000-4-2(ESD) 15kV(Air), 8kV(Contact)
IEC 61000-4-4(EFT) 40A($t_p=5/50ns$)
IEC 61000-4-5(Lightning) 24A($t_p=8/20\mu s$)
- One device protects one directional line.
- Tow devices protect two high-speed line pairs.
- Low capacitance.
- Low leakage current.
- Low operating and clamping voltage.

APPLICATIONS

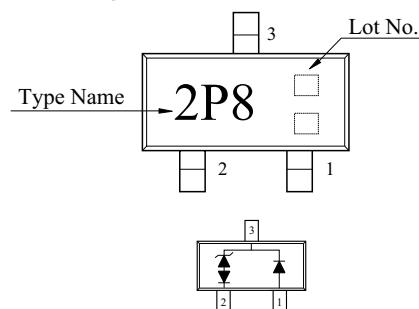
- Cellular Phone Handsets and Accessories.
- Microprocessor based equipment.
- Personal Digital Assistants (PDA's)
- Notebooks, desktops PC, & servers.
- High-Speed data lines.
- Laser Diode Protection.
- LAN/WAN equipment.
- 10/100 Ethernet.

MAXIMUM RATING ($T_a=25^\circ C$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Pulse Power ($t_p=8/20\mu s$)	P_{PK}	400	W
Peak Pulse Current ($t_p=8/20\mu s$)	I_{PP}	24	A
Operating Temperature	T_j	-55 ~ 150	$^\circ C$
Storage Temperature	T_{stg}	-55 ~ 150	$^\circ C$



Marking



PG2.8CUS23

ELECTRICAL CHARACTERISTICS (Ta=25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Reverse Stand-Off Voltage	V _{RWM}	Pin 3 to 2 or Pin 1 to 2	-	-	2.8	V
Punch-Through Voltage	V _{PT}	I _{PT} =2 μA, Pin 3 to 2	3.0	-	-	V
Snap-Back Voltage	V _{SB}	I _{SB} =50mA, Pin 3 to 2	2.8	-	-	V
Reverse Leakage Current	I _R	V _{RWM} =2.8V, Tc=25 °C Pin 3 to 2 or Pin 1 to 2	-	-	1	μA
Clamping Voltage	V _C	I _{PP} =2A, tp=8/20 μs, Pin 3 to 2	-	-	3.9	V
		I _{PP} =5A, tp=8/20 μs, Pin 3 to 2	-	-	7	
		I _{PP} =24A, tp=8/20 μs, Pin 3 to 2	-	-	12.5	
		I _{PP} =5A, tp=8/20 μs, Pin 1 to 2	-	-	8.5	
		I _{PP} =24A, tp=8/20 μs, Pin 1 to 2	-	-	15	
Junction Capacitance	C _J	V _R =0V, f=1MHz (Pin 3 to 1&2) [Pin 1&2 tied together]	-	70	100	pF
		V _R =0V, f=1MHz (Pin 1 to 2) [Pin 3 N.C.]	-	5	10	
Steering Diode Characteristics						
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Reverse Breakdown Voltage	V _{BR}	I _t = μA, Pin 3 to 1	40	-	-	V
Reverse Leakage Current	I _R	V _{RWM} =2.8V, Tc=25 °C, Pin 3 to 1	-	-	1	μA
Forward Voltage	V _F	I _F =1A, Pin 1 to 3	-	-	2	V

EPD TVS Characteristics.

The EPD TVS employs a complex npnp structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. The EPD mechanism is achieved by engineering the center region of the device such that the reverse biased junction does not avalanche, but will “punch-through” to a conducting state. This structure results in a device with superior dc electrical parameters at low voltages while maintaining the capability to absorb high transient currents.

The IV characteristic curve of the EPD device is shown in figure 1. The device represents a high impedance to the circuit up to the working voltage (V_{RWM}). During a transient event, the device will begin to conduct as it is biased in the reverse direction.

When the punch-through voltage (V_{PT}) is exceeded, the device enters a low impedance state, diverting the transient current away from the protected circuit. When the device is conducting current, it will exhibit a slight “snap-back” or negative resistance characteristic due to its structure. This must be considered when connecting the device to a power supply rail. To return to a non-conducting state, the current through the device must fall below the snap-back current. (approximately <50mA.)

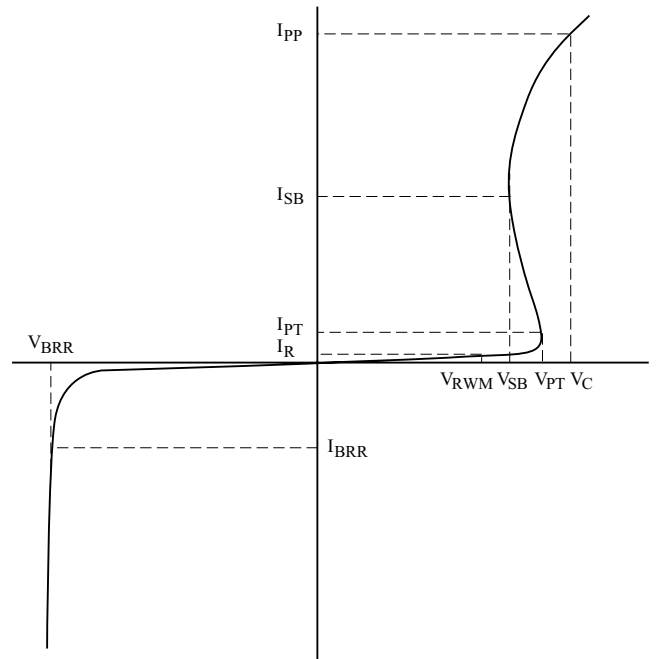
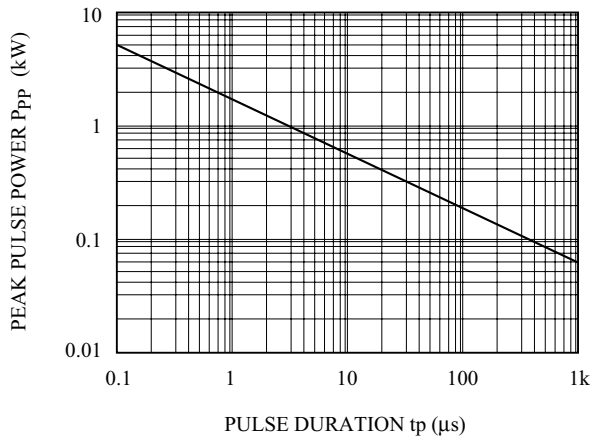
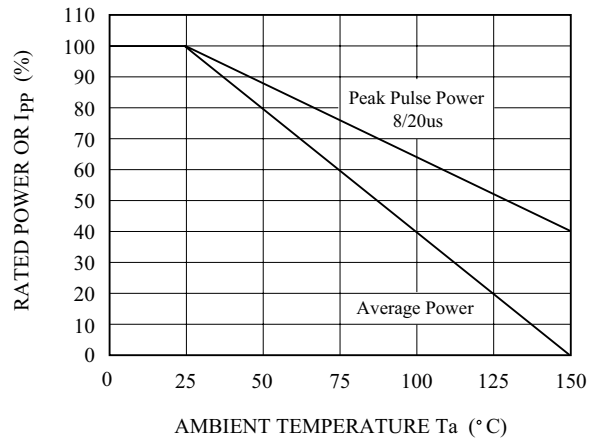


Figure 1. EPD TVS VI Characteristic curve.

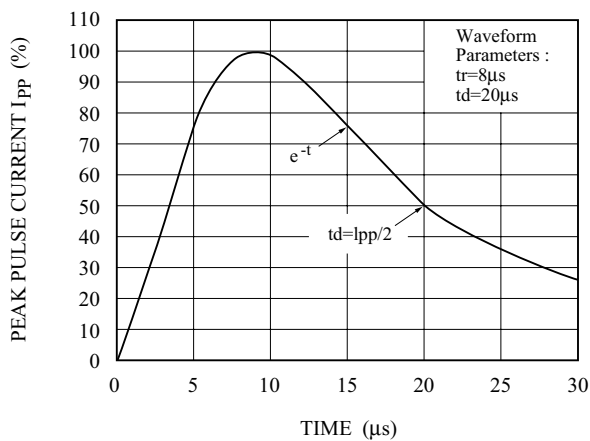
NON-REPETITIVE PEAK PULSE
POWER VS. PULSE TIME



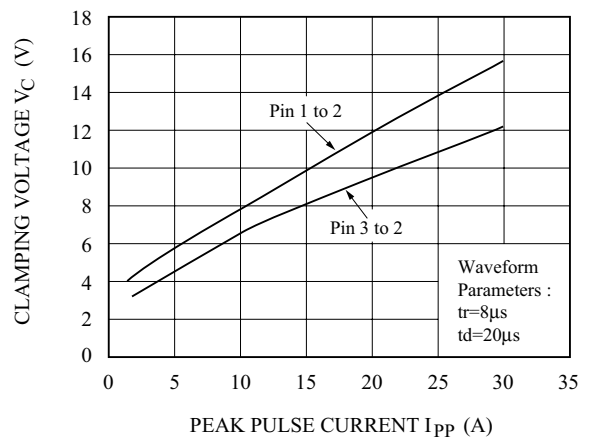
POWER DERATION CURVE



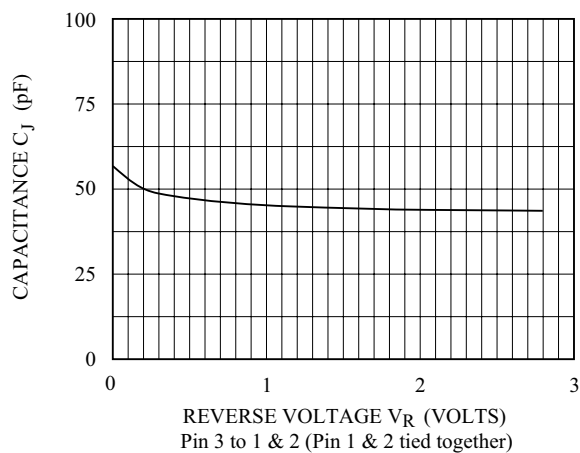
PULSE WAVEFORM



CLAMPING VOLTAGE VS.
PEAK PULSE CURRENT



$C_J - V_R$



$C_J - V_R$

